Indian Express. page no. 13 dt. 29.02.2024



Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY

BDA Outer Ring Road, Mallathahally, Bengaluru - 560 056 Tel - 080- 23211232 & Mob No -9986003865

AIT/SS/3579/2023-24

Date: 28.02.2024

TENDER NOTIFICATION

Sealed quotations are invited from Reputed/Authorized firms for supply & Installation of the following Equipment.

- A) Equipment to E&C Dept Under VGST Grant.
- B) Xilinx FPGA Spartan 6 trainer Kits to ETE Dept.

Details and specification of requirements can be downloaded from college website www.drait.edu.in. The sealed quotation shall be attached with a DD of Rs.500/- for each item on or before 27.03.2024 and submit the sealed quotations on or before 28.03.2024 by 1.00 PM. Quotations will be opened on the same day i.e.28.03.2024 at 4.00 PM.

Sd/- Principal

Sd/- Secretary, PVPWT

EXECUT No. 4119

Bids for upto 06: be visite http://sp procurer NIB No.:-UBN No.: DIPR/C/12



HDFC B

Regd. Office: HDFC Bank House, Se

Branch: #51, HDFC H

Tel:-080-41183000 CIN L65920

E-AUCTION SALE NOTICE (Sale)

E-Auction Sale Notice for Sale of Immovable Assets under the Securitization of Security Interest Act, 2002 read with proviso to Rule 9(1) of the

The Authorised Officer of HDFC Bank Limited (erstwhile HDFC Limited having amalgamated with HI NCLT-Mumbai vide order dated 17th March 2023) (HDFC) issues E-Auction Sale Notice for Sale of Assets and Enforcement of Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act, 2002 read with proviso to Rule 9 (1) of the Security Interest Act,

TENDERFORM

N	0.		
14	υ.	_	

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY

(An Autonomous Institution, Aided by Govt. of Karnataka, Affiliated to VTU & Approved by AICTE, New Delhi)

BDA Outer Ring Road, Near Jnanabharathi Campus, Mallathalli, Bengaluru – 560 056

Country Code (91) + STD Code 080, Tel – 23211232, MOB NO -9986003865

www.drait.edu.in e-mail: principal@drait.edu.in

		The state of the s	
AIT/SS/ 3579 /2023-	24		Date: 28.02.2024
To,			
M/s			

SUB: Invitation quotations for supply and installation of Xilinx FPGA 6 trainer kits to Electronics & Telecommunication Engineering Department. - Reg.

You are invited to submit your most competitive price for supply and installation Xilinx FPGA 6 trainer kits to Electronics & Telecommunication Engineering Department with the following description.

S1.#	SPECIFICATIONS	Qty.	Rate Rs.	Amount Rs.
1	Xilinx FPGA 6 trainer kits	12 Nos		
	NOTE: Detailed description/Specification is here with enclosed			

2. Bid Price

- a) The quotation shall be for the full quantity as described above. Corrections if any, should be made by strike off and rewrite with new figure duly attested with date.
- b) All duties, taxes and other levies (Show separately) payable by the supplier shall be included in the total price of the tender amount.
- c) The rates quoted by the bidder shall be fixed for the product and escalation clause not allowed.
- d) The prices should be quoted in Indian Rupees only.
- 3. Each bidder shall submit only one quotation.
- 4. Validity of Quotation: The validity of the quotation should be mentioned in the tender which is not less than 90 days.
- 5. No Advance payment.
- 6. Evaluation of Quotations

The purchaser will evaluate and compare the quotations determined to be substantially responsive i.e. which are

(a) properly signed, (b) confirm to the terms and conditions, and (c) specifications.

nology

 $\left(\frac{1}{3}\right)$

Award of Contract

The purchase order will be placed with the supplier whose quotation has been determined to be substantially responsive and who has offered the lowest evaluated quotation price.

- 8. The bidder whose bid is accepted will be notified of the award of contract by the purchaser prior to expiration of the quotation validity period. The terms of the accepted offer shall be incorporated in the purchase order.
- 9. Payment shall be made after delivery and satisfactory installation as per our specification.
- 10. You can obtain tender form from the Store section by paying Rs.500/- in DD OR can download from the website of the Institution www.drait.edu.in. and should be accompanied DD for Rs.500/- as tender document fees. DD should be in favor of Principal Dr.AIT, Bangalore.
- 11. You are requested to provide your offer latest by 1.00 pm on 28.03.2024 along with a bank draft at 2% of the bidding amount or tender price(Including taxes) on the total amount in favour of "The Principal Dr.AIT Bangalore," as EMD/Quotations that do not accompany EMD are liable to be rejected.
- 12. Quotations will be opened on 28.03.2024 at 4.00 pm in the Principal's chamber.
- 13. Sealed quotations shall be addressed to the purchaser at the following address: The Principal, Dr. Ambedkar Institute of Technology, Stores Section, Near Jnanabharathi Campus, Mallathahalli, Bangalore - 560 056. with super scribing "Quotation for supply and installation of Xilinx FPGA 6 trainer kits to Electronics & Telecommunication Engineering Department.
- 14. Insurance
 - The goods supplied under the contract shall be fully insured in Indian Rupees against loss or damage incidental to manufacture or acquisition, transportation, storage and delivery.
- 15. The Guarantee & warranty period must be specified clearly.
- 16. The bidder shall provide the copy of the following.
 - i) Previous year I.T Filed copy. ii) GST Number iii) Copy of PAN.
 - iv) Venders list of the previous supply & at least two performance certificates from the Venders. v) Previous two years Audit report.
- 17. Bidders Should Qualify Eligibility Criteria as mentioned in the specification.
- 18. Notwithstanding the above, the purchaser reserves the right to accept or reject any of the quotations / to cancel the bidding process and reject all quotations without assigning any reasons at any time prior to the award of the purchase/
- 19. We look forward to receiving your quotations and thank you for your interest in this procurement.

Dr. Ambedkar Institute of Technology



Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BANGALORE-560 056. Department of Electronics & Telecommunication Engineering

Xilinx FPGA Spartan 6 Trainer Kit specifications

- 32 Nos. of digital input using slide switches with LED indication
- 32 Nos. of digital output using discrete LEDs.
- 16× 2 LCD is provided for display the text message.
- · One Reset Switch.
- One switch for giving manual clock.
- FPGA configuration through.
 - On board Xilinx USB to JTAG Programmer with isolation to configure FPGA
- On board Flash Prom XCF04S (Programmable through USB to JTAG programmer).
- Total 186 I/O Pins: 100 Pins used for integrating peripheral like LED, Switches etc., balance pins are available to user in 3numbers of 20 pin header.
- 1 Number of 26 pin header to interface VLIM cards like Traffic Light Controller / On-board TLC.
- On board programmable PLL oscillator from 1 MHz to 100MHz using jumpers
- 4Nos of 7 segment LED display.
- One relay and Buzzer.
- Stepper & DC motor drive requried on board (Motors Required)
- 4x4 matrix key.
- On board I2C RTC Interface.
- On board Temperature Sensor Interface.
- SPI Based Analog to Digital Converter and Digital to Analog Converter.

Lab Incharge

Proveen. K.B.

Dept. of Electronics & Telecommunication Engg. Dr. Ambedkar Institute of Technology

Bengaluru-560 056

Dr. Ambedkar Institute of Technology

Bengaluru-560 056