Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)

BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr.AIT/ECE/356 Date : 05.07.2018

To

Director (Admin & HR)
KPTCL, Kaveri Bhavan
Bengaluru - 560 009,
Karnataka.

Subject: Internship for Engineering student of Electronics and Communication.

Dear Sir/Madam,

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bengaluru. It is an autonomous institution affiliated to Visvesvaraya Technological University (VTU) Belagavi. The Institute is aided by the Government of Karnataka, approved by All India Council for Technical Education (AICTE) New Delhi.

In reference to the above context Mr. Chinmaya G bearing USN: 1DA15EC037 is a bonafide student of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and has completed 3rd Year examination in June 2018 and he offers himself to be candidate for the "Internship". He may be extended all facilities for Internship in the Supervisory Control and Data Acquisition (SCADA) section of your organization in the month of July 2018 (4 weeks).

The candidate will be governed by the rules and regulations of your department and Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the said period of training. All the cost with regard to travel and incidentals will be borne by the individual concerned. Upon completion of Internship, a report should be forwarded to us.

5/7/18

HOD

(Dr. G.V. Jayaramaiah)
Head of the Department
Dept. of Electronics & Communication Engg.,
Dr. Ambedkar Institute of Technology.
Bengaluru-560 056

(Dr. C Nanjundaswamy)
Principal,
Dr. Ambedkar Institute of Technology

Principal
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

KARNATAKA POWER TRANSMISSION CORPORATION LIMITED

No: KPTCL/HRDC/B-75/89311/18-19/ 1333-34

HRD Centre, KPTCL, Whitefield Road,
Hoody, Bengaluru-560048.
Email: admnhrdckptcl@gmail.com
Date: 9 AUG 2018

To,

The Principal,
Dr. Ambedkar Institute of Technology,
Bengaluru.

Sir,

Sub: Completion of Internship training on **"SCADA in KPTCL"** – Reg.

Ref: Letter No: KPTCL/ HRDC/ B-75/ 89311/ 18-19/ 871-73 Dated: 11.07.2018.

Vide letter cited under ref, approval was accorded to **Chinmaya. G.,** USN No: 1DA15EC037, pursuing B.E course (Third Year) in Electronics and Communication Engineering, at Dr. Ambedkar Institute of Technology, Bengaluru to do Internship training on **"SCADA in KPTCL"** under the guidance of Sri. S. B. Chandrashekaraiah, Executive Engineer (Ele), SCADA (Designs), KPTCL, Anand Rao Circle, Bengaluru.

Sri. S. B. Chandrashekaraiah, Executive Engineer (Ele), SCADA (Designs), KPTCL, Anand Rao Circle, Bengaluru has certified that the student has successfully completed the Internship training, within the specified period from 12th July 2018 to 31st July 2018. The student will submit the copy of the report personally to your office for further needful.

Yours faithfully,

9/8/18

Administrator,
HRDC, KPTCL

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
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BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Date : 18.5.2018

Ref. No. Dr. AIT/EC/207/18-19

To
The Human Resource Manager,
Bosch Ltd.,
Naganathapura, Bangalore-560100

18th May 2018

Sir/Madam,

SUB: Permission to carryout internship at your organization.

This is to certify that Sunil DP (USN: 1DA15EC173) student of Dr. Ambedkar Institute of Technology, studying B.E in Electronics and Communication Engineering, would like to apply for internship under Bosch Ltd. for a period of 30days. It gives immense opportunity to acquire knowledge and help the student gain hands-on experience.

Further, it is stated that the student wish to do internship in Bosch Ltd. with all his interest. We would be grateful for considering the case for internship.

Thanks and Regards,

18/5/18

(Dr. Jayaramaiah G V)
Head of Department, ECE
Dr. Ambedkar Institute of Technology

(Dr. C Nanjundaswamy)
Principal,
Dr. Ambedkar Institute of Technology

Ph : 23218534, 23211232, 23211505 / 06 / 07, Fax : 080-23217789, E-mail : principal@dr-ait.org, Website : www.dr-ait.

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)

BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. DT.AIT/EC/208/18-19

Date : 18.5.2018

To
The Human Resource Manager,
Bosch Ltd.,
Naganathapura, Bangalore-560100

18th May 2018

Sir/Madam,

SUB: Permission to carryout internship at your organization.

This is to certify that SHASHANK T (USN: 1DA15EC141) student of Dr. Ambedkar Institute of Technology, studying B.E in Electronics and Communication Engineering, would like to apply for internship under Bosch Ltd. for a period of 30days. It gives immense opportunity to acquire knowledge and help the student gain hands-on experience.

Further, it is stated that the student wish to do internship in Bosch Ltd. with all his interest. We would be grateful for considering the case for internship.

Thanks and Regards,

18/5/18

(Dr. Jayaramaiah G V)
Head of Department, ECE
Dr. Ambedkar Institute of Technology

(Dr. C Nanjundaswamy)
Principal,
Dr. Ambedkar Institute of Technology

FROM

SAHANA. S

1DA15EC177

VI th semester 'c' section

ECE department.

Date : 8 May. 2018.

Principal W/C'S

Forwarded & her request may be consider & her own responsibility she may be permitted
Jayaraman G.J 08/5/18

Permitted A
Issue
[signature] 8/5

To,

The Principal

Dr Ambedkar institute of Technology

Subject: Permission letter for Internship letter.

Respected Sir,

I am SAHANA. S having USN 1DA15EC177 studying 3rd year engineering in ECE department I am willing to attending a internship training in (electronics corpation) BEL. Bangalore for a period of 15 days i.e from 1st july to 15th july 2018.

I assume you that my responsibility during this period of training will be mine and of my parents and all the cost with regard to travel and incidentials will be borne by me.

Hence I humbly request you to grant me a request letter to [BEL], Bangalore to allow me to attend the Project training from 1st july 2018 to 15th july 2018. The format of the required letter is attached with this letter.

Thank you.

Parent's sign
Mamatha. B.R

Yours Faithfully

[signature]

[SAHANA. S]

1DA15EC177

As per the recommendation of her Parents. The above student Sahana. S is studying in VI sem 'c' section is interested in attending 15 days internship from 1/07/18 to 15/07/18. Please to the
[illegible] [signature] 8/5/18

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)

BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr. AIT/EC/209/18-19 Date : 18.5.2018

To
The Human Resource Manager,
Bosch Ltd.,
Naganathapura, Bangalore-560100

18th May 2018

Sir/Madam,

SUB: Permission to carryout internship at your organization.

This is to certify that Ranjith L (USN: 1DA15EC122) student of Dr. Ambedkar Institute of Technology, studying B.E in Electronics and Communication Engineering, would like to apply for internship under Bosch Ltd. for a period of 30days. It gives immense opportunity to acquire knowledge and help the student gain hands-on experience.

Further, it is stated that the student wish to do internship in Bosch Ltd. with all his interest. We would be grateful for considering the case for internship.

Thanks and Regards,

18/5/18

(Dr. Jayaramaiah G V)
Head of Department, ECE
Dr. Ambedkar Institute of Technology

(Dr. C Nanjundaswamy)
Principal,
Dr. Ambedkar Institute of Technology

To
The Human Resource Manager,
Associated Cement Company Ltd.,
Wadi(JN), Gulbarga,585225

6th June 2018

Sir/Madam,

SUB: Permission to carryout internship at your organization.

This is to certify that SUJITH KUMAR PATANGE (USN: 1DA15EC149) student of Dr. Ambedkar Institute of Technology, studying B.E in Electronics and Communication Engineering, would like to apply for internship under Associated Cement Company Ltd., for a period of 30days (June 2018). It gives immense opportunity to acquire knowledge and help the student gain hands-on experience.

Further, it is stated that the student wishes to do internship in Associated Cement Company Ltd. with all her interest. We would be grateful for considering the case for internship.

Thanks and Regards,

Jayaramaiah G V 02/6/18

(Dr. Jayaramaiah G V)
Head of Department, ECE
Dr. Ambedkar Institute of Technology

(Dr. C Nanjundaswamy)
Principal,
Dr. Ambedkar Institute of Technology

To,
HoD
The student's parent permitted him for internship and had taken responsible for any damage happen to the company or to the Institution by him. So, I kindly request him to permit to do internship.

[Mentor]
7/6/18

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)

BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr. AIT/EC/385/18-19

Date : 18.07.18

To

Human Resource Department
Electronics Department
Bharat Heavy Electricals Limited
2606, Mysore Road,
Bangalore 560026

Subject: Internship/ In-plant training for B.E. in Electronics and Communication Engineering students

Respected Sir/Madam,

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bengaluru. It is an autonomous institution affiliated to Visvesvaraya Technological University(VTU) Belgavi. The institute is aided by the Government of Karnataka, approved by All India Council for Technical Education (AICTE) New Delhi.

In reference to the above context Ms Chaitra K bearing USN: 1DA15EC030 is Bonafide student of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE(ECE) and she offers herself to be a candidate for the "Internship/ In-plant Training" as a part of her curriculum. She may be extended all facilities for Internship/ In-plant training in your organization on the allotment days i.e. for a period of 20 days (18-07-18 to 5-08-18).

The candidate will be governed by the rules and regulations of your department and Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the period of training. All the cost with regard to travel and incidentals will be borne by the individual concerned. We would be obliged if you could grant permission for the above mentioned student to undergo Internship/ In-plant training successfully.

Thanking you

Yours Sincerely,

Signature of HOD

Signature of PRINCIPAL

Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)
BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. TO Dr.AIT/ECE/364

Date 07.07.2018

The General Manager (HR)

Bharat Electronics Ltd,

BEL Complex,

Bengaluru

Dept. of Electronics and Communication Engg.,
Dr. Ambedkar Institute of Technology.
Bengaluru - 560056

Dear Sir/Madam,

Subject: Internship for B.E in Electronics and Communication Engineering student.

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bengaluru. It is an autonomous institution affiliated to Visvesvaraya Technological University (VTU) Belagavi. The Institute is aided by theGovernment of Karnataka, approved by All India Council for Technological Education (AICTE) New Delhi.

In reference to the above context Ms. KUMUDINI G bearing USN: 1DA15EC072 is a bonafide student of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY who has completed 3rd year in B.E (Electronics and Communication) in June 2018 with overall aggregate of CGPA: 9.33 and she offers herself to becandidate for the "Internship Training". She may be extended all facilities for internship training in your esteemed organization in the month of July 2018.

The candidate will be governed by the rules and regulations of your department and Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY takes the responsibility of safety during the said period of training. All the cost regard to travel and incidentals will be borne by the individual concerned. Upon completion of internship training a report should be forwarded to us.

We hope you consider our request favourably.

Thanking You,

HOD 09/7/18

Signature of HOD
Dept. of Electronics and Communication Engg.,
Dr. Ambedkar Institute of Technology.
Bengaluru - 560056

Signature of PRINCIPAL
Principal
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

TO

The General Manager (HR)

Bharat Electronics Ltd,

BEL Complex,

Bangalore

Dear Sir/Madam,

Subject: Internship for B.E in Electronics and Communication Engineering student.

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bangalore. It is an autonomous institution, Affiliated to Visvesvaraya Technological University (VTU) Belagavi. The Institute is aided by the Government of Karnataka, approved by All India Council for Technological Education (AICTE) New Delhi.

In reference to the above context Ms. KUMUDINI G bearing USN: 1DA15EC072 is a Bonafide student of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY studying in 7th semester of B.E in Electronics and Communication with overall aggregate of CGPA: 9.33 and she offers herself to be a candidate for the "Internship Training". She may be extended all facilities for internship training in your esteemed organization in the month of July 2018.

The candidate will be governed by the rules and regulations of your department and takes the responsibility of safety during the said period of training. All the cost regard to travel and incidentals will be borne by the individual concerned Upon completion of training a report should be forwarded to us.

We hope you consider our request favourably.

Thanking You,

Signature of HOD

Signature of PRINCIPAL

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)

BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr. AIT/ECE/360

Date : 07-07-2018

From

The Principal
Dr.AMBEDKAR INSTITUTE OF TECNOLOGY
BDA Outer Ring Road,Mallathally,
Bengaluru-560056

Dept. of Electronics and Communication Engg.,
Dr. Ambedkar Institute of Technology.
Bengaluru - 560056

To,

The Principal,
TTC/RWF(Rail Wheel Factory),
Yelahanka,
Bengaluru- 560064

Subject: Internship for B.E. in Electronics and Communication Engineering students.

Dear Sir/Madam,

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bengaluru. It is an autonomous institution affiliated to Visvesvaraya Technological University (VTU)Belgavi. The Institute is aided by the Government of Karnataka, approved by All India Council for Technical Education (AICTE)New Delhi.

In reference to the above context Mr. Mahesh Kumar S bearing USN: 1DA15EC080, Ms. Meghana K bearing USN:1DA15EC089, Ms. Niveditha Bhat bearing USN:1DA15EC099, Ms. Prathibha C bearing USN: 1DA15EC108 are bonafide students of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY who have completed 3rd year in BE (ECE) in June 2018 and they offer themselves to be candidates for "INTERNSHIP". They may be extended all facilities for Internship in your organization for the duration of 2 weeks,upto july 2018.

The candidates will be governed by the rules and regulations of your department and Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY owns responsibility of safety during the said period of internship. All the cost with regard to travel and incidentals will be borne by the individuals concerned. Upon completion of internship, a report should be forwarded to us.

HOD 6/7/18

Signature of HOD
Dept. of Electronics and Communication Engg.,
Dr. Ambedkar Institute of Technology.
Bengaluru - 560056

Signature of PRINCIPAL

Ph : 23218534, 23211232, 23211505 / 06 / 07, Fax : 080-23217789, E-mail : principal@dr-ait.org. Website : www.dr-ait.o

FORMAT FOR DECLARATION BY STUDENTS

With reference to the offer for intership / project work vide letter No Dr.AIT/ECE/360 dated 7/7/18 I/We hereby undertake the following.

i) I/We will be doing intership/project work From 15/7/18 to 4/8/18 at Rail Wheel Factory, Yelahanka

ii) I/We am/are not entitled to any remuneration in the form of stipend, salary or allowances of any kind by the Raiway administration / PSU. I/We am/are also not entitled to any pass or PTO form Indian Railway.

iii) I/We would abide by all General rules and regulation of discipline and conduct at the Railway administration / PSU.

iv) I/We am/are liable to compensate to the Railway administration / PSU concerned for any loss or damage to equipment and fittings that may be caused during the course of training in workshops etc.

v) I/We will not be treated as employee of Indian Railway and as such will not be entitled to any compensation or damange from the Railway administration / PSUs for any injury to me/us or my/our property etc.

vi) I/We agree to be under the administrative control and discipline of the Head of the Unit / office concerned.

vii) I/We will not claim any advantage for employment in Indian Railway in future on the basis of the internship/project work.

Date	Name of student	Signature
6/7/18	Kumudini G	Kumudini G
6/7/18	Mahesh Kumar S	S Mahesh Kumar
6/7/18	Meghana K	Meghana K
6/7/18	Niveditha Bhat	Niveditha Bhat
6/7/18	Prathibha C	Prathibha C

Declaration by the Institute

Dr. Ambedkar Institute of Technology (Name of the Institute) undertakes to indemnify Railway administration for any loss or damage to equipment and fittings that may be caused by Mr / Ms or above Students during his / her/their intership / project work with the Indian Railways.

(Authorised Signature)
For Head of the Institute
Stamp

Principal
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

6/7/18

BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr.AIT/ECE/337

Date : 29.06.2018

From

The Principal
Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY
BDA Outer Ring Road, Mallathally
Bengaluru -560056

HOD
Dept. of Electronics and Communication Engg.
Dr. Ambedkar Institute of Technology.
Bengaluru - 560056

To The Human Resource Manager
Wipro Ltd.,
Doddakannelli, Sarjapur Road,
Bangalore – 560035

Subject: Internship Program at Wipro Limited from 9th July 2018 to 5th August 2018.

Dear Sir/Madam,

Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bengaluru. It is an autonomous institution affiliated to Visvesvaraya Technological University (VTU) Belagavi. The institute is aided by the government of Karnataka approved by All India Council for Technical Education (AICTE) New Delhi.

This is to certify that **Pragya Pandey, USN-1DA15EC104** is a bonafide student of **Dr. Ambedkar Institute of Technology, Bangalore** affiliated to **Visveswaraya Technological University**, **Belgavi.**

Further to our discussion, we confirm that Pragya Pandey, USN-1DA15EC104 has been identified to undergo the 1 month internship program as part of their academic curriculum at Wipro Technologies from 9th July 2018 to 5th August 2018.

The candidate will be governed by the rules and regulations of your department and Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the valid period of internship. All the costs with regard to travel and incidentals will be borne by the individuals concerned. Upon completion of internship a report should be forwarded to us.

29/6/18

SIGNATURE OF HOD

HOD
Dept. of Electronics and Communication Engg.
Dr. Ambedkar Institute of Technology.
Bengaluru - 560056

SIGNATURE OF PRINCIPAL

Dr. Ambedkar Institute of Technology

Bangalore-560056

Pragya Pandey
4th Year
Dept. of Electronics and Communication Engineering
Dr. Ambedkar Institute of Technology
Bangalore-560056

gy
Delhi)
6
2018

25 June 2018

The HOD
Dept. of Electronics and Communication Engineering
Dr. Ambedkar Institute of Technology
Bangalore-560056

SUB: REQUEST FOR PERMISSION FOR PURSUING INTERNSHIP WITH WIPRO FROM 9TH JULY 2018 TO 8TH AUG 2018 (1 MONTH)

Respected Sir,

I would like to bring it to your kind notice that I, **Pragya Pandey (1DA15EC104)**, have been selected to pursue a 1 month internship with Wipro Ltd. from **9th July 2018** to **8th August 2018.**

I kindly request you to permit me for the same and oblige.

Thanking you
Yours Faithfully

Pragya

Pragya Pandey
(1DA15EC104)

forwarded to HoD
Please consider her request during vacation.
25/6/18

8/2816

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)

BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr AIT/ECE/318 Date : 26.06.2018

To,

The Human Resource manager,
Thales India Pvt Ltd,
Richmond Road,
Richmond Town,
Bangalore-560025

Respected Sir/Madam,

Subject: Internship of BE student of Electronics and Communication Department

Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bangalore. It is an autonomous institution affiliated to Visveswaraya Technological University(VTU), Belagavi. The institute is aided by Government of Karnataka approved by All India Council of Technical Education(AICTE) New Delhi.

In reference to the above context Ms C.M.Bhargavi bearing USN:1DA15EC028 is a Bonafidestudent of Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd year examination in June 2018 and she offers herself to be a candidate for "internship training". She may be extended all facilities for internship training in your organization on the allotted days. (July 2018)

The candidate will be governed by the rules and regulations of your department andDr. AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the said period of training. All the expenses with regard to travel and incidentals will be borne by the individual concerned. Upon completion of training a report should be forwarded to us.

26/6/18

Signature of HOD

Signature Principal

Dr. Ambedkar Institute of Technol

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)

BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. ~~33~~ Dr.AM/ECE/339 Date : 02/07/2018

From

The Principal
DR.AMBEDKAR INSTITUTE OF TECHNOLOGY
BDA Outer Ring Road, Mallathally
Bengaluru-560056

To

The Manager
Bharat Heavy Electricals Limited,
Cnr Rao Circle, IIse Post, Malleswaram,
Bangalore-560003.

Subject: Internship Project at BHEL from 2nd July 2018 to.2nd August 2018.

Dear Sir,

DR.AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bengaluru. It is an autonomous Institution affiliated to Visvesvaraya Technological University (VTU), Belagavi.

The institute is Aided by the Government of Karnataka, Approved by All India Council for Technical Education (AICTE), New Delhi.

This is to certify that Bharath.K , USN-1DA16EC144 is a bonafide student of DR. AMBEDKAR INSTITUTE OF TECHNOLOGY, affiliated to Visvesvaraya Technological University (VTU), Belagavi.

In reference to the above context, we confirm that Bharath.K, bearing USN-1DA16EC144 has been identified to undergo the 1 month Internship Project on their own interest at Bharat Heavy Electricals Limited (BHEL) from 2nd July 2018 to 2nd August 2018.

The candidate will be governed by the rules and regulations of your department and DR AMBEDKAR INSTITUTE OF TECHNOLOGY and shall hold responsibility of safety during the valid period of Internship Project. All the costs with regard to travel and incidentals will be borne by the individual concerned. Upon completion of Internship a report should be forwarded to us.

02/7/18
Signature Of HOD

Signature of Principal

Dr Ambedkar Institute of Technology

Bangalore-560056

Dr. Ambedkar Institute of Technology

(Aided by Government of Karnataka)
(Affiliated to Visvesvaraya Technological University)
Near Jnana Bharathi Campus, BDA Outer Ring Road, Bangalore - 560 056.

Ref. No. .....

Date .....

To,

The General Manager

Bharat Electronics Limited

Bangalore

Respected Sir/Madam,

Subject: Internship for BE student of Electronics and Communication Department

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian Technical Institute located in Bangalore. It is an autonomous institution affiliated to Visvesvaraya Technological University (VTU), Belagavi. The institute is aided by Government of Karnataka and approved by All India Council of Technical Education (AICTE), New Delhi.

In reference to the above context, Ms. BHUMIKA S bearing USN: 1DA15EC026 is a bonafide student of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd year BE examination in June 2018 and she offers herself to be a candidate for 'internship training'. She may be extended all the facilities for internship training in your organisation in the month of July 2018.

The candidate will be governed by the rules and regulations of your department and Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the said period of training. All the expenses with regard to travel and incidentals will be borne by the individual concerned. Upon completion of training, a report shall be forwarded to us.

Thanks and Regards,

21/6/18

(Dr. Jayaramaiah G V)

Head of Department, ECE

Dr. Ambedkar Institute of Technology

(Dr. C Nanjundaswamy)

PRINCIPAL

Dr. Ambedkar Institute of Technology

Principal

Bangalore - 560 056.

Dr. Ambedkar Institute of Technology

Dr. Ambedkar Institute of Technology
(Aided by Government of Karnataka)
(Affiliated to Visvesvaraya Technological University)
Near Jnana Bharathi Campus, BDA Outer Ring Road, Bangalore - 560 056.

Ref. No. DDAIT/ECE/281 Date: 21.06.2018

To,

The General Manager HR,
Bharath Electronics Limited,
. Bengaluru- 560013

Respected Sir/Madam,

Subject: Internship for BE student of Electronics and Communication Department

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian Technical Institute located in Bangalore. It is an autonomous institution affiliated to Visveswaraya Technological University (VTU), Belagavi. The institute is aided by Government of Karnataka approved by All India Council of Technical Education (AICTE) New Delhi.

In reference to the above context Mr Bhargava U G bearing USN: 1DA15EC024 is a Bonafide student of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd year BE examinations in June 2018 and he offers himself to be a candidate for "internship training". He may be extended all the facilities for internship training in your organisation in the month of July 2018.

The candidate will be governed by the rules and regulations of your department and Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the said period of training. All the expenses with regard to travel and incidentals will be borne by the individual concerned. Upon completion of training, a report shall be forwarded to us.

21/6/2018

Signature of the HOD

Signature of Principal

Principal
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

Dr. Ambedkar Institute of Technology

(Aided by Government of Karnataka)
(Affiliated to Visvesvaraya Technological University)
Near Jnana Bharathi Campus, BDA Outer Ring Road, Bangalore - 560 056.

Ref No Dr AIT/ECE/280 Date 21/06/2018

To.

The General Manager HR,
Bharath Electronics Limited,
Bengaluru- 560013

Respected Sir/Madam,

Subject: Internship for BE student of Electronics and Communication Department

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian Technical Institute located in Bangalore. It is an autonomous institution affiliated to Visveswaraya Technological University (VTU), Belagavi. The institute is aided by Government of Karnataka approved by All India Council of Technical Education (AICTE) New Delhi.

In reference to the above context Ms Anupama A V bearing USN: 1DA16EC403 is a Bonafide student of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd year BE examinations in June 2018 and she offers herself to be a candidate for "internship training". She may be extended all the facilities for internship training in your organisation in the month of July 2018.

The candidate will be governed by the rules and regulations of your department and Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the said period of training. All the expenses with regard to travel and incidentals will be borne by the individual concerned. Upon completion of training, a report shall be forwarded to us.

21/6/18

Signature of the HOD

Signature of Principal

Principal
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

Dr. Ambedkar Institute of Technology

(Aided by Government of Karnataka)
(Affiliated to Visvesvaraya Technological University)
Near Jnana Bharathi Campus, BDA Outer Ring Road, Bangalore - 560 056.

Ref. No. Dr. AIT/ECE/267

Date 15.06.2018

From

The Principal
Dr.AMBEDKAR INSTITUTE OF TECNOLOGY
BDA Outer Ring Road, Mallathally,
Bengaluru 560056

To

The Manager
Bharat Heavy Electricals Limited,
Mysore Road,
Muthachari Industrial estate,
Deepajali Nagar,
Bengaluru 560039,
Karnataka.

Subject: Internship for Engineering students of Electronics and Communication.

Dear Sir/Madam,

Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bengaluru. It is an autonomous institution affiliated to Visvesvaraya Technological University (VTU) Belgavi. The Institute is aided by the Government of Karnataka, approved by All India Council for Technical Education (AICTE) New Delhi.

In reference to the above context Ms. Mahalakshmi S bearing USN: 1DA15EC079, is bonafide students of Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd Year examination in June 2018 and they offer themselves to be candidates for the "Internship". They may be extended all facilities for Internship in your organization for duration of 30-45days(June 18,2018 to July 31,2018).

The candidates will be governed by the rules and regulations of your department and Dr.AMBEDKAR INSTITUTE OF TECNOLOGY and responsibility of safety during the said period of training. All the cost with regard to travel and incidentals will be borne by the individual concerned .Upon completion of Internship, a report should be forwarded to us.

15/6/18

Signature of HOD

Signature of PRINCIPAL
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

Ph. : 23218534 / 23211504 / 05 / 06, 23211232 Fax : 080-23217789 Email : principal@dr-ait.org Website : www.dr-ait.org

Ref. No. Dr AIT/ECE/252

Date 21.06.2018

From,
The Principal
Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY
BDA Outer ring road, Mallathahalli,
Bengaluru-560056

To,
The Manager
BHEL Electro porcelains Division
Prof. CNR Circle
Malleshwaram, Bangalore-560012

Subject: Internship for BE students of Electronics and Communication Dept.

Dear Sir/Madam,

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian Technical Institute located in Bangalore. It is an autonomous institution affiliated to Visveswaraya Technological University (VTU) Belgavi. The Institute is aided by the Government of Karnataka approved by All India Council of Technical Education (AICTE) New Delhi.

In reference to the above context Ms Akshatha.N bearing USN: 1DA15EC007 is a bonafide student of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd year examination in June 2018 and she offers herself to be a candidate for the "Internship Training". She may be extended all facilities for internship training in your organisation in the month of July 2018.

The candidate will be governed by the rules and regulations of your department and Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the said period of training. All the cost with regard to travel and incidentals will be borne by the individual concerned. Upon completion of training a report should be forwarded to us.

21/6/18

Signature of HOD

Signature of Principal

Principal
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

Technological University)
Campus, BDA Outer Ring Road, Bangalore - 560 056.

No. Dr.AIT/ECE/268

Date 15.06.2018

From

The Principal
Dr.AMBEDKAR INSTITUTE OF TECNOLOGY
BDA Outer Ring Road, Mallathally,
Bengaluru 560056

To

The Human Resource Manager,
Helicopter Division,Hindustan Aerounautics Ltd.,
Vimanapura, Bengaluru-17,
Karnataka.

Subject: Internship for Engineering students of Electronics and Communication.

Dear Sir/Madam,

Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bengaluru. It is an autonomous institution affiliated to Visvesvaraya Technological University (VTU) Belgavi. The Institute is aided by the Government of Karnataka, approved by All India Council for Technical Education (AICTE) New Delhi.

In reference to the above context Ms. HANAMANTHA RAMANNA KARIKAL bearing USN: 1DA15EC046, is bonafide students of Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd Year examination in June 2018 and they offer themselves to be candidates for the "Internship". They may be extended all facilities for Internship in your organization for duration of 15 days(July 1,2018 to July 20,2018).

The candidates will be governed by the rules and regulations of your department and Dr.AMBEDKAR INSTITUTE OF TECNOLOGY and responsibility of safety during the said period of training. All the cost with regard to travel and incidentals will be borne by the individual concerned .Upon completion of Internship, a report should be forwarded to us.

15/6/18

Signature of HOD

Signature of PRINCIPAL
Principal
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)

BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr AIT/ECE/255 Date : 13/06/2018

To

Senior Deputy General Manager,
Human Resource,
Electro porcelains Division, Bharat Heavy Electricals Ltd.,
Malleshwaram, Bengaluru-560012,
Karnataka.

13th June 2018

Dear Sir/Madam,

Subject: Internship for Engineering student of Electronics and Communication.

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian Technical Institute located in Bengaluru. It is an Autonomous Institution affiliated to Visvesvaraya Technological University (VTU) Belgavi. The Institute is aided by the Government of Karnataka, approved by All India Council for Technical Education (AICTE) New Delhi.

In reference to the above context Mr. Harsha R bearing USN: 1DA15EC050 is bonafide student of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd Year examination in June 2018 and he offer himselves to be candidate for the "Internship". He may be extended all facilities for Internship in your organization for duration of 30 days (July 2018).

The candidate will be governed by the rules and regulations of your department and Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the said period of training. All the cost with regard to travel and incidentals will be borne by the individual concerned. Upon completion of Internship, a report should be forwarded to us.

13/6/18

Signature of HOD

Signature of PRINCIPAL

Principal
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)

BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr. AIT/ECE/251 Date : 13.06.2018

To

The Manager

Bharat Earth Movers Limited

Thippsandra,Bangaluru 560075

Subject: Internship for B.E in Electronics and Communication Engineering students

Dear Sir/Madam,

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bangalore. It is an autonomous institution affiliated to Visvesvaraya Technological University (VTU) Belgavi. The Institute is aided by the Government of Karnataka,approved by All India Council for technological Education (AICTE) New Delhi.

In reference to the above context Ms KUSUMA R bearing USN-1DA15EC073, Ms MADHURYA R bearing USN-1DA15EC077, Ms POOJA N bearing USN-1DA15EC102 are Bonafide students of Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 6th semester BE(ECE) and will be completing 6th semester examination in June 2018 and they offer themselves to be candidates for the "Internship Training". They may be extended all facilities for Internship training in your organization on the allotted days i.e from June 2018 to July 2018.

The candidates will be governed by the rules and regulations of your department and Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the said period of training. All the cost with regard to travel and incidentals will be borne by the individual concerned .Upon completion of training , a report should be forwarded to us.

13/6/18

Signature of HOD

Signature of PRINCIPAL

Principal
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)
BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr AIT/ECE/261

Date : 14.06.2018

. From

The principal
Dr AMBEDKAR INSTITUTE OF TECNOLOGY
BDA outer ring road, Mallathally,
Bengaluru- 560056

To

The Human Resource manager
Bharat Electronics Limited,
Jalahalli post,Bengalure-560013,

Subject: Internship for Engineering students of Electronics and Communication .

Respected sir/madam,

Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY is in an Indian technical institute located in Bengaluru .it is an autonomous institution affiliated to Visvesvaraya Technological University (VTU) Belagavi. The institute is aided by the government of Karnataka ,Approved by all India council for technical education (AICTE) New Delhi.

In reference to the above context Ms.J POOJA bearing USN:1DA17EC048 is bonafide students of Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 1 st year BE(ECE) and will be completing 1st year examination in june 2018 and they offer themselves to be candidates for duration of 30 days.

The candidate will be governed by the rules and regulation of your department and Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the said period of training .all the cost with regard to travel and incidentals will be borne by the individual concerned. upon completion of internship ,a report should be forwarded to us.

14/6/18

Signature of HOD

Signature of principal
PRINCIPAL
Dr. Ambedkar Institute of Technology
Bengaluru-560 056

Dr. Ambedkar Institute of Technology

(Aided by Government of Karnataka)
(Affiliated to Visvesvaraya Technological University)
Near Jnana Bharathi Campus, BDA Outer Ring Road, Bangalore - 560 056.

Ref. No. Dr. AIT/ECE/283 Date 21.06.2018

From,
The Principal
Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY
BDA Outer ring road, Mallathahalli,
Bengaluru-560056

To,
The Manager
BHEL Electro porcelains Division
Prof. CNR Circle
Malleshwaram, Bangalore-560012

Subject: Internship for BE students of Electronics and Communication Dept.

Dear Sir/Madam,

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian Technical Institute located in Bangalore. It is an autonomous institution affiliated to Visveswaraya Technological University (VTU) Belgavi. The Institute is aided by the Government of Karnataka approved by All India Council of Technical Education (AICTE) New Delhi.

In reference to the above context Ms Anusha.A bearing USN: 1DA15EC015 is a bonafide student of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd year examination in June 2018 and she offers herself to be a candidate for the "Internship Training". She may be extended all facilities for internship training in your organisation in the month of July 2018.

The candidate will be governed by the rules and regulations of your department and Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY and responsibility of safety during the said period of training. All the cost with regard to travel and incidentals will be borne by the individual concerned. Upon completion of training a report should be forwarded to us.

21/6/18

Signature of HOD

Signature of Principal
Principal
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

Affiliated to Visvesvaraya Technological University, Belgaum
BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr. AIT/ECE/252

Date : 13.06.2018

To

The Director,
National Aerospace Laboratories,
Old Airport Road, Kodihalli,
Bengaluru 560017,
Karnataka.

Subject: Internship for Engineering student of Electronics and Communication.

Dear Sir/Madam,

Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bengaluru. It is an autonomous institution affiliated to Visvesvaraya Technological University (VTU) Belgavi. The Institute is aided by the Government of Karnataka, approved by All India Council for Technical Education (AICTE) New Delhi.

In reference to the above context Mr. Chethan M S bearing USN: 1DA15EC036 is bonafide student of Dr.AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd Year examination in June 2018 and he offer himselves to be candidate for the "Internship". He may be extended all facilities for Internship in your organization for duration of 6 weeks.

The candidate will be governed by the rules and regulations of your department and Dr.AMBEDKAR INSTITUTE OF TECNOLOGY and responsibility of safety during the said period of training. All the cost with regard to travel and incidentals will be borne by the individual concerned .Upon completion of Internship, a report should be forwarded to us.

13/6/18

Signature of HOD

Signature of PRINCIPAL

PRINCIPAL
Dr. Ambedkar Institute of Technology
Bangalore - 560 056.

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)
BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr.AIT/ECE/249 Date : 11.06.2018

From

The Principal
Dr. AMBEDKAR INSTITUTE OF TECNOLOGY
BDA Outer Ring Road, Mallathally,
Bengaluru 560056

To

ASEA Brown Boveri (ABB),
Plot No. 5 & 6, 2nd Stage,
Peenya Industrial Area, Phase IV
Peenya, Bangalore, Karnataka 560058

Subject: Internship for B.E. in Electronics and Communication Engineering students.

Dear Sir/Madam,

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bengaluru. It is an autonomous institution affiliated to Visvesvaraya Technological University (VTU) Belgavi. The Institute is aided by the Government of Karnataka, approved by All India Council for Technical Education (AICTE) New Delhi.

In reference to the above context Mr. PRANAV M bearing USN: 1DA15EC106, Mr. PRITHVI RAJ MANNUR bearing USN: 1DA15EC112, Mr. PRAVEEN C bearing USN: 1DA115EC109 and Mr. KEMPARAJU N bearing USN: 1DA15EC067 are bonafide students of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd Year examination in June 2018 and they offer themselves to be candidates for "INTERNSHIP". They may be extended all facilities for Internship in your organization for the duration of 15 or 30 days. (June 15, 2018 to July 10, 2018)

The candidates will be governed by the rules and regulations of your department and Dr. AMBEDKAR INSTITUTE OF TECNOLOGY and responsibility of safety during the said period of internship. All the cost with regard to travel and incidentals will be borne by the individuals concerned . Upon completion of internship, a report should be forwarded to us.

11/6/18

Signature of HOD

Signature of PRINCIPAL
Principal
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

218534, 23211232, 23211505 / 06 / 07. Fax : 080-23217789. E-mail : principal@dr-ait.org. Website : www.dr-ait.

Panchajanya Vidya Peetha Welfare Trust (Regd)

Dr. Ambedkar Institute of Technology

(An Autonomous Institution, Aided by Government of Karnataka
Affiliated to Visvesvaraya Technological University, Belgum & Approved by AICTE New Delhi)

BDA Outer Ring Road, Near Jnana Bharathi Campus, Mallathally, Bengaluru - 560 056

Ref. No. Dr AIT/ECE/248 Date : 11.06.2018

From

The Principal
Dr. AMBEDKAR INSTITUTE OF TECNOLOGY
BDA Outer Ring Road, Mallathally,
Bengaluru 560056

To

Bharat Electronics Limited (BEL),
Vidyranyapura Road, Jalahalli,
Bengaluru, Karnataka 560013

Subject: Internship for B.E. in Electronics and Communication Engineering students.

Dear Sir/Madam,

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY is an Indian technical institute located in Bengaluru. It is an autonomous institution affiliated to Visvesvaraya Technological University (VTU) Belgavi. The Institute is aided by the Government of Karnataka, approved by All India Council for Technical Education (AICTE) New Delhi.

In reference to the above context Ms. PARINEETHA N S bearing USN: 1DA15EC100, Mr. KISHORE KUMAR G bearing USN: 1DA15EC070 and Ms. PRATHIKSHA S J bearing USN: 1DA16EC424 are bonafide students of Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY pursuing 3rd year BE (ECE) and will be completing 3rd Year examination in June 2018 and they offer themselves to be candidates for "INTERNSHIP". They may be extended all facilities for Internship in your organization for the duration of 15 or 30 days. upto July 31, 2018

The candidates will be governed by the rules and regulations of your department and Dr. AMBEDKAR INSTITUTE OF TECNOLOGY and responsibility of safety during the said period of internship. All the cost with regard to travel and incidentals will be borne by the individuals concerned .Upon completion of internship, a report should be forwarded to us.

11/6/18

Signature of HOD

Signature of PRINCIPAL

PRINCIPAL
Dr. Ambedkar Institute of Technology
Bangalore - 560 056

Ph : 23218534, 23211232, 23211505 / 06 / 07, Fax : 080-23217789, E-mail : principal@dr-ait.org. Website : www.dr-ait.org

From,

Chinmaya G (USN: 1DA15EC037)

7th Semester, B. E., Department of ECE,

Dr. Ambedkar Institute of Technology,

Bengaluru – 560056

Through,

Mentor, Dept of ECE, Dr. AIT

Through,

The HOD, Dept of ECE, Dr. AIT

To,

The Principal,

Dr. AIT, Bengaluru – 560056

04th July, 2018

Respected Sir,

Subject: Request for provision of letter-head for internship at KPTCL

I, Chinmaya G (USN: 1DA15EC037) of 7th Semester, B. E. in ECE, am interested in doing an internship at the Supervisory Control and Data Acquisition (SCADA) section of Karnataka Power Transmission Corporation Limited (KPTCL) in the month of July 2018. As per the above-mentioned subject, we request you to kindly consider our request and provide the letter-head.

Thank you,

Yours Sincerely,

Chinmaya G (1DA15EC037)

Enclosed: Letter from parent

5/7/18

w/cs. to HOD.
Respected sir,
He is a student under my mentorship, he is interested to do internship in KPTCL. Sir, I kindly request you please give a permission to do internship & do needful to him.

05/07/18
(Nagavathna HS)

To
Human Resource Manager
BESCOM (KPTCL)
Rajajinagar

14th June2018

Sir/Madam,

SUB: Permission to carryout internship at your organization.

This is to certify that **TEJASWINI.R (USN 1DA15EC160)** student of **Dr. Ambedkar Institute of Technology,** studying **B.E in Electronics and Communication Engineering,** would like to apply for internship under BESCOM(KPTCL) for a period of **One month.** It gives immense opportunity to acquire knowledge and help the student gain hands-on experience.

Further, it is stated that the student wish to do internship in BESCOM (KPTCL) with all his interest. We would be grateful for considering the case for internship.

Thanks and Regards,

14/6/18

(Dr. Jayaramaiah G V)
Head of Department, ECE
Dr. Ambedkar Institute of Technology

(Dr. C. Nanjundaswamy)
Principal,
Dr. Ambedkar Institute of Technology

To,
HOD
The student's parent permitted her for internship and had taken responsible for any damage happen to the company or to the Institution by her. So, I kindly request her to permit to do internship.

[Mentor]
14/6/18

ಕರ್ನಾಟಕ ಸರ್ಕಾರ

ಕಾಲೇಜು ಮತ್ತು ತಾಂತ್ರಿಕ ಶಿಕ್ಷಣ ಇಲಾಖೆ

Ph: 08230-200070

Email: pplgeckrpet2018@gmail.com

ಪತ್ರ ಸಂಖ್ಯೆ: ಸ.ಇಂ.ಕಾ.ಕೆ/04/ಸಿಬ್ಬಂದಿ/2021-22

ಪ್ರಾಂಶುಪಾಲರ ಕಾರ್ಯಾಲಯ

ಸರ್ಕಾರಿ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜು,

ಕೆ.ಆರ್.ಪೇಟೆ-571 426

ದಿನಾಂಕ: 16/02/2022

: ಹಾಜರಾತಿ ಪ್ರಮಾಣ ಪತ್ರ :

ಡಾ. ಮಹಲಿಂಗ ಪಿ ಮನ್ನಿ, ಪ್ರಾಧ್ಯಾಪಕರು, ಇ & ಸಿ ಇಂಜಿನಿಯರಿಂಗ್ ವಿಭಾಗ ಡಾ ಅಂಬೇಡ್ಕರ್ ಇನ್ಸ್ಟಿಟ್ಯೂಟ್ ಆಫ್ ಟೆಕ್ನಾಲಜಿ, ಬೆಂಗಳೂರು ಇವರು ಈ ಸಂಸ್ಥೆಯಲ್ಲಿ ದಿನಾಂಕ: 16/02/2022 ರಂದು Screening cum Evaluation Committee ಯಲ್ಲಿ ವಿಷಯ ತಜ್ಞರಾಗಿ ಕಾರ್ಯನಿರ್ವಹಿಸಲು ಸಭೆಯಲ್ಲಿ ಹಾಜರಿರುತ್ತಾರೆ ಎಂದು ಪ್ರಮಾಣೀಕರಿಸಲಾಗಿದೆ.

ಪ್ರಾಂಶುಪಾಲರು 16.02.2022

ಸರ್ಕಾರಿ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜು

ಕೆ.ಆರ್. ಪೇಟೆ - 571 426

ಇವರಿಗೆ,

ಡಾ. ಮಹಲಿಂಗ ಪಿ ಮನ್ನಿ

ಪ್ರಾಧ್ಯಾಪಕರು, ಇ & ಸಿ ಇಂಜಿನಿಯರಿಂಗ್ ವಿಭಾಗ

ಡಾ ಅಂಬೇಡ್ಕರ್ ಇನ್ಸ್ಟಿಟ್ಯೂಟ್ ಆಫ್ ಟೆಕ್ನಾಲಜಿ, ಬೆಂಗಳೂರು

ಕರ್ನಾಟಕ ಸರ್ಕಾರ

ಕಾಲೇಜು ಮತ್ತು ತಾಂತ್ರಿಕ ಶಿಕ್ಷಣ ಇಲಾಖೆ

Ph:08230-200070
Email:pplgeckrpet2018@gmail.com

ಪತ್ರ ಸಂಖ್ಯೆ:ಸ.ಇಂ.ಕಾ.ಕೆ/ಶೈಕ್ಷಣಿಕ/2021–22

ಪ್ರಾಂಶುಪಾಲರ ಕಾರ್ಯಾಲಯ
ಸರ್ಕಾರಿ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜು
ಕೆ.ಆರ್.ಪೇಟೆ–571 426

ದಿನಾಂಕ: 15–02–2022.

ಸುತ್ತೋಲೆ

ವಿಷಯ: E & C Engineering ವಿಷಯದ Screening Cum Evaluation Committee ರಚಿಸುವ ಕುರಿತು

ಉಲ್ಲೇಖ: ಆಯುಕ್ತರು, ಕಾಲೇಜು ಮತ್ತು ತಾಂತ್ರಿಕ ಶಿಕ್ಷಣ ಇಲಾಖೆ, ಬೆಂಗಳೂರು ಇವರ ಕಛೇರಿ ಪತ್ರ ಸಂಖ್ಯೆ: ADMIOEST/10/2021-JD-DEPT, ದಿನಾಂಕ:02/02/2022

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ಮೇಲ್ಕಂಡ ವಿಷಯ ಮತ್ತು ಉಲ್ಲೇಖಕ್ಕೆ ಸಂಬಂಧಿಸಿದಂತೆ, ನಮ್ಮ ಸಂಸ್ಥೆಯ E & C Engineering ವಿಭಾಗದಲ್ಲಿರುವ ಸಹಾಯಕ ಪ್ರಾಧ್ಯಾಪಕರು ವೃಂದ–ಎ ಮತ್ತು ಬಿ ಇವರುಗಳಿಗೆ API ಆಧಾರಿತ (CAS) ವೃತ್ತಿಪದೋನ್ನತಿ ನೀಡುವುದರ ಸಲುವಾಗಿ Screening Cum Evaluation Committee ಯನ್ನು ಈ ಕೆಳಕಂಡಂತೆ ರಚಿಸಲಾಗಿದೆ. ಕೆಳಕಂಡ ಸಮಿತಿಯಲ್ಲಿನ ಸರ್ವಸದಸ್ಯರು ದಿನಾಂಕ:16/02/2022 ರ ಬುಧವಾರ ಪೂರ್ವಾಹ್ನ 10.00 ಗಂಟೆಗೆ ಪ್ರಾಂಶುಪಾಲರ ಕೊಠಡಿಯಲ್ಲಿ ಆಯೋಜಿಸಿರುವ ಸಭೆಯಲ್ಲಿ ಹಾಜರಿರಲು ಕೋರಿದೆ.

ಕ್ರ.ಸಂ	ಸಮಿತಿ	ಹೆಸರು ಮತ್ತು ಪದನಾಮ
1	ಅಧ್ಯಕ್ಷರು	ಡಾ ಕೆ.ಆರ್.ದಿನೇಶ್ ಪ್ರಾಂಶುಪಾಲರು ಸರ್ಕಾರಿ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜು, ಕೆ.ಆರ್.ಪೇಟೆ
2	ಸದಸ್ಯ ಕಾರ್ಯದರ್ಶಿ	ಡಾ ಸತೀಶ ಎನ್ ಎಸ್ ಪ್ರಾಧ್ಯಾಪಕರು & ಮುಖ್ಯಸ್ಥರು ಸಿವಿಲ್ ಇಂಜಿನಿಯರಿಂಗ್ ವಿಭಾಗ ಸರ್ಕಾರಿ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜು, ಕೆ.ಆರ್.ಪೇಟೆ
3	ಸದಸ್ಯರು/ವಿಷಯ ತಜ್ಞರು	ಡಾ ಕೆ ಬಿ ರಾಜ ಪ್ರಾಧ್ಯಾಪಕರು &ಮುಖ್ಯಸ್ಥರು, ಇ & ಸಿ ಇಂಜಿನಿಯರಿಂಗ್ ವಿಭಾಗ, ಯು ವಿ ಸಿ ಇ, ಕೆ.ಆರ್.ಸರ್ಕಲ್, ಬೆಂಗಳೂರು–560 001.
4	ಸದಸ್ಯರು/ವಿಷಯ ತಜ್ಞರು	ಡಾ. ಮಹಲಿಂಗ ವಿ ಮನ್ನಿ ಪ್ರಾಧ್ಯಾಪಕರು, ಇ & ಸಿ ಇಂಜಿನಿಯರಿಂಗ್ ವಿಭಾಗ ಡಾ ಅಂಬೇಡ್ಕರ್ ಇನ್ಸ್ಟಿಟ್ಯೂಟ್ ಆಫ್ ಟೆಕ್ನಾಲಜಿ, ಬೆಂಗಳೂರು–560 056
5	ಸದಸ್ಯರು	ಮಂಜುನಾಥ್ ಉಪಾಧ್ಯ ಪಿ ಎಸ್ ರಿಜಿಸ್ಟ್ರಾರ್, ಸರ್ಕಾರಿ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜು, ಕೆ.ಆರ್.ಪೇಟೆ

ಧನ್ಯವಾದಗಳೊಂದಿಗೆ,

ತಮ್ಮ ವಿಶ್ವಾಸಿ

15.02.2022

GOVERNMENT OF KARNATAKA
Department of Technical Education

ಸಂಖ್ಯೆ: ಸಇಕಾರಾ/25/ಇಎಸ್‌ಟಿ/2021

ಪ್ರಾಚಾರ್ಯರ ಕಾರ್ಯಾಲಯ,
ಸರ್ಕಾರಿ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜು,
ರಾಮನಗರ–562159, ದಿ: 12–02–2022

:: ಹಾಜರಾತಿ ಪ್ರಮಾಣ ಪತ್ರ ::

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ಡಾ. ಮಾಹಾಲಿಂಗ ವಿ ಮಂಡಿ ಪ್ರಾಧ್ಯಾಪಕರು ಇ&ಸಿ ವಿಭಾಗ Dr. A.I.T Bangalore, ಇವರು ದಿ:12–02–2022 ರಂದು ಈ ಸಂಸ್ಥೆಯ ಸಹಾಯಕ ಪ್ರಾದ್ಯಾಪಕರು (ವೃಂದ– ಎ/ಬಿ) ಇವರುಗಳಿಗೆ API ಆಧಾರಿತ (CAS) ವೃತ್ತಿಪದೋನ್ನತಿ ನೀಡುವುದರ ಸಲುವಾಗಿ Screening cum Evaluation Committee ಯಲ್ಲಿ ವಿಷಯ ಪರಿಣಿತರಾಗಿ ಭಾಗವಹಿಸಿರುತ್ತಾರೆಂದು ಹಾಜರಾತಿ ಪ್ರಮಾಣ ಪತ್ರ ನೀಡಲಾಗಿದೆ.

ಪ್ರಾಂಶುಪಾಲರು.
Principal
Govt. Engineering College
Ramanagara - 562159

ಇವರಿಗೆ:–

ಡಾ. ಮಾಹಾಲಿಂಗ ವಿ ಮಂಡಿ ಪ್ರಾಧ್ಯಾಪಕರು ಇ&ಸಿ ವಿಭಾಗ Dr. A.I.T Bangalore ಇವರ ಮಾಹಿತಿಗಾಗಿ.

ಪ್ರತಿ:–

ಕಡತಕ್ಕೆ.

ಕರ್ನಾಟಕ ಸರ್ಕಾರ
ಕಾಲೇಜು ಮತ್ತು ತಾಂತ್ರಿಕ ಶಿಕ್ಷಣ ಇಲಾಖೆ
ಸರ್ಕಾರಿ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜು, ಬೇಡರಪುರ, ಚಾಮರಾಜನಗರ–571313
ದೂರವಾಣಿ ಸಂಖ್ಯೆ: 08226–230055
ಫ್ಯಾಕ್ಸ್ ನಂ: 08226–230022

ಸಂಖ್ಯೆ: ಜಿಇಸಿಸಿ/ಸಿಬ್ಬಂದಿ/2021–22/6೩೮ ದಿನಾಂಕ 07–02–2022

ಹಾಜರಾತಿ ಪ್ರಮಾಣ ಪತ್ರ

ಡಾ: ಮಹಲಿಂಗ ವಿ ಮಂಡಿ, ಪ್ರಾಧ್ಯಾಪಕರು, ಇ ಅಂಡ್ ಸಿ ವಿಭಾಗ, ಡಾ: ಅಂಬೇಡ್ಕರ್ ಇನ್ಸ್ಟಿಟ್ಯೂಟ್ ಆಫ್ ಟೆಕ್ನಾಲಜಿ., ಬೆಂಗಳೂರು ಇವರು 07–02–2022 ರಂದು ನಮ್ಮ ಕಾಲೇಜಿನಲ್ಲಿ ನಡೆದ "Screening Cum Evaluation" ಸಮಿತಿಯ ಇ ಅಂಡ್ ಸಿ ವಿಭಾಗದ ವಿಷಯ ತಜ್ಞರಾಗಿ ಸಭೆಯಲ್ಲಿ ಪಾಲ್ಗೊಂಡಿರುತ್ತಾರೆ. ಎಂದು ಈ ಮೂಲಕ ದೃಢೀಕರಿಸಿದೆ.

Sincerely,
ಪ್ರಾಂಶುಪಾಲರು 07/02/2022

GOVERNMENT OF KARNATAKA
Department of Technical Education

ಸಂಖ್ಯೆ: ಸಇಕಾರಾ/25/ಇಎಸ್‌ಟಿ2021

ಪ್ರಾಚಾರ್ಯರ ಕಾರ್ಯಾಲಯ,
ಸರ್ಕಾರಿ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜು,
ರಾಮನಗರ-562159, ದಿ:05-02-2022

:: ಸೂತ್ತೋಲೆ ::

ವಿಷಯ:- ಸಂಸ್ಥೆಯಲ್ಲಿ ದಿ:12-02-2022 ರಂದು Screening cum Evaluation Committee (E&C Engginering Department) ರಚಿಸುವ ಕುರಿತು.

ಉಲ್ಲೇಖ:- ಆಯುಕ್ತರು ಕಾಲೇಜು ಮತ್ತು ತಾಂತ್ರಿಕ ಶಿಕ್ಷಣ ಇಲಾಖೆ ಬೆಂಗಳೂರು ಇವರ ಕಛೇರಿ ಪತ್ರ ಸಂಖ್ಯೆ:ADMIOEST/10/2021-JD-DEPT. ದಿ:02-02-2022.

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ಮೇಲ್ಕಂಡ ವಿಷಯ ಮತ್ತು ಉಲ್ಲೇಖಕ್ಕೆ ಸಂಬಂಧಿಸಿದಂತೆ ಈ ಸಂಸ್ಥೆಯ ಇ&ಸಿ ಇಂಜಿನಿಯರಿಂಗ್ ವಿಭಾಗದಲ್ಲಿರುವ ಸಹಾಯಕ ಪ್ರಾಧ್ಯಾಪಕರು (ವೃಂದ-ಎ/ಬಿ) ಇವರುಗಳಿಗೆ API ಆಧಾರಿತ (CAS) ವೃತ್ತಿಪದೋನ್ನತಿ ನೀಡುವುದರ ಸಲುವಾಗಿ Screening cum Evaluation Committee (E&C Engginering Department) ಯನ್ನು ಈ ಕೆಳಕಂಡಂತೆ ರಚಿಸಲಾಗಿದೆ.

ಸ್ಥಾನೀಕರಣ ಸಮಿತಿಯ ಸಭೆಯಲ್ಲಿ ಇರುವ ಅದ್ಯಕ್ಷರು/ಸದಸ್ಯರು ಹಾಗೂ ವಿಷಯ ತಜ್ಞರ ವಿವರಗಳು

1.	ಡಾ. ಜಿ. ಪುಂಡರೀಕ ಪ್ರಾಂಶುಪಾಲರು ಸರ್ಕಾರಿ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜು ರಾಮನಗರ	ಅದ್ಯಕ್ಷರು
2	ಡಾ. ಡಿ ಮಧು ಪ್ರಾಧ್ಯಾಪಕರು ಮತ್ತು ವಿಭಾಗಾಧಿಕಾರಿಗಳು ಮೆಕ್ಯಾನಿಕಲ್ ವಿಭಾಗ ಸರ್ಕಾರಿ ಇಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜು ರಾಮನಗರ	ಸಂಯೋಜಕರು/ಸದಸ್ಯರು
3	ಡಾ. ವಸಂತ್ ಬಿ. ಪ್ರಾಧ್ಯಾಪಕರು ಮತ್ತು ವಿಭಾಗಾಧಿಕಾರಿಗಳು ಕಂಪ್ಯೂಟರ್ ಸೈನ್ಸ್ ವಿಭಾಗ	ಸದಸ್ಯ ಕಾರ್ಯದರ್ಶಿಗಳು

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
("ಜ್ಞಾನ ಸಂಗಮ" ಬೆಳಗಾವಿ, ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ)
'ಜ್ಞಾನ ಸಂಗಮ', ಬೆಳಗಾವಿ - ೫೯೦ ೦೧೮ ಕರ್ನಾಟಕ ರಾಜ್ಯ, ಭಾರತ
Visvesvaraya Technological University
(State University of Government of Karnataka Established as per the VTU Act, 1994)
"Jnana Sangama", Belagavi-590 018, Karnataka State, India

Prof. A. S. Deshpande B.E., M.Tech., Ph.D.
REGISTRAR

Phone : (0831) 2498100
Fax : (0831) 2405467

Ref: VTU/Aca/2021-22/A5/ 2553

Date: 04 SEP 2021

To,
Dr. Mahalinga Mandi,
Professor, E& C Department,
Dr. Ambedkar Institute of Technology,
BDA Outer ring Road,
Near Jnana Bharathi Campus,
Mallathally,
BENGALURU -560056.
Mobile : 9448800637

Sir,

Sub : Nomination to the Selection Committee panel for recruitment of Faculty positions –reg.

Ref : 1) Principal, BMS Institute of Technology and Management, Bengaluru, dtd. 01/09/2021.
2) The Hon'ble Vice-Chancellor's approval dated : 13/09/2021.

With reference to the above subject, I am pleased to nominate you as University Nominee to the Selection Committee panel for faculty selection interview at BMS Institute of Technology and Management, Bengaluru-560 064.

You are requested to accept the same and attend the meeting of the faculty Selection Committee of BMS Institute of Technology and Management, Bengaluru as " **University Nominee**" for the faculty selection process as and when requested by the principal of the college and ensure that the prescribed norms of AICTE and VTU with regard to qualification and experience of the candidates are complied with.

Thanking you,

Yours faithfully,

14/9/2021

REGISTRAR

Copy to :

1. The Principal, BMS Institute of Technology and Management, Bengaluru -560 064 with information to send the meeting notice to **Dr. Mahalinga Mandi**. Please note that, the TA/DA /Hospitality of VTU Nominee for attending the meeting has to be borne by your Society/ Institution.
2. Office copy.

3Q SUTANTRA | NAWIN GURUKULA

Ref No : 3QNGAL01
Date : 13-10-2020

To,
Dr. Tanuja

Sub: Appointment Letter – Academic programs

Dear Madam, with reference to our discussion, we are please to consider your interest & appoint you as our **"Advisor for Academic Programs"** for the duration of One year w.e.f 14-10-2020.

This is a Mutual beneficiary commitment activity between you & the company for the welfare of students of Technical graduates to enhance the skill level, hence there will be no financial part is involved.

Wishing you good luck and a successful career with us,

Sincerely,

Director
3Q SUTANTRA LLP

ಬೃಹತ್ ಬೆಂಗಳೂರು ಮಹಾನಗರ ಪಾಲಿಕೆ
Bruhat Bengaluru Mahanagara Palike

BYE ELECTIONS TO LEGISLATIVE ASSEMBLY OF KARNATAKA 2020

ORDER OF APPOINTMENT OF PRESIDING AND ASSISTANT PRESIDING OFFICERS

Ref. No:-5125

In pursuance of sub section (1) and (3) of section 26 of representation of peoples act 1963(43 of 1951). I here by appoint the officer specified in the column 1 of the table below for election duty as **PRO** in Bye Elections to Legislative Assembly of Karnataka 2020.

TABLE

Name of the Presiding Officer/APRO	Designation	Office Address and Mobile No
NAGARATHNA HS	ASSISTANT PROFESSOR	DEPARTMENT OF TECHNICAL EDUCATION
Polling Duty Alloted : PRO	DR AMBEDKAR INSTITUTE OF TECHONOLOGY BANGALORE	DR AMBEDKAR INSTITUTE OF TECHNOLOGY BANGALORE 560056

KGID/EMPLOYEE ID 31001000030104 Mobile Number : 9731736388

NOTE :

1. On your appointment to election duty, under article 324(6) of the Constitution read with section 13CC of the Representation of the People Act, 1950 and section 28A of the RP Act, 1951 you are directly working under control, supervision and discipline of Election Commission of India.
2. This appointment order shall bind aforesaid appointee for attending training, mustering as well as for poll duty on the day of poll i.e., on 03-11-2020
3. The Presiding officers and Assistant Presiding Officer shall attend the first level training on the date, time, venue mentioned

Rehearsal	Date and Day	Time	Venue
1	19-10-2020 MONDAY	9.30 A.M	R N S TRUST Engineering College, Kengeri Uttarahalli main road, Channasandra, Bangalore-560098

4. **YOU ARE CAUTIONED THAT FAILURE TO REPORT FOR ELECTION TRAINING, MUSTERING AND ELECTION DUTY GIVEN ABOVE SHALL ATTRACT COGNIZABLE PENAL ACTION U/S 134 OF RP ACT 1951 AND IMMEDIATE FIR WILL BE REGISTERED AGAINST YOU AND DISCIPLINARY ACTION WILL ALSO BE INITIATED UNDER RELEVANT PROVISIONS OF SERVICE RULES**
5. You are entitled to cast your vote by Postal Ballot(PB)/Election Duty Cetificate (EDC) for which you may apply in FORM-12 /12A respectively which is enclosed with this order. For applying postal ballot please bring your EPIC card and appointment order zerox on training date. However request for PB is to be sent to the Returning Officer of the constituency where you are registered as an elector.
6. Please bring 2 passport size photographs attested by your office head for afixing on the ID card while coming for training.
7. Allotment of assembly segment, party number and constitution of the Party will be intimated lat
8. To know your part no and serial no please send a SMS as prescribed to Mob No. 9731979899. Type KAEPIC space type EPIC ID number and message to the mobile number given.
9. While coming for training, please bring your BANK PASSBOOK Xerox copy along with correct bank account number, IFSC Code and bank branch details to facilitate direct payment of remuneration to your account
10. Name of the nodal officer SHEKAR Mobile Number : 9448738758

Place : Bengaluru Urban District
Date : 15/10/2020

(N. MANJUNATHA PRASAD, I.A.S
District Election Officer
Bengaluru Urban District

Bruhat Bengaluru Mahanagara Palike

BYE ELECTIONS TO LEGISLATIVE ASSEMBLY OF KARNATAKA 2019

ORDER OF APPOINTMENT OF PRESIDING AND ASSISTANT PRESIDING OFFICERS

Ref. No:-6248

In pursuance of sub section (1) and (3) of section 26 of representation of peoples act 1963(43 of 1951), I here by appoint the officer specified in the column 1 of the table below for election duty as **APRO** in Bye Elections to Legislative Assembly of Karnataka 2019.

TABLE

Name of the Presiding Officer/APRO	Designation	Office Address and Mobile No
TANUJA PATGAR P	LECTURER	DEPARTMENT OF TECHNICAL EDUCATION
Polling Duty Alloted : APRO	E4 DR AMBEDKAR INSTITUTE OF TECHNOLOGY BANGALORE GOVT P U COLLEGE HOODI BANG 48 AS454	
KGID/EMPLOYEE ID 04003100230146		Mobile Number : 9900165763

NOTE :

1. On your appointment to election duty, under article 324(6) of the Constitution read with section 13CC of the Representation of the People Act, 1950 and section 28A of the RP Act, 1951 you are directly working under control, supervision and discipline of Election Commission of India.
2. This appointment order shall bind aforesaid appointee for attending training, mustering as well as for poll duty on the day of poll i.e., on 05-12-2019.
3. The Presiding officers and Assistant Presiding Officer shall attend the first level training on the date, time, venue mentioned

Rehearsal	Date and Day	Time	Venue
1	24-11-2019 Sunday	9.30 A.M	R V COLLAGE OF ENGINEERING RVCE POST MYSORE ROAD KENGERI BANGALORE 560059

4. **YOU ARE CAUTIONED THAT FAILURE TO REPORT FOR ELECTION TRAINING, MUSTERING AND ELECTION DUTY GIVEN ABOVE SHALL ATTRACT COGNIZABLE PENAL ACTION U/S 134 OF RP ACT 1951 AND IMMEDIATE FIR WILL BE REGISTERED AGAINST YOU AND DISCIPLINARY ACTION WILL ALSO BE INITIATED UNDER RELEVANT PROVISIONS OF SERVICE RULES.**
5. You are entitled to cast your vote by Postal Ballot(PB)/Election Duty Cetificate (EDC) for which you may apply in FORM-12 /12A respectively which is enclosed with this order. For applying postal ballot please bring your EPIC card and appointment order zerox on training date. However request for PB is to be sent to the Returning Officer of the constituency where you are registered as an elector.
6. Please bring 2 passport size photographs attested by your office head for afixing on the ID card while coming for training.
7. Allotment of assembly segment, party number and constitution of the Party will be intimated later.
8. To know your part no and serial no please send a SMS as prescribed to Mob No. 9731979899. Type KAEPIC space type EPIC ID number and message to the mobile number given.
9. While coming for training, please bring your BANK PASSBOOK Xerox copy along with correct bank account number, IFSC Code and bank branch details to facilitate direct payment of remuneration to your account
0. Name of the nodal officer SRI SRINIVASA MURTHY DV Mobile Number : 9449749248

Place : Bengaluru Urban District

Date : 19/11/2019

B.H. Anil Kumar

(B.H. Anil Kumar I.A.S)
District Election Officer
Bengaluru Urban District

ಬೃಹತ್ ಬೆಂಗಳೂರು ಮಹಾನಗರ ಪಾಲಿಕೆ
Bruhat Bengaluru Mahanagara Palike

GENERAL ELECTIONS TO THE LOK SABHA 2019

ORDER OF APPOINTMENT OF PRESIDING AND ASSISTANT PRESIDING OFFICERS

Ref. No:-131398

In pursuance of sub section (1) and (3) of section 26 of representation of peoples act 1963(43 of 1951), I here by appoint the officer specified in thecolumn 1 of the table below for election duty as **PRO** in General Elections to Lok Sabha 2019.

TABLE

Name of the Presiding Officer/APRO	Designation	Office Address and Mobile No
TANUJA PATGAR P Polling Duty Alloted : PRO	LECTURER	DEPARTMENT OF TECHNICAL EDUCATION E4 DR AMBEDKAR INSTITUTE OF TECHNOLOGY BANGALORE DR AMBEDKAR INSTITUTE OF TECHNOLOGY BDA OUTER RING ROAD NEAR JANAN BHARATHI CAMPUS MALLATHAHALLI BANGALORE 560056
KGID/EMPLOYEE ID 04038500370041		Mobile Number : 6360373101

NOTE :

1. On your appointment to election duty, under article 324(6) of the Constitution read with section 13CC of the Representation of the People Act. 1950 and section 28A of the RP Act, 1951 you are directly working under control, supervision and discipline of Election Commission of India.
2. This appointment order shall bind aforesaid appointee for attending training, mustering as well as for poll duty on the day of poll i.e., on 18-04-2019.
3. The Presiding officers and Assistant Presiding Officer shall attend the first level training on the date, time, venue mentioned

Rehearsal	Date and Day	Time	Venue
1	01-04-2019 Monday	9.30 A.M	PES COLLEGE 50 FEET ROAD BSK 1ST STAGE 2ND BLOCK BANGALORE 560050

4. **YOU ARE CAUTIONED THAT FAILURE TO REPORT FOR ELECTION TRAINING, MUSTERING AND ELECTION DUTY GIVEN ABOVE SHALL ATTRACT COGNIZABLE PENAL ACTION U/S 134 OF RP ACT 1951 AND IMMEDIATE FIR WILL BE REGISTERED AGAINST YOU AND DISCIPLINARY ACTION WILL ALSO BE INITIATED UNDER RELEVANT PROVISIONS OF SERVICE RULES**
5. You are entitled cast your vote by Postal Ballot(PB)/Election Duty Cetificate (EDC) for which you may apply in FORM-12 /12A respectively which is enclosed with this order. For applying postal ballot please bring your EPIC card and appointment order zerox on training date. However request for PB is to be sent to the Returning Officer of the constituency where you are registered as an elector.
6. Please bring 2 passport size photographs attested by your office head for afixing on the ID card while coming for training.
7. Allotment of assembly segment, party number and constitution of the Party will be intimated lat
8. To know your part no and serial no please send a SMS as prescribed to Mob No. 9731979899. Type KAEPIC space type EPIC ID number and message to the mobile number given.
9. While coming for training, please bring your BANK PASSBOOK Xerox copy along with correct bank account number, IFSC Code and bank branch details to facilitate direct payment of remuneration to your account
0. Name of the nodal D V SREENIVASA MURTHY Mobile Number : 9449749248

Place : Bengaluru Urban District
Date : 24/03/2019

(N. Manjunatha Prasad I.A.S)
District Election Officer
Bengaluru Urban District

BYE ELECTIONS TO LEGISLATIVE ASSEMBLY OF KARNATAKA 2019

ORDER OF APPOINTMENT PRESIDING / ASSISTANT PRESIDING AND POLLING OFFICERS

Pursuance of sub section (1) and (3) of section 26 of Representation of Peoples Act 1963(43 of 1951), I here by appoint the officers specified in the para (2) of the table below as Presiding / Assistant Presiding / Polling Officers for the polling station code number (polling party number) specified in the para(1) below for Legislative Assembly Constituency – 156 Mahalakshmi Assembly forming part of Bengaluru North Lok Sabha Constituency

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P.S 158
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10.3

TABLE

Polling Party Number	116		
Name of the Presiding Officer	DR P R RANGARAJU		DEPARTMENT OF PRE UNIVERSITY EDUCATION
	LECTURER		DAYANANDA PU COLLEGE K S LAYOUT BANGALORE AS004
	9845810630	5422	
	Employee ID :	04000500110004	DAYANANDA PU COLLEGE K S LAYOUT BANGALORE AS004
Name of Assistant Presiding Officer	TANUJA PATGAR P		DEPARTMENT OF TECHNICAL EDUCATION
	LECTURER		E4 DR AMBEDKAR INSTITUTE OF TECHNOLOGY BANGALORE
	6360373101	6248	
	Employee ID	04003100230146	E4 DR AMBEDKAR INSTITUTE OF TECHNOLOGY BANGALORE
Name of Polling Officers	LAKSHMI H V		DEPARTMENT OF PUBLIC INSTRUCTIONS
	ASSISTANT TEACHER		VINAYAKA HIGH SCHOOL
	9972919157	1966	
	Employee ID :	04001402130002	NO1 60FEET ROAD THOMAS BUILDING KURUBARAHALLY BANGALORE 86 .
	RAGHUKUMAR N		DEPARTMENT OF PUBLIC INSTRUCTIONS
	ASSISTANT TEACHER		TAGORE MEMORIAL HS
	9980810709	2426	
	Employee ID :	04001401160009	TAGOREMEMORIAL HIGH SCHOOL MARAPPANAPALYA YASHWANTHPUR BANGALORE
Polling Officer authorized to perform the functions of presiding officer in the latter's absence	TANUJA PATGAR P		DEPARTMENT OF TECHNICAL EDUCATION
	LECTURER		E4 DR AMBEDKAR INSTITUTE OF TECHNOLOGY BANGALORE
	6360373101	6248	
	KGID/Employee ID:	04003100230146	

Rehearsal	Date and Day	Time	Venue
2	01/12/2019 SUNDAY	9.30 A.M	KARNATAKA MARATHA WELFARE ASSOCIATION PRIMARY SCHOOL BESIDE HINDU SADARA KSHEMABIVRIDDI SANGHA WEST OF CHORD ROAD 2ND STAGE MAHALAKSHMI PURAM BANGALORE 560086

NOTE

The Poll will be taken on 05/12/2019 during the hours of 7AM to 6 PM

The Polling Personnel shall attend the 2nd Level training on the date, time and venue mentioned above.

The Polling personnel shall report at mustering venue

VIDYAVARDHAKA SANGHA SARDAR PATEL SCHOOL DHRUVADHAMA 19TH JEMAIN ROAD 1ST BLOCK RAJAJINAGAR BANGALORE 560010 on 04/12/2019 at 9.00 AM

Their attendance will be marked there. Thereafter they will be taken to alloted polling station in the assembly constituency mentioned above for performing election duty there.

You are entitled to cast your vote by Postal Ballot (PB)/Election Duty Certificate (EDC) for which you may apply in FORM-12 /FORM-12A respectively. For casting vote through PB, bring your EPIC card and a copy of the appointment order on 2nd training date. However request for PB is to be sent to the Returning Officer of the constituency where you are registered as an elector.

YOU ARE CAUTIONED THAT FAILURE TO REPORT FOR ELECTION TRANING, MUSTERING AND ELECTION DUTY SHALL ATTRACT COGINZABLE PENAL ACTION U/S 134 OF RP ACT 1951 AND IMMEDIATE FIR WILL BE REGISTERED AGAINST YOU AND ALSO DISCIPLINARY ACTION WILL BE INITIATED UNDER RELEVANT PROVISIONS OF SERVICE RULES

Nodal Officer SRI SRINIVASA MURTHY DV Mobile Number 9449749248

Place : Bengaluru Urban District

Date : 27/11/2019

(B.H. Anil Kumar I.A.S)
District Election Officer
Bengaluru Urban District

ಬೃಹತ್ ಬೆಂಗಳೂರು ಮಹಾನಗರ ಪಾಲಿಕೆ
Bruhat Bengaluru Mahanagara Palike

GENERAL ELECTIONS TO THE LOK SABHA 2019

Ref. No:-131398

ORDER OF APPOINTMENT OF PRESIDING AND ASSISTANT PRESIDING OFFICERS

In pursuance of sub section (1) and (3) of section 26 of representation of peoples act 1963(43 of 1951), I here by appoint the officer specified in thecolumn 1 of the table below for election duty as **PRO** in General Elections to Lok Sabha 2019.

TABLE

Name of the Presiding Officer/APRO	Designation	Office Address and Mobile No
TANUJA PATGAR P	LECTURER	DEPARTMENT OF TECHNICAL EDUCATION
Polling Duty Alloted : PRO	E4 DR AMBEDKAR INSTITUTE OF TECHNOLOGY BANGALORE	DR AMBEDKAR INSTITUTE OF TECHNOLOGY BDA OUTER RING ROAD NEAR JANAN BHARATHI CAMPUS MALLATHAHALLI BANGALORE 560056
KGID/EMPLOYEE ID	04038500370041	Mobile Number : 6360373101

NOTE :

1. On your appointment to election duty, under article 324(6) of the Constitution read with section 13CC of the Representation of the People Act, 1950 and section 28A of the RP Act, 1951 you are directly working under control, supervision and discipline of Election Commission of India.
2. This appointment order shall bind aforesaid appointee for attending training, mustering as well as for poll duty on the day of poll i.e., on 18-04-2019.
3. The Presiding officers and Assistant Presiding Officer shall attend the first level training on the date, time, venue mentioned

Rehearsal	Date and Day	Time	Venue
1	01-04-2019 Monday	9.30 A.M	PES COLLEGE 50 FEET ROAD BSK 1ST STAGE 2ND BLOCK BANGALORE 560050

4. **YOU ARE CAUTIONED THAT FAILURE TO REPORT FOR ELECTION TRAINING, MUSTERING AND ELECTION DUTY GIVEN ABOVE SHALL ATTRACT COGNIZABLE PENAL ACTION U/S 134 OF RP ACT 1951 AND IMMEDIATE FIR WILL BE REGISTERED AGAINST YOU AND DISCIPLINARY ACTION WILL ALSO BE INITIATED UNDER RELEVANT PROVISIONS OF SERVICE RULES**
5. You are entitled cast your vote by Postal Ballot(PB)/Election Duty Cetificate (EDC) for which you may apply in FORM-12 /12A respectively which is enclosed with this order. For applying postal ballot please bring your EPIC card and appointment order zerox on training date. However request for PB is to be sent to the Returning Officer of the constituency where you are registered as an elector.
6. Please bring 2 passport size photographs attested by your office head for afixing on the ID card while coming for training.
7. Allotment of assembly segment, party number and constitution of the Party will be intimated lat
8. To know your part no and serial no please send a SMS as prescribed to Mob No. 9731979899. Type KAEPIC space type EPIC ID number and message to the mobile number given.
9. While coming for training, please bring your BANK PASSBOOK Xerox copy along with correct bank account number, IFSC Code and bank branch details to facilitate direct payment of remuneration to your account
0. Name of the nodal D V SREENIVASA MURTHY Mobile Number : 9449749248

Place : Bengaluru Urban District

Date : 24/03/2019

(N. Manjunatha Prasad I.A.S)
District Election Officer
Bengaluru Urban District

Hindawi
Journal of Nanomaterials
Volume 2022, Article ID 6491747, 7 pages
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Research Article

Cloud Computing and Networking for SmartFarm AgriTech

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[1]*Department of ECE, Dr. Ambedkar Institute of Technology, Bengaluru-56, India*
[2]*Department of ETE, RV College of Engineering, Bengaluru, India*
[3]*Department of Chemical Engineering, School of Mechanical, Chemical and Materials Engineering, Adama Science and Technology University, Adama-1888, Ethiopia*

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Academic Editor: Samson Jerold Samuel Chelladurai

In this paper, the implementation of SmartFarm AgriTech is done using IoT and cloud computing. The current world population is 7.9 billion and supposed to reach 12 billion by 2050, and it is difficult to feed such population in the future. So, for feeding the entire population, the agriculture sector should be embedded with the latest technologies. People living in urban city will be covered with their work and day to day activities which makes it really difficult to travel the village and monitor their cultivation regularly. Without proper maintenance of farms, it is hard to get the desired results, so using the cloud computing, IOT, networking, and many other technologies, one can easily maintain and monitor the crops, weather, water, and spraying fertilizers whenever needed. This SmartFarm AgriTech System is designed using Raspberry Pi and Arduino as the main microcontrollers to control the various sensors, relay-switch, and motor. AWS and ThingSpeak are used to create server and APIs to collect and store the data through Internet or via a Local Area Network (LAN). In addition to that, a GUI (Graphical User Interface) application is also created to control and monitor the data coming from Raspberry Pi and Arduino board.

1. Introduction

Smart farming is an emerging concept that refers to managing farms using technologies like IOT, robotics, drones, and AI to increase the quantity and quality of products while optimizing the human labor required by production. The Internet of Things has provided not only a way to better measure and control growth factors, like irrigation and fertilizer; on a farm, it will change how we view agriculture in its entirely. This paper discusses what a smart farm is and how the Internet of Things will affect farming in the future. Smart farming focuses on the management of farm activities through the utilisation of data collected from multiple sources (historical, geographical, and instrumental). Being technologically advanced does not always imply that a system is intelligent. Smart systems are distinguished by their capacity to record and interpret data. Hardware (IoT) is used in smart farming to collect data and provide actionable insights to manage all farm operations, both before and after harvest. The data is well-organized, always accessible, and full of information on all aspects of finance and field operations that can be viewed from anywhere in the world.

Some of the technologies that are available for present-day farmers are as follows:

(i) Sensors: soil, water, light, humidity, and temperature management

(ii) Software: specialized software solutions that target specific farm types or use case agnostic IoT platforms

(iii) Connectivity: cellular, LoRa, etc.

Design and ASIC Implementation of Efficient 8-bit Integer Division Algorithms

pdf (https://www.annalsofrscb.ro/index.php/journal/article/view/4175/3336)

Anusha R Naganur, Dr. Ramesh S

Abstract

Many algorithms are developed for implementing division in hardware. This paper describes the efficient 8-bit integer division algorithms. The 8-bit division algorithms are intended and enforced Verilog code in activity model. Then the division algorithms are synthesized and enforced on ASIC Implementation. A division could be purposefully a slice of the arithmetic and logic unit and division is the one foremost difficult operation among all the fundamental arithmetic operations. In this paper we have designed 8-bit division algorithm for signed and unsigned numbers that performs specific division operations. When the results are analyzed, comparison of performance parameters (like speed, area, delay and power consumption) are optimized. Verilog Hardware Description Language (HDL) is used to verify the functionality of the considered algorithms and synthesized using cadence tool and the layout has beengenerated. Nc-launchhasbeenusedforsimulation,genus for the synthesized design and innovus is used for physical design. Compared to all proposed algorithms the restoring unsigned division algorithm consumes the total power of 0.8107 mW and minimum netlist of213.

How to Cite

Anusha R Naganur, Dr. Ramesh S. (2021). Design and ASIC Implementation of Efficient 8-bit Integer Division Algorithms. *Annals of the Romanian Society for Cell Biology*, 12463–12474. Retrieved from https://www.annalsofrscb.ro/index.php/journal/article/view/4175

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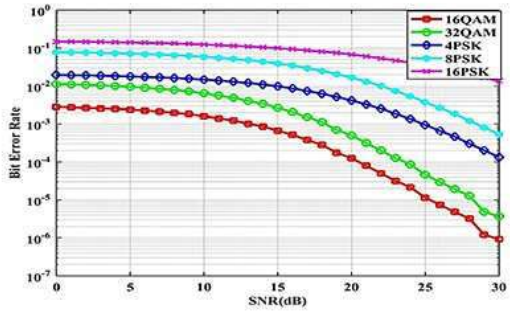
Indian Journal of Science and Technology

ARTICLE



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Year: 2020, **Volume**: 13, **Issue**: 42, **Pages**: 4374-4385

Year: 2020, Volume: 13, Issue: 42

Original Article

Performance evaluation of chaotic spreading codes in massive MIMO OFDM system

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Corresponding author:
chidu.20ait@gmail.com

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ABSTRACT

Background/Objectives: Wireless communication systems are growing towards the implementation of 5G communication systems to satisfy the demand of services in future. OFDMA has some shortcoming like one or more subcarriers of OFDM are completely affected due to the characteristic of the transmission channel. Spreading scheme has been introduced to combat the aforementioned issue. Furthermore, communication channels are affected by multipath fading which changes the amplitude of the received signal. This fading severely

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Cluster Based Routing Protocol Using Energy Centric Multi Objective Salp Swarm Algorithm for WSNs

Gundeboyina Srinivasalu[1]* **Hanumanthappa Umadevi[2]**

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[2]*Department of Electronics & Communication Engineering,*
Dr. Ambedkar Institute of Technology, Bengaluru, India
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Abstract: Wireless Sensor Network (WSN) is an immense collection of low-power, intelligent and multifunctional sensor nodes for sensing and monitoring the environmental conditions. The information collected from sensors are transmitted to the sink or Base Station (BS). The sensors in the WSN use the battery energy and the energy consumption of the nodes are considered as an important constraint in the network. In order to overcome the issue related to the energy consumption, a cluster based routing protocol is developed in the WSN. In this paper, an appropriate Cluster Head (CH) selection and route generation are obtained using the Energy Centric Multi Objective Salp Swarm Algorithm (ECMOSSA). The main objective of using ECMOSSA is to improve the network lifetime of the WSN by minimizing the node's energy consumption. The performance of the proposed ECMOSSA method is evaluated by means of alive nodes, total energy consumption, total packets received by the BS, throughput and network lifetime. Moreover, the ECMOSSA method is evaluated with one classical approach namely Low-Energy Adaptive Clustering Hierarchy (LEACH) protocol as well as this ECMOSSA is compared with Grey Wolf Optimizer (GWO)-Dual Hop Routing (DHR) method and Cat- Salp Swarm Algorithm (C-SSA) to evaluate the efficiency of ECMOSSA. The last node dies (i.e., network lifetime) of the ECMOSSA is 1704 that is high when compared to both the LEACH and GWO-DHR method.

Keywords: Cluster head selection, Energy centric multi objective salp swarm algorithm, Energy consumption, Network lifetime, Route generation, Wireless sensor network.

1. Introduction

WSN is a type of self-organizing networks that composes of numerous sensor nodes to process the sensing and communication tasks using the radio waves. The purpose of the WSN is to identify the mobile target's movement (e.g. fire spread and wildlife) or observe the conditions (e.g. humidity and temperature) [1, 2]. The sensor nodes in the WSN senses various parameters such as moisture level, temperature, light intensity, vibration, pressure and so on [3]. This WSN plays a major role in the abandoned real time applications such as Industrial monitoring, surveillance in battle field, climatic and weather monitoring, health monitoring, natural disaster prevention, traffic monitoring, environmental condition monitoring and so on [4]. Sensors in WSN have many advantages such as self-identification, time awareness, self-diagnosis and simple installation while coordinating with the remaining sensors to generate the dynamic self-organized networks. However, these sensors have different constraints such as restricted energy, memory and computational ability [5, 6].

Generally, the WSN is densely installed in the harmful places where the recharging or replacement of the battery is impossible as well as the human monitoring scheme is very risky [7]. The communication task carried out by the sensor node consumes a high amount of energy when compared to remaining tasks such as sensing and processing tasks [8]. Accordingly, the energy efficiency is considered as the main constraint because of the restricted battery capacity of the sensors [9]. In order

Survey on the Intelligibility of Dysarthric Speech

Sunitha S V[1], Shivaputra[2], S Soundeswaran[3]
Dept. of ECE[12], Dept. of Chemistry[3]
Vijaya Vittala Institute of Technology[1], Dr. Ambedkar Institute of Technology[23]-Bengaluru

***Abstract*—People with speech disorders is very difficult to communicate with others. Dysarthria is a neuro-motor disorder in which involves weak articulation due to its lack of influence over the articulatory muscles, which results in decreased intelligibility. Dysarthric patients are hard to understand sluggish and slurred speech..The paper seeks to change the Dysarthric speech in order to enhance its intelligibility. When determining the intelligibility,Vowels and consonants play a very important role. One approach is to locate a region of interest and adjust the signal during that time when it is necessary to correctly identify the region. Significant instants of time known as landmarks are observed as a preliminary phase around which changes are made. Another approach is by using a synthesis method and the typical pitch of dysarthric speech and synthesize vowels to alter the vowel formants. These synthesized vocals replace the Dysarthric speech vocal parts to form words.**

Keywords*— *Dysarthria, formants, intelligibility, landmarks, slurred speech, sluggish speech, synthesized vocals

I.INTRODUCTION

The word dysarthria[1] originates from dysarthia and arthrosis, which is complicated or imperfect to articulate. Dysarthria is due to weakness of the muscle of the Nervous system, such as brain injury, strokes, throat, tongue, etc. Disruption to the peripheral or central nervous system affects the speech production. These dysfunctions restrict the normal function of the vocal articulator but do not impactdaily understanding. Laryngeal nerve disruption decreases vocal fold vibration regulation, resulting in distorted speech. Dysarthria type and complexity focus on which region is impaired by the nervous system. Cerebral palsy, for example, is a brain injury that leads to less coordination of the muscles. Spastic dysarthria is caused by the disruption to the spinal cord or brain which impacts the muscles involved in making speech. This results in speech with anomalous features that may be unintelligible to various degrees Dysarthric speech's decreased intelligibility can complicate, frustrating and time consuming verbal communication[1].

Dysarthria is categorized into 6 various kinds depending on the affected part of the nervous system[2,3]. Spastic flaccid, hypokinetic, hyperkinetic, ataxic, mixed are the 6 various kinds. In all 6 forms of dysarthria, the common disorder is phonatory dysfunction. This reduces the speakers ' intelligibility by altering the speech's naturalness[2,5]. This condition is very hard to evaluate because it correlates with other breathing, prosody disorders, articulation, rhythm, and phonation[4].

NADIA
Advancement Through Research

SYNTHESIS OF CONCENTRIC CIRCULAR ARRAY ANTENNA THINNING USING ROUND & PUSH TO LIMIT BINARY EVOLUTIONARY PROGRAMMING

[31 Dec 2020 | vol. 13 | no. 4 | pp. 33-44]

About Authors:

Meenakshi L Rathod1*, Meera A2 and Manoj Kumar Singh3
-1Dept.of E&C Engg., Dr. Ambedkar Institute of Technology, Bangalore, India
-2Dept. of E&C Engg., B.M.S.College of Engineering, Bangalore, India
-3Manuro Tech.Research Pvt. Ltd., Bangalore, India

Abstract:

In this work, the desired radiation pattern is achieved by the use of thinning concept which reduces the side lobe level and first null radiation bandwidth of concentric circular array antenna. The objective of minimizing the number of elements of array to reduce the price has been optimized using evolutionary strategy. The proposed method is carried out using a self-adaptive strategy of mutation along with round and push to limit form and to transform the solution from real domain to binary domain. The proposed method has been applied over two ring concentric circular array. This approach of transformation has shown to be better as compared to conventional sigmoid function transform approach. The advantages have been shown by performance comparison against the firefly method. The suggested method has not only achieved superior design characteristics but also without fail there is a faster convergence.

Keywords:

Circular Array Antenna, Thinning, Side Lobe Level, Half Power Beam Width, First Null Beam Width, Evolutionary Programming

About IJFGCN

IJFGCN aims to facilitate and support research related to future generation communication and networking. Our Journal provides a chance for academic and industry professionals to discuss recent progress in the area of future generation communication and networking.

IJGDC Published Article

VERIFICATION AND VALIDATION OF ASBO BASED ANTENNA ARRAY RADIATION PATTERN SYNTHESIS FOR POWER OPTIMIZATION

Published 31 MARCH 2021 • vol 14 • no 1 • PP. 35-42

Authors:

Meenakshi L. Rathod, *Department of E&C Engg. Dr. Ambedkar Institute of Technology, Bangalore, India*
Meera A, *Department of E&C Engg. B.M.S. College of Engineering, Bangalore, India*

Abstract:

This paper discusses the results of array antenna radiation pattern obtained from MATLAB and CST microwave studio to provide a basis for comparison between results. For verifying and validating the MATLAB results obtained by natural computation approach called Adaptive Social Behavior Optimization (ASBO), same parameters are used on CST microwave studio EM simulation. ASBO has applied to synthesize the radiation pattern of the linear antenna array with controlled nulls in the direction of unwanted interference sources. Each array element phase parameter has considered for controlling the shape of the pattern in order to steer the main beam in the desired direction and define null in the direction of interference. The radiation pattern of a microstrip patch antenna array resonating at 9 GHz with controlled null is synthesized using CST simulation tool. The phase parameter of each array element has been considered for controlling the shape of the pattern in order to steer the main beam in the desired direction and define null in the direction of interference. Hence the elements on CST are excited with same phase as computed by ASBO using MATLAB. The EM simulation results of CST show a close correlation with those obtained through MATLAB.

Keywords:

Verificatin, Antenna array, Side Lobe Level(SLL), Null, CST, Matlab

Research Article

Design of Microstrip Dual-Mode Wideband Bandpass Filter with Controlled Center Frequency and Bandwidth Using Bandstop Filter Topology

Shobha Hugar, V.B. Mungurwadi & J.S. Baligar

Published online: 30 May 2021

Download citation https://doi.org/10.1080/03772063.2021.1929518 Check for updates

Abstract

This paper discusses a new method for designing a microstrip dual-mode, sharp skirt, wideband bandpass filter with controlled center frequency and bandwidth from bandstop filter topology. A meander closed loop resonator with directly connected orthogonal feed lines provides a Bandstop filter (BSF) with reduced size. A pair of L-shaped open stubs introduced along the diagonal axis D-D[1] realizes a

Optimized Modular Arithmetic and Logic unit in Reversible Logic

Girija S[1], Dr. Sangeetha B.G[2]
Department of Electronics and Communication, Dr. Ambedkar Institute of Technology, India
Department of Electronics and Communication, RNS Institute of Technology, India
girija.pari@gmail.com, sangeethabg@gmail.com

Abstract

Low power consumption is the most desirable factor in all data processing systems. Past the CMOS technology needs to be dominated by other technologies owing to limitations in further scaling down of transistors has reached physical limitations. Device intensity and speeds must be achieved by combating the power issues. The trend is to look for other technologies that guarantee minimal or zero power dissipation. Reversible logic is gaining admiration among researcher for its zero-power dissipation. Arithmetic and logical unit is a subsystem central to any computers performing several operations based on control signals. This paper proposes an approach to design an efficient and optimized Arithmetic and Logical Unit (ALU) to adaptable for quantum computers. ALU proposed performs arithmetic and logical operations based on the choice. Its performance is evaluated based on cost metrics of reversible logic, in comparison with available designs shows an improvement of 38% in quantum cost, 35% of unused outputs and 100% reduction in ancilla inputs.

Keywords: *Ancilla, Garbage, integrated, quantum cost*

1. Introduction

Increase in density is directly proportional to increase in power consumption which is not preferable in modern mobile computing devices. There are futuristic technologies emerging to tackle issues like area, low power and extremely high speed. Reversible logic is a technology in the fore front due to its capability for achieving zero power dissipation. In conventional logic, during computation, information bit loss occurs resulting in power consumption. This is avoidable if operations were to be carried out in reversible manner according to [1]. Author Bennet's paper claimed amount of energy would be conserved in a designed circuit if operations were to be executed in reversible way [2]. Moore predicted number of transistors would be doubles every 18 months and associated problems with this is increased energy to accommodate higher magnitude of transistors. Reversible computation is unconventional, involving special type of gates rather than conventional gates. Reversibility adopted in digital circuits is called logical reversibility. Reversible circuits are built with reversible gates which has special property where number input and output vectors are same, bijective in nature. Findings reveal energy dissipation are due to bit loss not due to process involved, hence reversible logic preserves this consumption [20]. Future belongs to quantum computing and fundamentally operations involved in quantum computing are reversible in nature. Just like the bit 0 and 1 fundamental to characterize information in conventional logic, quantum computing uses quantum bits <0 and <1 states of qubits. Quantum bits can be in

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Optimized Low Power Dual Edge Triggered Flip-flop with Speed Enhancement

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Abstract: This paper gives a novel low-power approach with pulse generating circuits using dual edge triggered flip-flops. By doing so, flip-flop might operate at 1.2Volts, with the novel quick latch and conditional precharging.

This paper aims at a new proposed low power dual edge triggered flip-flop with speed enhancement to achieve low power consumption with a shorter delay in power usage, hence, it is well suited for low-power digital system applications. The new proposed low power dual edge triggered flip-flop also aims at comparison with the three DETFF, Static Output Controlled Discharge Flip-Flop (SCDFF), Dual Edge Triggered Static Pulsed Flip-flop (DETSPFF), and Pervious work on Dual Edge Triggered flip-flop, proves to achieves with reduction in numbers of transistors in the stack and increases the number of charge-paths results in a faster operational speed. According to simulation on Spectre simulator, it has been observed that total power consumption of proposed flip flop at 0.67 switching activity is 30.16 % and 27.36 % less than that of previous arts DSPFF and SCDFF respectively. Clock-gated sense-amplifier is incorporated to reduce power consumption at low switching activity. The simulation is done using Cadence tool with 45nm standard CMOS technology.

Index Terms: Dual Edge Triggered (DET), DETFFs (double-edge-triggered flip-flops), Dual Edge Triggered Static Pulsed flip-flop (DETSPFF), Static output Controlled Discharge Flip-flop (SCDFF), FF (Flip-Flop), Single Edge Triggered (SET), Sense Amplifier (SA), VLSI (Very large scale integration).

1. Introduction

The clock matrix constitutes clock distribution networks and FF are the most potent hungry components for numerous VLSI digital systems.

It consumes thirty percent to sixty percent of total system power with the FF's & the final divisions of the clock distribution network driving flip-flops using 90 percent of that. The system power division of clocking can be supplementary evident as a result of the new generation frequency scaling and extensive pipelining. Because today's portable digital circuits have a restricted power budget, it's critical to reduce the power dissipation in clock network and flip-flops.

There are several ways to reduce clock power. The most influential way is V_{dd} scaling, which has quadratic impact on PcIk' However, V_{dd} has already been reduced along with downscaling of process. The capacitance is unlikely to decrease as long as the number of transistors in a circuit becomes larger and functionality is more complex. One effective way to reduce f_{Clk} without performance degradation is to use dual edge-triggered flip-flops (DETFFs). The cross DETFF requires only half of f_{clk} to maintain the same throughput as single edge-triggered flip-flop (SETFF). Two main categories of DETFFs are master slave and pulse triggered. They put positive and negative flip-flops in parallel to perform dual edge triggering. These structures are straightforward. However, the internal are charging and discharging at every clock cycle regardless of the input even when they are sampled at the same value. This wastes a lot of power. Pulse triggered flip-flop is used for low power consumption.

The paper discussion organizes in following manner. The previous work on dual edge triggered flip-flops (DETFF) is reviewed, the structure and operating principal of proposed design, simulation results are presented and in last, we draw conclusion in the final section.

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IOT BASED ENVIRONMENT MONITORING SYSTEM

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Abstract : Indoor air quality defines the quality of air in a premise, which intern refers to the health and comforts of inhabitants. The microbial action which depends on surrounding temperature and humidity, gaseous pollutants, dust particles etc. affect the IAQ. These pollutants can adversely affect the health of building occupants. To overcome this problem an air quality monitoring system is necessary. As a solution a toolkit has been developed to view the live air quality.

IndexTerms **- IOT, Blynk Cloud, AQI.**

I. INTRODUCTION

The proposed paper is an IOT based application to deal with air pollution. How it works and what are all the models present will be explained. The aim of the paper is to provide an IOT based solution to tool (air pollution) with the help of sensor such as mq135 various air parameters can be sensed. To transmit sensed elements we need one development board and we are going to use NODE MCU. The proposed prototype with the help of Wi-Fi it uploads all fetched information of air into satellites. This is the overall idea of paper. It's an IOT based application it makes use of an sensor. The heart of the paper is NODE MCU development board and with help of Wi-Fi the read parameters are uploaded to centralized server.

II. REVIEW OF LITERATURE SURVEY

If we talk about conventional monitoring system, they are much expensive and consume a lot of space and is not ideal for indoor applications. We also come across many systems where the system reads wrong concentration of pollutants. This happens when the sensors used are not calibrated properly before using it. These problems have been solved by us by making a portable system, keeping in mind about the cost. And also, we have calibrated all the sensors properly and as we have used IOT, the user can get to know about the pollutants through the use of cloud in addition to the LCD screen.

III. PROBLEM DEFINTION AND PROPOSED METHOD

The proposed system is IOT based paper and all functional units present in the proposed system connected in network. Since all the things such as sensors, servers they work together over an network and they communicate easily each other. The data which is collected from sensors get upload to cloud servers instantly with mobile. This helps authority such as pollution control board authorities to fetch the data easily and with the help of real time data they can take conclusions/actions instantly .This is the advantage of proposed system.

Auto Sunlight Tracking Solar Powered IOT Based Light Control System

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Abstract

This paper deals with Sunlight Tracker Solar Powered IOT Based Light Control System. This is a concept to conserve energy and reduce pollution caused by exhaustible resources. It is implemented using Arduino Uno as it is cheap and open source. The function of this system is to detect human presence in the surrounding using IR sensors and communicate with the Arduino Uno board to control the lighting system. The Intelligent System works according to the presence and arranges the dimness and controlling system of the light along with the simultaneous working of the solar tracker. The solar tracker receives sunlight in a more efficient way than a conventional solar panel by tracing the path of the sunlight.

Keywords: LDR, IR emitter and receiver, LCD, Arduino Uno Board, Supply, Motors.

1. Introduction

The work is about automation of lighting system powered with solar tracker for efficient application of lighting system. Energy crisis is a critical issue in the present day due to the increase in demand for power. At present smart lighting ensure reduction of power consumption. The auto sunlight tracker powered IOT based light control system not only reduces power consumption by controlling light but also promotes the use of renewable energy. We achieve this using IR sensors and LDR's by continuously monitoring the illumination in surrounding and human presence. The solar tracker is 30% more efficient than a conventional solar panel which remains in a stationary position. This paper will help us to overcome that problem along with Utilizing the solar energy collected through solar tracker. There by ensuring the utmost minimization of electricity, this will help in developing economic crisis of the country.

2. Pervious Work

2.1. Literature Survey for Auto Solar Tracking System

This describes the working and architecture of an automatic solar tracker system. The system consists of light dependent resistors which senses the direction in which maximum solar power is being received and which is given to Arduino Uno which process the output. LDR is an active sensor which constantly monitors light in surrounding and rotates the solar panel in the direction where strength of sunlight is maximum. Due to rotation of earth around sun, solar panels can't always face the sun. This system constantly controls the solar panel to face the earth.

This paper explains how global warming is a major issue and how we can prevent it using such systems. The Solar tracking system is based on AVR microcontroller, which is the brain of the entire system. It will monitor and control the entire system. Our system is cost effective and installation is quite easy, but installation of solar tracker is a bit complex. It consists of LDR's, metal structure and solar panel. This solar panel converts the solar energy to electrical energy through photo voltaic effect and stores it in the battery. This paper mainly targets to reduce carbon emissions and have a reliable power supply.

Ultra-Optimized 8-bit Unsigned Array Multiplier design using Reversible Logic

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Abstract: Low power dissipation has become the key concern for design of computational circuit and implementation. Reversible logic is one of the best alternative method to reduce power dissipation compared to irreversible logic circuit. Multipliers designed using reversible logic has a wide variety of applications in digital signal processing and other computational applications. The forthcoming computing is extremely reliant on reversible logic because reversible logic computation shrinks the power dissipation compared to irreversible logic-based circuit. The paper proposes, 4-bit and 8-bit reversible unsigned array multiplier using HNG, Peres and BME gates. The design utilizes 20 reversible logic gates, 28 garbage outputs and 104 quantum cost. The simulation result shows 50% reduction in constant inputs and garbage outputs, 30% reduction in number of gates and 20 % reduction in quantum cost. Furthermore, proposed design is matched with the existing designs in terms of optimization parameters.

Index Terms: Array Multiplier, Reversible Logic, Quantum Cost, Garbage Output, BME gate.

1. Introduction

Information preservation is the key motivation in reversible logic to reduce the energy dissipation of circuit designed. Landauer's principle mentions that removal of each bit of information releases an amount of kTln2 joules of heat energy [1], where k equal to 1.380648 10e23 Joules per Kelvin, Boltzmann constant and T is the temperature in Kelvin. Reversible logic offers an optimized solution to energy dissipation in the form of heat. Bennet proved that if the computation is done in reversible way, it is possible to reduce the power dissipation of kTln2 joules of energy [2, 3]. A gate is said to be reversible, one to one mapping between the input and output variables and output pattern has a unique vector [4]. The significant optimization parameter plays a key role in the design of reversible circuit is constant inputs, garbage outputs, gate count and quantum cost. Feyman, Toffoli, Peres and Fredkin gates are fundamental building gates in the design of reversible circuits [5].

Multipliers are the key major computational components used in computations and other numerous applications [6]. With the enhancements in designs and technology, many investigators are investigating to design multipliers which offer the best design targets such as reduced area in terms of gate count, low quantum cost, high speed, hence regularity of design for numerous high speed, low quantum cost and optimized VLSI applications. Optimized multiplier must have less gate count, consumes less power and should have high speed of operation. Various methods are available in the literature, to design optimized multipliers [7-9]. External methods are associated with the changes of input characteristics but internal methods are associated with the technology and architecture.

Array multiplier is identified because of its regular structure. Designs are done by add and shift method [7]. Partial products are generated by multiplying one bit of the multiplicand with each bit of multiplier and is generated according to their bits generated and added.

The paper presents an ultra-area optimized and quantum cost efficient array multiplier using reversible logic. Multiplier is designed using BME gate to produce partial products and multi bit addition using Peres and HNG gate.

2. Proposed Reversible Unsigned Array Multiplier Framework.

Among the existing multiplier design unsigned array multiplier is most identified because of its regular arrangement. It is based on generating partial products, adding and shifting algorithm as shown in fig 1. Addition operation can be performed by ripple carry adder or any fast adder. Generally, array multiplier requires N (N-1) number of adders to

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Title

Study and Performance analysis of different multiprocessor real time schedulers

Authors

RAMAPPA HIREMANI
Siddesha K
Kavitha Narayana B M

Abstract

A scheduling system for real time scenario consists of clock, processing hard-ware elements and clock. In real time systems, a task/process exhibits schedulability in which real time system accepts the tasks and does task completion based on the task deadline defined in the scheduling algorithm. To perform the real time scheduling, different scheduling algorithms were developed and are able to man-age the multiprocessor architectures. However, these algorithms are leading to new challenges in scheduling due to more complexity of the multiprocessors. Al-so, the scheduling algorithms cannot be evaluated without a real as well as complex implementation. This manuscript focused on the study and performance analysis of different multiprocessor real time schedulers. The performance analysis is carried out by using SimSo scheduling tool that extracts the scheduler class from python. In this, the scheduling algorithms like Deadline Partitioning (DP)-WRAP, EKG, Earliest deadline first (EDF) are studied and analyzed for their performance. From the analysis is observed that Load on EDF is much different than EKG and DP-WRAP as it meets deadlines. Most of the time, the schedulers like DP-WRAP and EDF are considered as partitioned scheduler most of the time and also DP-WRAP scheduler generates lot of migrations. Hence, EDF scheduler is considered as more efficient than DP-WRAP and EKG schedulers based on preemptions and migrations. However, some of the jobs are aborted due to dead-line misses.

Key Words

Real time scheduling, Multiprocessor, Scheduling algorithms, Preemptions and Migrations

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Generation of Narrowband Signals for Wireless Body Area Networks

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Abstract - *Wireless body area networks (WBAN's) have gained much attention recently because of miniaturization of electronic device and due to a multitude of applications. Narrowband communication is emerging transmission technology for WBAN's because of reduced hardware complexity. In this paper summarizes the design issues for physical layer proposals with narrowband signals. Here minimum shift keying (MSK) modulation technique is used as one of the design issues of the WBAN's and presents the MATLAB and SIMULINK implementation of generation of narrowband signals using MSK modulation scheme.*

Key Words: modulations, continuous phase frequency shift key (CPFSK), minimum shift key (MSK), wireless body area networks (WBAN's).

1. INTRODUCTION

The recent trends in communication and technical developments of the last few decades are grasping attention towards several prominent applications for wireless body area networks (WBANs) such as health monitoring or ubiquitous computing. The use of wireless networks and the constant miniaturization of electrical invasive/non-invasive devices have empow- ered the development of Wireless Body Area Networks (WBANs). In a WBAN, several small nodes are placed close or directly on the human body. Since such nodes shall get their power from rechargeable batteries or by energy harvesting they have to be very energy efficient. Moreover, due to cost reasons and due to the relative high number of nodes in a WBAN the nodes shall be of low complexity. One transmission technology for WBANs promising less complex hardware is narrowband communication.

WBAN system can be categorized into two parts by its applications: medical BAN and non-medical BAN. Nonmedical BAN can be regarded as wearable consumer electronics and entertainment devices for the on-body communications. Medical BAN consists of implant devices and wearable medical systems to measure the health status of human body with In-body or on-body communications. Since there are different requirements for the systems by various applications, the several technologies for physical layer designs are suggested as amplitude shift keying (ASK), variations of frequency-shift keying (FSK), offset quadrature. The ultra wideband (UWB) technologies are also proposed with impulse radio (IR), chirp, and frequency modulation (FM) method. The narrowband proposals are explained interms of frequency bands, modulation options, and some key features such as modulation, packet structure, and so on.

2. NARROWBAND TECHNOLOGY

The basic design approach for the in-body or on-body communications demands the simplicity and efficiency in physical layer implementation. Since the technical requirements show diverse applications and large span of data rate, however, there will be a difficulty in selecting the prominent technology for the WBAN systems. The merit of narrow band communication is to realize stable long-range communication. In addition to, the carrier purity of transmission spectrum is very good; therefore it is available to manage an operation of many radio devices within same frequency bandwidth at same time. [1]

2.1 Modulation technic overview

In the analog communication, digital modulation of data transmission relies on the use of sinusoidal carrier wave to modulate the incoming data bit stream. In digital pass band transmission the incoming data stream is modulated onto a carrier with fixed frequency limits imposed by band pass channel of interest. In this event the modulation process making the transmission possible involves switching, or commonly known as keying, the amplitude, frequency or the phase of the sinusoidal carrier in some fashion in accordance with the incoming data stream. Thus there are three basic signaling schemes [2]

1. Amplitude shift keying : Amplitude is varied in accordance with the input data
2. Frequency shift keying : Frequency is varied in accordance with the input data
3. Phase shift keying : Phase is varied in accordance with the input data.

3. MINIMUM SHIFT KEYING (MSK)

In digital communication modulation technique binary data consisting of sharp transitions between "one" and "zero" states and vice versa actually creates signals that have sidebands extending out a long way from the carrier, and this leads problems for many radio communications systems, as any sidebands outside the allowed bandwidth cause interference to adjacent channels and any radio communications links that may be using them.

MSK, minimum shift keying has the feature that there are no phase discontinuities and this significantly reduces the

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Transactional Blockchain Implementation With Client Interface Using SHA-256 Cryptographic Hashing

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Author Name : Shwetha N, Gangadhar N, Sangeetha N, Anagha Anand, Divya, Jyeshta B Suyog

ABSTRACT
Block-chain Technology is a peer to peer, decentralized, distributed ledger technology (DLT) which has taken the business and tech world by storm. Block chain uses the concept of using hashing in the blockchain system to make it so secure that no one can make changes or remove the records once saved in the blockchain. Transactions are authenticated by miners who are part of the decentralized network. In this paper we are trying to implement transactional blockchain with client interface using SHA-256 cryptographic hashing.
Keywords: Blockchain technology, decentralized network, distributed ledger technology(DLT), SHA-256 hashing.

ROBUST FACE RECOGNITION USING HYBRID FEATURES

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ROBUST FACE RECOGNITION USING HYBRID FEATURES

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ABSTRACT

Face Recognition is one of the most prominent recognition methods to give authentication to an individual. Since the face is the most important Identification feature of a human being, the Face biometric trait plays a key role in recognition of an individual. This paper contributes an efficient algorithm for the recognition of Individuals using Face biometric. The proposed algorithm captures the face features using Harris, SIFT, and SURF techniques from a preprocessed face image. The Linear Discriminant Analysis is used for dimension reduction of the Face features. The Nearest Neighbor classifier is used for matching and performance is analyzed by measuring TSR, FRR, FAR, and EER values for JAFFE and ORL databases.

Key words: Face Recognition; Scale-Invariant Feature Transform (SIFT), Speeded up robust features (SURF), Nearest Neighbor (NN), Total Success Rate (TSR), False Rejection Rate (FRR), False Acceptance Rate (FAR), Equal Error Rate (EER), Linear Discriminant Analysis (LDA)

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1. INTRODUCTION

The Biometric recognition is an essential system and is used to authenticate the individual identity using the physiological or behavioral characteristics of an individual which provides the authentication even at surveillance activities. Biometric Authentication of an individual has become a more protected and secured method in today's world because of its high reliability in recognition against usual methods like Authentication codes, Passwords, Personal ID cards, PIN codes, and Swipe cards which are being outdated because authentication is easily

Generation of Binary Sequences of Length 10230 Bits Having Better Odd and Even Correlation with Large Linear Complexity for Use in Global Navigation Satellites Systems (GNSS) Applications

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Abstract:

Binary sequences used in Global Navigation Satellites Systems (GNSS) are found to be easily decoded due to less linear complexity. The correlation properties are extremely important while selecting the sequences for GNSS Applications. Linear Feedback Shift Register (LFSR) based Sequences are being used in GNSS Systems such as Global Positioning System (GPS) L2 CM (L2 frequency band Civil Moderate) Signal. Due to the short cycling of LFSR these sequences result in poor correlation properties. In this work the properties of binary sequences used in the state of the art GPS L2CM Navigation signal is explored. The odd and even correlation properties of GPS L2CM sequences are presented in detail. These sequences are analyzed for their Linear Complexity property. A method is proposed for generation of 10230 bit length binary sequences. A new set of binary sequences with set size of 47 sequences are generated using chaotic real sequences. The generated sequences are analyzed for odd correlation, even correlation and linear complexity properties. The proposed binary sequences are found to have better correlation and excellent linear complexity properties as compared to GPS L2 CM Sequences, which make them suitable for use in GNSS Applications.

Keywords:

global positioning system (GPS), global navigation satellites systems (GNSS), chaotic logistic map, auto correlation, cross correlation, linear complexity (LC)

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Efficient Temporal-key Based Encryption Mechanism for WSN-ETEM

Premakumar MN, Ramesh S

Abstract: ***Wireless sensor networks (WSNs) are a promising technology for several industrial real-time and quotidian applications. Due to inherent limitations in WSN, security is a crucial issue. Cryptographic primitives are the fundamental components for designing security protocols to achieve security and privacy in WSN. Based on the review, it has been analyzed that the majority of security protocols for WSN are based on encryption and key distribution. The main open issue for these approaches concerns the establishment of security with an involvement of complex procedure, which presents considerable memory overheads, in contrast with the limited resources of sensor nodes. Therefore, the proposed work presents the modeling of an analytical approach for efficient encryption using temporal key management for robust security services to resists potential attacks and enables secure communication. The utilization of temporal-key mechanism in encryption operation offers additional support to routing operation in the network for secure data transmission with negligible computational overhead, thus preserving a higher level of energy savings in packet transmission operation. The validation of the proposed system performance is carried out a simulation study, which shows the effectiveness of the proposed system in terms of node remaining energy and processing time.***

Keywords: WSN, Security, Authentication, Encryption, Key distribution, routing, sensors

I. INTRODUCTION

Wireless Sensor Networks (WSNs) are a collection of inexpensive micro sensor devices that are typically deployed in surveillance areas. These micro sensor devices have the inherent features of an ad hoc function that communicates over a radio channel, designed to sense events, collect information, and pass collected information to the user via a local repository center called the base station-(BS) [1-2]. As an emerging technology, WSN has practical value and has become a backbone for various applications and has gained global attention in many organizations. The sensor devices or nodes in the distribution area can get a lot of detailed and reliable information for various applications such as military, automobile industry, agriculture, urban management, security surveillance, biomedical, environmental monitoring, disaster relief, smart home, smart healthcare, and so on[3]. However, WSN is mainly organized in harsh surroundings where human intervention is quite difficult. There is a real challenging factor associated with the sensor nodes as it belongs to resource constraints nature such as energy, bandwidth, computing potential, and storage volume are limited, making WSN vulnerable [4]. The security of WSN has caused widespread social concern. Especially in critical applications like military target detection, healthcare for which information is very sensitive, and once WSN is attacked, and then it can lead to catastrophic consequences. Therefore, a robust, efficient security protocol is required in WSN to attain confidentiality protection and authentication functions to enable a fairly safe environment for node communication and data transmission against malicious activity [5-6]. Therefore, the challenges associated with WSN security have become a key issue in the research field. Over the past few years, a lot of research has been done on security aspects of WSN to provide reliable communication and data sharing operations. Unfortunately, many traditional security techniques are not feasible and are not suitable to be implemented in WSNs with resource deficient nodes as they are associated with high computational complexity [7-8]. Therefore, the major challenge in WSN security is the trade-off between energy use reduction and security enhancement [9]. As WSN is nowadays adopted in various realtime and delay-sensitive applications, it is necessary to promote security features about hybrid approaches with high energy efficiency as different types of information exchange processes occur in WSNs and have different security needs [10]. Therefore a single security mechanism cannot meet these requirements. Therefore, the proposed research work offers a novel security approach formulated using an encryption mechanism and temporal key management scheme. Thereby the proposed schemes enable less-complexity based robust security implementation mechanism that can restrict the adverse impact of security threats and various types of attacks and meets the higher energy-efficiency requirements by supporting user demand clustering operation during routing process for the data transmission. Finally, the performance validation of the proposed methodology is analyzed regarding the remaining energy and processing time. The remainders of this paper are ordered as follows: Section-II is carried review of existing literature. Section-III illustrates research problem based on the review study. Section IV discusses proposed design. Section-V presents algorithm as operational strategy for implementing proposed methodology. Section VI presents result and discussion. Finally the conclusion is presented in Section VII.

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Chaotic Binary Sequence Generator based on Logistic Map

K. Chidananda Murthy, Mahalinga. V. Mandi, R. Murali

Abstract*— Pseudorandom binary sequences find various applications in different areas such as security, communication, steganography and cryptography. The properties like sensitivity to initial condition, ergodicity, mixing property and dynamic behavior are used in the designing of random number generators known as chaotic systems. In this study, an efficient chaotic binary sequence generator using logistic map is proposed, implemented and analyzed. The proposed binary sequence generator generates 50 chaotic sequences by varying initial condition with fixed system parameter. Subsequently, the generated sequences are transformed to binary sequences using thresholding method. The output of binary sequences is statistically tested with FIPS 140-2 test suite in order to identify the specific properties expected for truly random binary sequences. The experimental results prove that the generated binary sequences possess identical characteristics of true random numbers and can pass all tests of FIPS 140-2 test suite.

Keywords: Chaotic map, chaotic binary sequence, logistic map, FIPS 140-2 and poker test.

I. INTRODUCTION

Communication technology and the popularity of the internet have expanded the field of data transmission and reception which leads to new challenges for securing user data from illegal access. Today, almost everyone across the globe is using internet for exchanging information. Hence, information security is of fundamental importance against unauthorized eavesdropping. Cryptographic techniques are the most popular and widely used methods to deal with the problems of information security. Several security systems make use of different cryptographic techniques to protect the data [1]. Various encryption methods are reported in literature. Amidst, pseudorandom binary sequence-based encryption method is utilized across various fields such as military, spread spectrum communications, watermarking and stochastic computation because of its execution speed, easy implementation and high security [2, 3, 4]. Many research efforts have been carried out on the generation of pseudo random numbers. Most of earlier methods depend on the linear congruential method, mid square method, linear and nonlinear feedback shift registers. However, these methods have limited security due to their fixed linear structure [5]. Further to this, these methods cannot satisfy the conventions of Golomb [6]. Hence, it is an interesting area of research to generate pseudorandom numbers with good statistical properties using cryptographic techniques.

Recently, nonlinear dynamical systems, chaos theory has caught more attention from researchers for generating random numbers. Chaotic systems are nonlinear deterministic, nonperiodic and non-converging in nature. The future importance of chaotic systems is dependent on their initial condition and system parameter. Properties of chaotic systems such as sensitivity to initial conditions, system or growth parameter, ergodicity, mixing property, flexibility of the length of sequences, good correlation properties, difficulty of interception and the multiple access capability [7] make the chaotic systems a potential candidate for spread spectrum communication. In addition to this, chaotic sequences are generated by deterministic systems, random like but they can be reproduced.

In this study, an efficient chaotic binary sequence generator using logistic map is proposed. 50 chaotic sequences are generated directly from the logistic map function by varying initial condition with discrete fixed system parameter. These analog chaotic sequences are converted to binary sequences using thresholding method. The randomness properties of the corresponding chaotic binary sequences are investigated. Statistical properties of the generated sequences are validated employing FIPS 140-2 test suite. Results reveal that the binary sequences pose good attributes of true random numbers, difficult to predict and stable.

The rest of the paper is structured as follows. Section 2 presents the review related works in this domain. Section 3 explains the logistic map function. Section 4 presents the functioning of the planned chaotic binary sequence generator. Section 5 provides numerical results and discussion. Section 6 concludes the paper followed by relevant references.

II. RELATED WORKS

Swami and Sarma [1] designed a pseudorandom number generator using logistic map function for spread spectrum communication. Performance of the proposed generator was validated on a multipath environment with Rayleigh channel. Kanso et al. [2] proposed two different methods for binary sequence generation. The first method was proposed using 1D logistic map and the second method was proposed with two logistic map functions. Beker and piper's test suites were employed to detect the characteristics of the binary sequence.

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Sharp Skirt Dual-Mode Bandpass Filter with Overlay Plate to Control Upper Passband Edge

Shobha Hugar, Vaishali B M, J S Baligar

Abstract: ***This paper presents design and analytical model for Sharp Skirt Dual-Mode Bandpass Filter for RF receivers. Proposed filter is designed using open stub loaded H shaped resonator. Based on analytical model insertion loss S_{21} and return loss S_{11} for proposed filter are demonstrated. Inductive Overlaying plate is proposed to control upper passband edge of proposed filter to improve frequency selectivity with fixed center frequency. The proposed filter has sharp frequency selective range from 5.1GHz to 9.2GHz. With overlay plate, frequency selective range is tuned to 5.1GHz-8.6GHz. Without overlaying plate the proposed filter has return loss greater than 10dB and insertion loss of 0.7dB. Lower and upper passband edges are at 5.1GHz and 9.2GHz with attenuation level of 52dB and 54dB respectively. With overlaying plate, the filter has same S_{11} and S_{21} parameters, but upper passband edge is shifted from 9.2GHz to 8.6GHz.***

Keywords: Dual-Mode, Overlayplate, Passband edge, Printed Circuit Board Technology

I. INTRODUCTION

The performance of RF receivers is measured in terms of its selectivity to receive desired range of frequencies and reject undesired frequencies to eliminate interferences from other channels. High performance miniaturized sharp frequency selectivity Microstrip Bandpass filters play a vital role in RF receivers. Since these filters are cost effective and easily fabricated by Printed circuit Board Technology (PCB) they have gathered more attention in satellite and mobile communications. In literature, Star shaped resonator with triangular perturbation, triangular patch with vertical and horizontal slots, symmetrical fractal structure etched on meander loop resonator have been proposed to design Dual-Mode filters [1-3]. Parallel coupled stepped impedance resonator with proper tapping at input and output resonators has been proposed [4] and tunable transmission zeros in stopband have been achieved with tapping at input and output. An "extended doublet" coupling schematic [5] has been proposed to create one pair of transmission zeros near passband to improve the selectivity of the filter. This paper demonstrates design and analytical model for proposed filter. The proposed filter comprises of Dual-mode H shaped resonator as depicted in fig 1.

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Symmetrical frequency response with two transmission zeros in lower and upper passband edges are achieved with source load coupling which enhances frequency selectivity of the filter. Proposed filter configuration is depicted in fig.2.

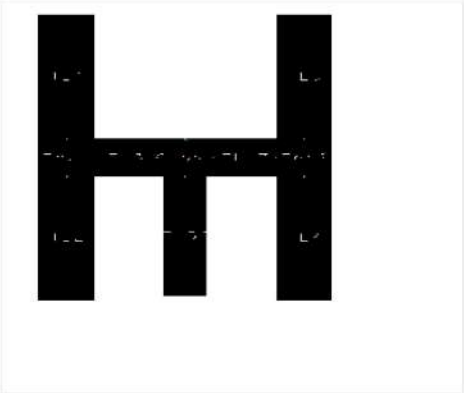

Fig.1. Proposed H shaped Dual-mode Resonator.

The paper is organized as follows. In Section II, Based on Analytical model, Insertion loss and Return loss for proposed filter are demonstrated. In Section III, controlling upper passband edge and tuning the frequency selective range of proposed filter with Overlaying plate is discussed. Section IV concludes the work presented in this paper.

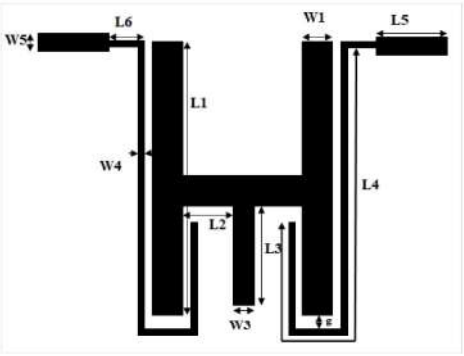

Fig.2 Proposed Filter Configuration

The proposed filter is designed for center frequency 7.45 GHz and flat passband between 7.2GHz to 7.9GHz, lower rejection band up to 100MHz with attenuation level of 20dB and upper rejection band up to 10GHz with attenuation level of 44.5dB.

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VHDL implementation of acquisition sensor for optical communication terminal

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ABSTRACT

This paper presents the development of the Acquisition sensor which is a part of overall Acquisition, Tracking and Pointing (ATP) mechanism for maintaining the Line Of Sight (LOS) between two Optical Communication Terminals (OCT). The ATP mechanism is basically used to align the transmitting and the receiving optical communication terminals which in turn can continuously transmit the data between them. The Acquisition sensor is designed to acquire the LASER image falling on it which is being transmitted by the transmitter terminal and to process this image to calculate the 2-axis angular error. This error is then used to re-position the terminal to maintain the LoS if it is out from the Field of View (FOV) of the transmitter by feeding this data to Tracking and Pointing modules of ATP mechanism.

Keywords— *Optical Communication Terminal (OCT), Acquisition sensor, Line of sight (LoS), Two-axis angular error, Centroid of an image, ATP mechanism*

1. INTRODUCTION

Optical Inter Satellite communication is one of the emerging technologies to meet data transfer requirements at higher rates. This requirement is arising from the space crafts which can handle a large amount of payload data. The main optical carrier of data in the optical inter satellite communication is the LASER beam having high data rate which enhances the communication capacity. The major challenge of Optical Inter Satellite Link is the requirement of precise pointing of optical beam, with high accuracy. To achieve this, Acquisition, Tracking and Pointing (ATP) mechanism is used. This mechanism establishes and maintains the communication link between the two Optical Communication Terminals (OCT). Acquisition sensor module in the ATP mechanism is used for initial pointing, and acquisition of data from the target terminal. During the acquisition phase of OCT, master terminal scans the uncertainty area of the target terminal using a fine laser beam of 20 µrad divergences. The target terminal will wait for the presence of a laser beam on its acquisition sensor. The function of the acquisition sensor is to derive the 2-axis angular error with respect to the Line of Sight (LOS) of OCTs.

2. DESIGNING ACQUISITION SENSOR

Acquisition sensor consists of a SWIR detector, analog processing section and FPGA based digital signal processing section. The function of FPGA is to generate the driving signals for the detector, and process the detector output by generating drive signals to the components in the analog processing block and compute the centroid. Additionally FPGA has to compute the 2-axis angular error for the Tracking sensor module.

The design of the Acquisition sensor using FPGA includes the functionality as shown in fig.1. The basic acquisition component used is the SWIR (Short Wave Infrared) detector. This detector will acquire the data (intensity) from the laser light of wavelength 1550 nm falling on it. The 8-channel analog intensity output produced by the detector is passed on to the analog signal processing circuit.

The analog signal processing circuit includes multiplexers for selecting between the multiple output lines of the detector and the analog to digital converters to convert the analog data into the digital form. The FPGA requires digital data for processing. This

ANALYSIS OF CONVOLUTIONAL NEURAL NETWORKS FOR RUST CONTROL IN BUILDING AND OTHER APPEARANCES

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ABSTRACT

Cutting-edge useful resource state of affairs appraisal method are widely tedious, arduous, and costly and gift nicely being and safety risks to surveyors, mainly at stature and rooftop stages that are difficult to get to. This paper dreams assessing using convolutional neural structures (CNN) in the direction of a mechanized discovery and confinement of key structure absconds, e.G., form, weakening, and stain, from pics. This text gives numerous convolutional neural machine prepare methodologies for consumption evaluation with appreciate to metallic surfaces. The impact of various shading regions, sliding window sizes, and convolutional neural device designs are examined. To this quit, the exhibition of two pretrained reducing aspect convolutional neural machine designs really as proposed convolutional neural gadget systems is classified, and it's miles confirmed that convolutional neural structures outflank wonderful in class vision-primarily based definitely consumption region movements closer to which is probably created dependent on ground and shading research utilising a primary multilayered perceptron prepare. Except, it is verified that one of the proposed convolutional neural structures essentially improves the computational time conversely with nice in elegance pretrained convolutional neural systems at the same time as preserving up comparable execution for intake discovery.

KEYWORDS: CNN, color spaces, neural network

1.INTRODUCTION

In tall shape maintenance, a huge goal is involved approximately the trustworthiness of the water supply framework and avoidance of water sullying. Forged iron is generally applied in water supply and waste removal frameworks due to the gain of excessive first-rate. Due to the fact hardened steel pipes frequently end up undesirable in residential pipework due to their immoderate prices [1], erosion is a typically watched form of essential harm.

Erosion (see discern 1) may be characterized as a substance process added approximately by the use of synthetic and electrochemical responses. .Is surprise is frequently seen in ecological situations along with an improved degree of dampness. .Ere are diverse varieties of intake, as an example, big erosion which happens as continually circulated nonprotective portions of rust and pitting that is a restrained purpose of unfavourable assault [2]. Intake achieves the pulverization of metallic pipework floor and consequently activates decrease in pipe control lifestyles and increment in building renovation value [3]. For positive scenario, this imperfection may moreover unequivocally have an effect on the strength of building tenants because of disintegration of water great. .Us, consumption must be recognized auspicious thru methods for infrequent overviews to assure the trustworthiness of channel frameworks and set up financially savvy aid methodologies.

In Vietnam absolutely as in numerous unique international locations, guide strategies achieved with the useful resource of human assessors are generally applied for circumstance appraisal of water supply/squander removal frameworks. As obviously referred to as interest to through Liu et al. [4] and Atha and Jahanshahi [5], these manual methodologies are work escalated and tedious. Eroded regions may be dismissed in places of funnel framework that are difficult to achieve and watch outwardly. Further, the procedures of records dealing with and revealing are likewise dreary for human professionals. .Erefore, there may be a all the way down to earth want to don't forget an increasingly gainful and actual approach for pipe situation assessment.

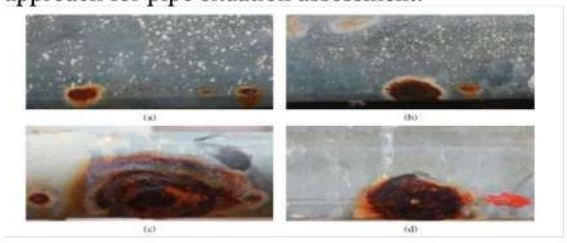

Figure 1: Corroded areas on pipe surface.

Real Time Minimum Energy Tracking Techniquies for Digital Load Circuit

Manjula N, Siva S Yellampalli

Abstract: Minimization of energy consumption is an important constraint in portable electronic devices such as smart phones or tablet PCs, laptops . With reliable energy measurement and estimation methods and tools, it is possible to accurate prediction of minimum energy consumption at different levels i.e., from circuit to architecture, architecture to system software and system software to application. Energy efficient design requires reducing energy dissipation in all stages of the design process without compromising the system performance and the quality of services..

Index Terms:, Energy efficient, Minimum energy Measurement, System performance..

I. INTRODUCTION

In modern digital integrated circuit design, one of the primary focuses of research is on energy efficient system. Energy efficient[1][10] is boardly defined as completing an application's workload at the lowest possible energy. The application are broken up into two general categories based on performance, high end application are:- servers, desktop computers and laptop computers. Low- end application:- portable media player[3], smart phone, tablets and bio-medical devices.The advance in technology is used to reduce energy consumption at different levels of abstraction by energy reduction techniques in the design flow, and the performance can be increased at each level of abstraction with additional functionalities. The various levels of abstraction are technological, circuit, logical and system level. Process and packing deals with technology level, routing and layout deals with circuit level. The logical level[2] is between the technological level and system level. encoding, clock gating and the use of parallel architecture, state-machines deals with logical level. The system level design which includes, partitioning, , algorithmic, power management, protocol design and programmable hardware, memory organizations which deals with connecting the resources in a correct functionally and efficient fashion.MEP is defined as the amount of energy consumed by a digital circuit at each per desired operation.

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II. DISSIPATION OF ENERGY

Digital circuit dissipates energy in two forms:-dynamic(E_d) and Statistic(E_s).

In general If N_{gate} to reverse logic gates, N_{turn} to accomplish number of times a task therefore E_d [4]can be equated as

$$E_d = N_{gate}\, N_{turn}\, C_L\, V^2_{dd}$$

C_L is the one logic gate of equivalent capacitance

Es can be expressed as

i) $V_{dd} > |V_{th}|$[4]

$$E_s = \frac{N^2_{gate} n_{bit}\, C_L\, I_o \exp(-v_{th}/nV_T)}{2k\mu\, C_{ox}\, W/L} \times V^2_{dd}/(V_{dd}-V_{th})^2$$

ii) $V_{dd} < |V_{th}|$[4]

$$E_s = N^2_{gate} n_{bit} C_L \times V^2_{dd}/\exp(V_{dd}/nV_T)$$

n_{bit} ⟶ bit number of the data
V_T ⟶ Thermal voltage.

$$E_t = E_d + E_s$$

The amount of energy dissipation in digital circuit is the sum of dynamic and statistic energy.

III ENERGY MEASUREMENT

Energy Measurement is defined as dynamic and leakage energy per operation. The charging of the internal load capacitance is the energy consumed[9] which is caused by the transistor switching is the dynamic energy.

$$E_{opdynamic}(V_{dd}) = C_L(V_{dd}) * V^2_{dd}$$

A small amount of quiescent current occurs in transistors due to this energy is consumed the consumed energy is the leakage energy.

$$E_{opleakage}(V_{dd}) = V_{dd} * I_L(V_{dd}) * t_{op}(V_{dd})$$

The consumed energy can be minimized in dynamic and leakage energy by reducing the supply voltage.

IV MINIMUM ENERGY MEASUREMENT TECHNIQUIES

Based on operating condition , technology, characteristics of the design. Minimum energy measurement techniquies can be classified as:

i) Dynamic voltage scaling

ii) Dynamic frequency scaling

iii) Dynamic voltage and frequency scaling

iv) Ultra dynamic voltage scaling

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A Novel Approach for Reconfiguring Dual-Mode Filter Based on Multilayer Structure

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Binary Sequences having Good Correlation and Large Linear Complexity Properties for Satellite Navigation Applications

**Dileep Dharmappa, Mahalinga V Mandi,
S. Ramesh**

Abstract: ***LFSR based binary sequences are known to have good correlation and better balance property and hence they are used in Satellite Navigation Applications as signature sequences. However, due to the code length requirements of length being multiple of on-board fundamental frequency 10.23MHz in GNSS systems, often the LFSR based codes have to be truncated (like 10230 bits). Due to the truncation the correlation property and the balance property gets degraded. Apart from the correlation and balance properties of the binary sequences the linear complexity property also plays an important role for GNSS applications where in users need to be protected against unintended or unauthorized access like commercial applications or military applications. In this work the balance property, even correlation, odd correlation and linear complexity property of the state of the art binary sequences of length 10230 bits being used for one of the GNSS system namely Galileo E5b-I primary sequences of length 10230 bits are evaluated. A method for generation of binary sequences having properties better than Galileo E5b-I primary sequences are presented. Binary sequences generated from the proposed method is analyzed for balance, linear complexity and correlation properties. It is found that the proposed sequences have better balance, correlation properties and high linear complexity. Due to the high linear complexity property, the proposed sequences provide inherent security for the system against spoofing and hence make the GNSS system secure.***

Keywords: ***Even Correlation, Odd Correlation, Linear Complexity, Chaotic Map, Binary Sequences, CDMA, GNSS.***

I. INTRODUCTION

Binary spreading sequences enable multiple services in Global Navigation Satellites Systems (GNSS) Systems. GNSS System namely Galileo is the European GNSS (GALILEO) which has completed its one year of the Initial Service during December 2017. The Galileo System is designed to provide better performance and accuracy for GNSS community than the similar systems such as, Global Positioning System (GPS) by US, Russians Global Navigation Satellite System (GLONASS) and Chinese BeiDou Navigation Satellite System (BEIDOU). The Initial services offered by Galileo include Open Service, Public Regulated Service (PRS) and Search and Rescue Service (SAR). Out of the four frequency bands being used by Galileo namely E5a, E5b, E6 and E1, the three bands E5a, E5b and E1 lie in the allocated spectrum for Aeronautical Radio Navigation Services (ARNS) towards providing dedicated safety critical applications for GNSS users.

The Galileo offers four types of services to GNSS community, namely Open Service (OS), Commercial Service (CS), Public Regulated Service (PRS) and Search and Rescue Service (SAR). In the frequency band E5b centered at 1207.14MHz, Galileo offers Open Service and Commercial Service using E5b-I Signal component (European GNSS Agency, Issue 1.3, December 2016). We present the primary spreading codes of length 10230 bits used for Galileo E5b-I are generated and their properties are analyzed.

Balance and correlation properties are important for open services, while for commercial services along with the above properties the linear complexity properties play an important role. Less linear complexity will lead to the detection of the CDMA code being used for communication in commercial applications. By detecting the CDMA code used in a commercial application there exists a possibility of spoofing which can lead to misleading information and is not easy to detect, hence binary sequences with high linear complexity finds applications in commercial GNSS applications.

Novelty of this work lies in the fact that the problem of conversion of real valued chaotic binary sequences is addressed. A method for conversion of binary sequences is provided in which the generated binary sequences retains the properties of the chaotic sequences. The generated binary sequences using the proposed method are found to be nonlinear and hence possess large linear complexity property. The generated sequences retain the odd and even correlation properties of the chaotic real valued sequences and hence the proposed sequences have better correlation properties both the odd correlation and even correlation properties as compared with LFSR based binary sequences. The results presented in this work are evident to prove the fact that the proposed method is novel in retaining the real valued chaotic sequences properties in the generated binary sequences.

Balance Property, Correlation Properties and Linear Complexity Property

Important properties for binary sequences used in CDMA namely correlation property, balance property and Linear Complexity property are defined in this section.

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Binary Sequences in Chaotic systems: A Review

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Abstract:

Chaotic systems have a number of interesting properties such as sensitivity on initial condition and system parameter, ergodicity and mixing (stretching and folding) properties, etc. These properties make the chaotic systems a worthy choice for constructing the cryptosystems as sensitivity to the initial condition/system parameter and mixing properties respectively are analogous to the confusion and diffusion properties of a good cryptosystem. In this paper we present a review of chaotic binary sequences using different chaotic maps like Logistic map, Tent map, Cubic map and coupled chaotic map and their suitability in cryptographic application systems.

Keywords: Chaotic maps, chaotic functions, spread spectrum communication, Code division multiple access.

1. INTRODUCTION

Chaos is characterized by deterministic nonlinear nonperiodic nonconverging and bounded behaviour. Chaotic sequence is an example of a discrete time continuous amplitude random sequence. The main characteristic of chaotic sequences is its sensitive dependence on initial conditions. Even if a small difference is introduced between the initial values, two chaotic sequences separate typically from each other after a short time period and are highly uncorrelated. Therefore, by using different initial values it is possible to produce a large number of chaotic sequences. One of the well-known one dimensional iterative maps which exhibits chaotic properties is logistic map which is regarded as a first order nonlinear recurrence equation over a real field.

Chaotic systems have a number of interesting properties such as sensitivity on initial condition and system parameter, ergodicity and mixing (stretching and folding) properties, etc. These properties make the chaotic systems a worthy choice for constructing the cryptosystems as sensitivity to the initial condition/system parameter and mixing properties respectively, are analogous to the confusion and diffusion properties of a good cryptosystem. In this article we present a review of chaotic binary sequences which possess the desirable properties for cryptographic applications. Some of the cryptographic applications in real time can be found in [1] to [10].

2. LITERATURE SURVEY

In this section we present a review of chaotic binary sequences in cryptographic applications and CDMA.

In [11], Narendra et.al. have discussed the concept of a random bit generator using chaotic maps. In this paper, the authors have proposed a new binary sequence generator called cross-coupled chaotic random bit generator (CCCBG) which exploits the interesting properties of a skew tent map. In the proposed CCCBG, authors have chosen two skew tent maps which are piecewise linear chaotic maps and cross-coupled. Using cross coupling, the authors show a forceful change in the behavior of both the chaotic maps regularly. By knowing the system parameter and initial conditions of one of chaotic maps, the behavior of CCCBG can be easily identified. The authors have used four statistical tests namely frequency test, Poker test, auto-correlation test and serial test on several large sized binary sequences generated by CCCBG to evaluate randomness and uniformity. The authors have also used NIST suite tests to evaluate the randomness of the bit streams generated by CCCBG.

In [12], Sukalyan Som et.al. have discussed RGB image encryption algorithm based on DNA coding and a chaos based pseudo random binary number generator. In this paper the authors have proposed an algorithm by scrambling the plain image using a generalized Arnold cat map in order to increase security. The scrambled image pixel is converted to DNA codes and again reconverted to integers where the choice of DNA coding rule is made pseudo random by the binary stream generated by chaos based PRBNG. The integers obtained after DNA coding and re-coding are diffused by performing exclusive OR operation with the integer sequences generated by 1D Logistic map producing the cipher image. The experimental results suggest that the proposed algorithm can successfully encrypt and decrypt RGB color images with secret keys. The simulation analysis shows that the proposed method is loss-less, secure and efficient. The authors have performed statistical tests like histogram analysis, correlation coefficient analysis, measures of central tendency and dispersion to authenticate their results.

In [13], Mahalinga V.Mandi et.al. have presented a new method of generation of chaotic discrete and binary sequences using Logistic map, Tent map and Cubic map. Normally in these schemes, cross correlation has a minimum value but not zero. If the number of users increases at a time, there is degradation in the quality of the received

A Fast convergence Modified VSSLMS algorithm for Smart antenna Beamforming

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Abstract— ***In today's world number of users increasing day by day for using mobiles. With the limited spectrum accommodating many users is difficult. SDMA technique will allocate user channels based on spatial separation reusing the same channel so bandwidth and capacity is hugely increased. In this paper a new innovative beamforming algorithm for smart antenna is used which makes use of modified variable step size least mean square algorithm (VSSLMS) in order to improve the convergence. In the previous approach of VSSLMS, the step size is varied in order to improve convergence, in proposed method along with variation of step size the speed increase module and convergence improve module block are used in order to execute alternative weights so that convergence is future improved.***

Keywords— ***Smart antenna, LMS, NLMS, Adaptive beam forming, VSSLMS, Modified VSSLMS, MATLAB.***

I. INTRODUCTION

As the numbers of mobile users are increasing day by day, the spectrum has limited capacity. Within the limited capacity huge number of users must be occupied which degrades the quality of service. Hence an algorithm is needed which can send the radiation towards the mobile users with the reduced error and convergence faster. An approach is needed which improve the radiation pattern as well as converges of the algorithm, so that main beam can be formed towards desired user at a faster rate as well as with more accuracy.

The aim of the algorithm is to form the main beam towards desired user and null or reduced radiation towards jammers using VSSLMS algorithm and also to improve the convergence capability of VSSLMS algorithm by using a novel four stage VSSLMS algorithm.

The convergence of the existing LMS algorithm is improved with the help of variable step size least means square method. The VSSLMS method will compute the step size dynamically so that the convergence is improved. The convergence can be further improved by making use of SM and CI module so that the speed of the weight computation is increased and then Algorithm will converge for about N/4 number of iterations so that it is huge improvement for beam forming algorithm.

II. RELATED WORK

The robust minimum variance [1] algorithm is a distortion less response (MVDR) beam former. The algorithm makes use of kalman filter which reduces the computational cost. Smart antenna [2] concepts are described which increases the capacity by directing the beam in different directions on the same frequency using Least Mean Square (LMS), Recursive Least Mean Square Algorithm (RLS), Normalized Least Mean Square (NLMS) and Sample Matrix Inverse (SMI).The smart antenna [3] algorithms will

Secured Electronic Voting System using Biometrics

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***Abstract*—In India voting procedure strictly follows the principle of electronic voting machine (EVM) which has simple design, reliability and fast accessing characteristics. Unfortunately, due to hardware problems in EVM's, malfunctioning officer's and illegitimate voter's invalid votes are being casted. This paper provides conceptual solution through multimodal biometrics which helps in enhancing security, eradicating the fraud and provides high level authentication. High accuracy is obtained by fusion of face and finger print recognition system.**

***Key words* — Electronic voting machine, multimodal biometrics, face recognition, finger print recognition**

I. INTRODUCTION

Voting has evolved over years [1] from purely manual process to more electronic means. The use of electronic devices in voting is known as electronic voting. According to electronic voting we should be able to ensure that authenticity of cast ballot can be verified and transaction should be untraceable.

Current voting system is based on a ballot machine where, when we press the button with the symbol the voting is done. Here there is a security risk, the person who votes may be fake person voting. The people there might not know that a person is using fake voting card, this may cause problems.

Electronic voting system security can be enhanced using Biometrics. Biometrics is the measurement and statistical analysis of a person's unique physical and behavioral characteristics. There are many techniques in biometrics like Face recognition, Finger print, iris recognition, hand geometry, palm veins, palm print etc.

In this technique, Face recognition and Finger print is used. A facial recognition is a biometric method of identification of an individual by comparing live capture or digital image data with the stored image data for that person. Finger print recognition refers to the method of identification and confirmation of the identity of a person based on comparison of two Finger prints (finger print in database and sensed finger print) and used for authenticating in computerized systems.

II. EXISTING VOTING SYSTEM

The existing voting procedure follows the principle of electronic voting machine (EVM) which has simple design, reliability and fast accessing characteristics. Unfortunately, due to hardware problems in EVM's, malfunctioning officer's and illegitimate voter's invalid votes are being casted, and the same person can vote multiple times. Voting system must provide results quickly, but existing voting system takes much time to produce the result.

In unimodal biometrics like Finger print has many draw backs like the Finger print will be taken with which the dirt inthe Finger, greases and other contaminated content will be recorded and there will be chances of finger print getting rejected. When the person has some marks on the finger or if he has cut on his finger the person will be considered an invalid voter [2].

This paper provides the conceptual solution for fraud voting procedure through multimodal biometrics which helps in enhancing the security, eradicating the fraud which provides high level authentication and consumes less time to provide results. Multi model biometrics is the fusion of two or more types of biometrics. High accuracy will be achieved by fusion of Face and Finger print recognition systems compared to present EVM system.

III. PROPOSED /PROTOTYPE DESIGN

The proposed EVM system has two inputs, one of the inputs is Face image and another is Finger print. Initially, in the Face recognition part, web camera captures the face image and it is processed as shown in figure. 1. The face region will be detected using the Viola and Jones algorithm[3], which contains three types which are Haar-like feature[4][5], AdaBoost and Cascading. The face features are extracted from the detected face image using HOG algorithm. The HOG algorithm[6][7] consists of two methods they are Intensity based method and Feature based method. Intensity based method is used to extract the face intensity features and feature based method is used to extract the magnitude and angle of face.

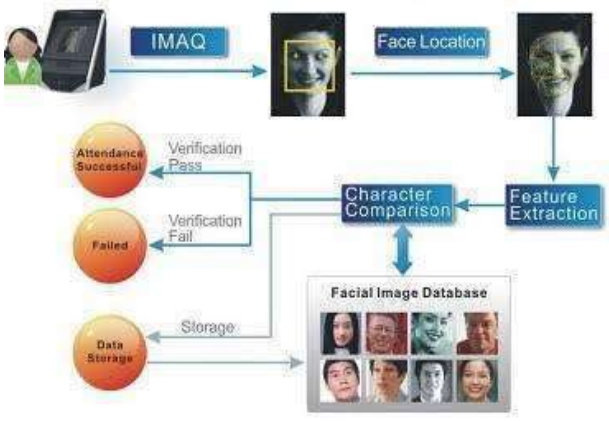

Fig.1. Face recognition verification process

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Human action recognition using fusion of features for unconstrained video sequences

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ABSTRACT

Effective modeling of the human action using different features is a critical task for human action recognition; hence, the fusion of features concept has been used in our proposed work. By fusing several modalities, features, or classifier decision scores, we present six different fusion models inspired by the early fusion schemes, late fusion schemes, and intermediate fusion schemes. In the first two models, we have utilized early fusion technique. The third and fourth models exploit intermediate fusion techniques. In the fourth model, we confront a kernel-based fusion scheme, which takes advantage of kernel basis of classifiers i.e. Support Vector Machine (SVM). In the fifth and sixth models, we have demonstrated late fusion techniques. The performance of all models is evaluated with ASLAN and UCF11 benchmark dataset of action videos. We obtained significant improvements with the proposed fusion schemes relative to the usual fusion schemes relative state-of-the-art methods.

1. Introduction

In the field of computer vision, a substantial amount of work has been dealt with spatial pattern recognition that involves extracting and identifying objects of interest from video sequences. However, by adding temporal expression, the power of the camera can be drastically increased and used to solve a huge variety of very composite and complex problems. Action recognition refers to an algorithm that the computer system uses to automatically recognize what human action is being or was performed, in a given video sequence. Over the last decade, action recognition has become a crucial research domain for many applications in computer vision field. Actually, it is the problem of classifying an action and assigning it a label of action class. Detecting action performed by humans using camera has a large impact in the industry domain; when a human performs action, his/her body goes through signature movement of body parts. To detect this movement and hence the action performed, computer science researcher needs to design a video system. Most of the recent research works done on action recognition are focused on videos, which are having different constraints, and hence performing action recognition on this video is a challenging task. Recently, these types of video benchmark dataset are released for action video performed by one or more than a human. Still, there is far more distance between the current progress work and real-time action

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HF Radar Signal Processing Algorithms for Air and Surface Target Detection

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***Abstract*—The well-known conventional microwave radars presently in use are efficient in target detection and tracking of targets at a few hundred kilometers range. The basic limitation of conventional radar systems operating at microwave frequencies is that the range coverage is restricted to regions where a line-of-sight (LOS) path exists between radar and target. The curvature of the Earth limits the microwave radar to distances that do not extend beyond the geometrical horizon. This distance may further be shortened due to topographical features such as mountains. Hence to overcome this limitation of microwave radars, we can use High Frequency (HF) radars which use the ionosphere for reflection of signals and detection of targets at distances beyond the line-of-sight or the geometrical horizon. In this paper we give an insight to the concept of HF radars, their working principle, and how they can replace the microwave radars in various fields.**

***Keywords*— Range, Doppler, Resolution, Clutter, Dwell Time, LOS (line-of-sight), DFT (Discrete Fourier Transform), high frequency;**

I. INTRODUCTION

The fundamental limitation of conventional radar systems operating at microwave frequencies is that the range coverage is nominally restricted to regions where line-of-sight (LOS) path exist between radar and target. Coverage may be restricted to much shorter ranges when topographical features such as mountains, shadow targets from radar illumination. Sometimes, microwave radars are prone to meteorological effects, like rain or hail, which has the potential to reduce target visibility due to weather clutter and increase signal attenuation, leading to poor performance.The HF radar overcomes the aforementioned limitations of conventionalmicrowave radar. The HF radar operates in the high frequency range (3-30MHz). An important property of HF band is the unique ability of HF signals to propagate over very long distances and illuminate the earth's surface well beyond the horizon. HF radar systems find application in early-warning wide-area surveillance and remote sensing. The targets maybe airborne (such as ballistic missiles, helicopters, military aircrafts, private aircraft and large commercial airlines) or could be surface targets (like patrol boats, cruisers, destroyers and aircraft carriers). Microwave radars also find application in similar areas such as surveillance functions, target detection, localization and tracking, and track-while-scan. Microwave radars differ from HF radars in providing early-warning at better resolution and accuracy.

II. HF RADAR

A. Signal Environment

A HF radar receives a mixture of different signals. The Signal Environment for HF radar is classified as shown in figure. Radar echoes are the signals received by radar due to echoes of the transmitted radar waveforms. Interference and noise come from other sources independent of the radar. Radar echoes are further subdivided into target echoes and clutter returns. Target echoes are commonly referred to as useful signals or desired signals. Unwanted echoes from other objects are referred to as clutter. In HF radar, clutter mainly arises due to backscatter from large areas of earth's surface (terrain or sea). External interference and noise may originate from natural or man-made sources.

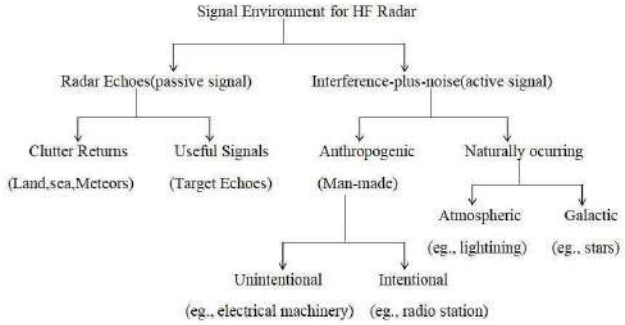

Fig 1.1 Signal Environment flow diagram for HF radar

In HF band, the main sources of natural noise include lightning and discharges, and galactic noise from sun and other stars. Man-made signals may be further subdivided as either originating from intentional and unintentional radiators. Intentional radiation includes short-wave radio broadcasts, point-to-point communication links, potentially jamming. Unintentional radiation may arise from industrial machinery and other electrical equipment. The sum of clutter, interference, and noise represents the composite disturbances that the radar echoes must compete with.

B. Principle of Operation of a HF Radar

HF Radars operate in the 3-30 MHz range of frequency. They use the ionosphere for the reflection of signals, which allows them to map ranges between 1000 to 3000 kms. Askywave HF Radar operates as follows:

Design of MMIC Class-E Power Amplifier with Adaptive Bias Control and Built-in Linearizer Using 0.5 µm pHEMT Technology

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Abstract— A new topology of Class-E power amplifier at 1.9 GHz designed and implemented using 0.5 µm GaAs pHEMT technology. The design adapts a built-in linearizer and adaptive bias control circuit which resulted with better linearity and Output power at 1 dB compression point(OP@1 dB). Two stage class-E amplifier with linear-mode pHEMT in the input bias circuit results in PAE of 89% at 1.9 GHz with output power (OP@1dB) of 21.5 dBm. The Third order intermodulation (IMD3) suppression of proposed Adaptive bias Class-E power amplifier with linear mode pHEMT in the input bias circuit is 52 dBc and it is 7 dBc higher compared to Class-E Power amplifier with pHEMT linearizer. It also results in 5% improvement in output power at 1 dB compression point (OP@1 dB) compared to Class-E power amplifier. The proposed PA incorporated with adaptive bias and built-in Linearizer using 0.5 µm GaAs pHEMT technology in PCS frequency band gives 40 dBc improvement in IMD3 compared to basic Class E power amplifier.

1. INTRODUCTION

The development in modern Wireless communication technology brings several challenges in order to provide higher datarate and wider coverage capabilities. It demands for high performance designs with low power consumption and low cost. The impact in battery life of a mobile handset is brought by higher PA efficiency, thus efforts are put on to implement efficient and linear PAs. Highly Linear Power amplifiers are required for recent mobile standards with non-constant envelope modulation schemes. The Class E amplifiers are switching amplifiers, highly efficient [1] in which the active device (transistor) works as a switch, such that voltage and current at the output of the active device are out of phase. To satisfy the linearity requirements of MMIC PA with available power,many linearization techniques are introduced and studied. Predistortion Technique is considered as better solution to improve the linearity of PA [2–5]. A high power HBT PA with active bias linearizer is discussed with a PAE of 21% at output power of 16 dBm in IS-95 systems [2]. The AlGaN/GaN HEMT microwave class-F amplifier uses a novel pre-distortion technique with two Schottky diodes which are independently bias controlled to provide compensation of nonlinearity [3]. Different configurations of predistorter circuits with diodes and MOSFETs provides a flat gain for UWB applications [4]. Enhancement of Linearity is achieved with improvement of IMD of 15 dB and adjacent channel power ratio of 7dB in case of QPSK modulation in a MMIC with built in HEMT linearizers at 44 GHz [5]. A new technique for PA design is discussed with adaptive bias and linearizer resulted in appreciable linearity with efficiency using 0.18 µm CMOS process [6].

2. CLASS-E POWER AMPLIFIER DESIGN

The load network of Class E amplifier is designed using reactance compensation principle to achieve wider bandwidth. The load network of Class-E consists of shunt and series reactance elements. The active device in class-E configuration acts as a switch which is driven by the driver stage to provide switching of the transistor between its on-state and off-state operating conditions. The Series and shunt resonance circuits vary exactly opposite to each other around the resonant frequency which reduces the overall reactance slope of the circuit. Due to this, there is a constant load angle over a wide bandwidth of operation.The single reactance compensation circuit in Class-E power amplifier is shown in Figure 1.

The admittance of the reactance compensation circuit is as shown in Equation (1),

$$Y_{in} = \left(j\omega C + \frac{1}{j\omega L} + \frac{1}{R + j\omega' L_0} \right) \tag{1}$$

where,

$$\omega' = \omega \left(1 - \frac{\omega_0^2}{\omega^2} \right) \tag{2}$$

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Trajectory Tracking of locomotive Using IMM-Based Robust Hybrid Control Algorithm

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Abstract: Locomotive surveillance is the most active research topic and still faces big technical challenges in railway safety control system. An end-to-end locomotive tracking and continuous monitoring system is necessary for safety measures in satellite visible and low satellite visible environment. These smart systems aim to updates the information on location, exact detection, speed limitation and also rail track information. This paper contributes to develop an intelligent tracking and monitoring system based on Internet of Things (IoT) platform using Differential Global Positioning System (DGPS) for improved tracking accuracy of locomotive in both environments. Interacting Multiple Model (IMM) tracking algorithm based on Di-filter model is proposed for analysis that make it easy to pinpoint the location and its status of the locomotive.

Keywords: DGPS, Di-filter, IMM Algorithm, Model Matching, Tracking Surveillance Model

1. Introduction

Many real world applications managed in military and civilian require accurate tracking of moving targets acquired by sensors. In military applications, tracking is continuously updated the performance of target's position and also tracking of enemy vehicles so that they are blocked and destroyed immediately [1]. In civilian applications target tracking is of much use in autonomous vehicles, home security etc. Accurate target tracking is used in many situations to accommodate the need for constant human help and thus it is simple to achieve much higher degree of intelligent, wireless and automatic [2]. There is loads of real time application for locomotive tracking and monitoring using satellite based navigation system with high level of speed and precision. These systems are more accurate, precise, efficient, low cost and less economic maintenance. But in poor satellite visible areas such as mountains, tunnel, valleys, deep cuttings etc. they are facing many service failure issues [3].

Land vehicle navigation technologies mainly depend on the Global Positioning System (GPS). The user platform mainly based on receiver which receives the radio signals from four or more satellites provides the position and velocity information. In spite of diverse application of GPS, the flexibility of service is still limited as the GPS based tracking accuracy is decreases when it passes through poor satellite visible areas such as tunnel, mountain, forest, slope, bridge, urban or canopy areas due to signal failure and attenuation [4, 6]. Different locations have affected by different atmosphere factors which vary with locations and these errors are corrected by Differential GPS. The most enhanced version of Global Positioning System is Differential Global positioning System (DGPS) [8]. It provides precise and improved location tracking accuracy than GPS. It increases the tracking accuracy of the target locations or the coordinates which are derived from the GPS receivers. For improvement in tracking accuracy and monitoring the integrity of GPS satellite radio transmissions, it provides differential correction to GPS receiver. With DGPS receivers, the position tracking accuracy is improved from 30m to better than 2m.

The performance of a tracking system is depending on the performance of the state estimation algorithm employed. In tracking system, accurate state estimation of targets is required for reliable data association and correlation [11].

Automated Border Security System

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Automated Border Security System

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Abstract— It is challenging for the soldiers to continuously monitor Illegal movements across the border due to extreme weather condition such as high temperature regions above 50o Celsius or low temperature regions with less than 0o Celsius. Soldiers survive under such conditions with extra wearing which makes them uncomfortable. Therefore the proposed project work substitutes the security monitoring soldiers with an automated security system. The proposed project consists of four IR and PIR sensors to detect both living and non-living bodies around 360o which intimates the soldiers about illegal entry and a stepper motor controlled gun which triggers when any one of these IR sensors detects any movement. The proposed system also consists of harmful gas detection unit. This project could enhance the border security electronically with automation and also reduce the work load of the soldiers to monitor the border 24*7.

Key words: Border Security, IR and PIR Sensors

I. INTRODUCTION

In the countries like India, soldiers cannot be present at every part of the border due to the long stretch and huge climatic changes such as Siachen, the world's highest battlefield, where the temperature rapidly changes causing avalanches causing many soldiers to die. This has affected the induction and de-induction of troops. However an automatic border security system can avoid the loss of several soldiers' lives. Currently there is no automatic weapon shooting system, expect in USA military they developed a sniper gun which aim, lock the target and automatically shoot, but the disadvantage being that the gun should be hold by person, by movable trigger pointer it aim and shoot. So even there is human intervention. This problem can be overcome by the proposed work, where automatic gun is placed on a controlled base, which can be adjusted in 360° by using stepper motors.

Many papers have been published on the related topics. Authors Tanmoy Maity, Mithun Mukherjee in [1] have proposed mine detecting robot with multiple sensors which can replace human workers in such complex environments as special places of coal mines, undesirable conditions inaccessible to humans or disasters of fire, earthquake, and mining. Authors A.G.Barrientos, J.C.G.Vidal, E.S.E.Quesada, J.P.O.Oliver, F.R.T.Macotela and M.O.Domínguez in [2] concentrated the architecture of a minesweeping robot which is designed and implemented as a research project.Authors X. Ma, Y. Miao, Z. Zhao, H. Zhang, J. Zhang in [3] have discussed the design of a micro-controller based fuzzy logic controller for a remote-controlled mine detecting robot. Authors Zhenjun He, Jiang Zhang, PengXu, Jiaheng Qin and Yunkai Zhu in [4] proposed the establishment and realization of an autonomous biped robot with object tracking function. Author Reza Abbaspour in [5] remote area. Authors Karthikeyan.A, Sarathkumar.V in [6] discussed the multimedia sensor based robot that gives images and sensor data of the environment

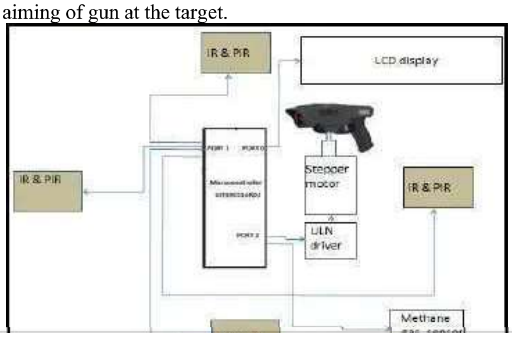
The objective of our work is to integrate IR sensors and PIR sensors to sense the movement of humans, to design harmful gas sensor to sense the harmful gas and to design the stepper motor to rotate in 360 degree rotation. This can be modelled by programming a microcontroller to receive signal from IR and PIR sensor, and send the signal to stepper motor. An active high signal from the Gas sensor is taken as a harmful gas is sensed and turns on the buzzer through relay. Microcontroller is programmed to rotate the base of the gun 90° for signal from one IR-PIR pair, so total 360 degree rotation can be covered by 4 IR and PIR sensor pairs.

The rest of this paper is organized as follows. Section 2 deals with the details related to design of proposed system and Section 3 deals with implementation of proposed design. In Section 4 we analyze results of the implemented system. Finally, we conclude this work in Section 5.

II. DESIGN

Here we are designing a prototype of the proposed project. When implemented in real time, the design of sensors cost will be comparatively high and also accuracy will be very high, which aims at tracking target more precisely and should be enclosed within a well-defined casein to withstand advert environmental conditions.

The Fig 1 shows the block diagram of the prototype of the proposed Automated Border Security System which senses the Intruders, trespassers and shoots automatically by aiming at the target. As it could be seen the proposed prototype is made up of 4 pairs of IR and PIR Sensors which senses any intruders or trespassers and will activate the laser gun which aims at the target and automatically triggers the gun. The 4 pairs of IR and PIR Sensors are helpful in monitoring trace passers around 360°. The automatic gun is positioned on a Step-motor controlled base which helps in aiming of gun at the target.



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FPGA Implementation of AHB to APB Protocol

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Abstract:*The field of technology is evolving at a very fast pace. The competition is very intense. So the need of the hour is to produce efficient system. In accomplishing this objective we are required to establish better interaction among all the components of the system. This requirement is fulfilled by the Advanced Microcontroller Bus Architecture (AMBA) protocol from Advanced RISC Machines (ARM).The AMBA is the on-chip standard for the communication among components in Application Specific Integrated Circuits (ASIC) or System on Chip (SoC). This paper focuses on the 2 protocols of AMBA which are Advanced High Performance Bus (AHB) and Advanced Peripheral Bus (APB) and theAPB bridge. The coding is done in Verilog synthesis on Xilinx 14.7 ISE and simulation on ISim simulator and FPGA implementation on Spartan 3.*

Keywords: AMBA; APB bridge, AHB, APB, IP, SoC, Verilog ,VLSI

1. Introduction

The miniaturization in the technology is leading to the emphasizing on the communication among the modules of the System on Chip (SoC). The SoC is the integration of all the components required onto the same chip so called System on Chip. The interaction between these components of the system is critical for every SoC. The intercommunication is maintained by AMBA protocol. The AMBA protocol provides an efficient way for the interaction and increases the performance of the system.

In figure 1 the components like Direct Memory Access (DMA), Random Access Memory (RAM), External Memory Interface, ARM processor are the components in SoC and the peripheral components like Universal Asynchronous Receiver Transmitter (UART), Timer, Keypad, Programmable Input Output (PIO). The communication here is established by AHB on the master side and by APB for the peripheral side. The bridge provides the interconnection between AHB to APB.

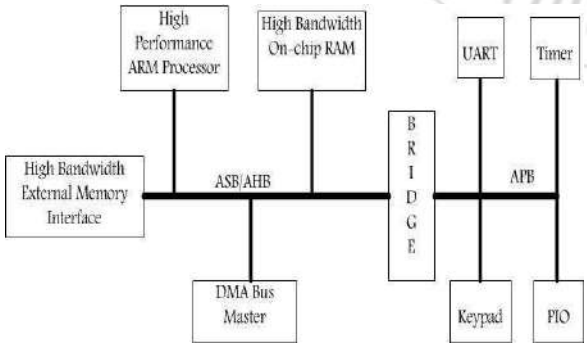

Figure 1: Communication established by AMBA

2. Related Work

The paper [1] describes the design of AHB to APB module. It describes the AHB module and the designing of AHB to APB Bridge. The coding is done in Verilog. Here the AHB monitor or driver is designed. The paperexplains only on the RTL simulation and is not implemented on FPGA.

The paper [2] describes about the APB protocol its comparison with AHB and ASB. The paper explains the state diagram of APB and describes the signals required for the APB and the coding is done in Verilog. The paper explains only about APB protocol and is good for understanding APB protocol.

The paper [3] describes about the AHB module and is coded in VHDL. The AHB signals are learnt and design of AHB arbiter is understood. The AHB module can be understood for implementation with the aid of this paper.

The paper [4] describes how an efficient Finite State Machine (FSM) for the AHB master with the understanding of the various signals of AHB master can be designed. The operation of AHB master is required for the designing an efficient FSM and thus the AHB master. The AHB module can only be designed.

The paper [5] describes the design of AHB arbiter with the emphasis on AHB arbiter architecture. The arbiter logic is explained. The paper basically is for design of arbiter for AHB in Verilog.

The paper [6] describes the design of incrementing burst transfer for AHB high performance. In this paper the focus is on the burst transfers and its capability of extracting high performance from AHB. The paper uses Verilog for coding AHB burst performance.

The paper [7] compares between the AMBA bus protocols of its version 2.0 that are AHB, ASB and APB. The comparison is based on their application to performance. The paper highlights the different buses and the features of the buses.

The paper [8] describes the design of AHB to APB module for different frequencies and phase. The paper explains the design of AHB to APB and their performance for different frequencies. The paper explains the design and helps in understanding of the interface between two protocols.

The paper [9] describes the performance comparison between various versions of AMBA protocols.

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A Novel Evolving Mutation Analysis approach of Hybrid Parallel Ant Colony Optimization algorithm for DICOM images

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Abstract

The information contained in a DICOM image is very crucial for telemedicine, tele-radiology and other medical diagnosis and prognostic applications. In the field of medical transcription there have been various techniques in detecting the edge of an image. In most of the computer vision systems, DICOM image is considered as a standard digital imaging process of storing, capturing and transmitting the required medical information of an individual. The meta-heuristic process used in detecting the edge of an image, topologically, while the evolving non-deterministic behavior, stochastically, is to be addressed through a natural selection process. In this paper we propose a hybrid genetic algorithm coupled with effective parallelism topology based Ant Colony Optimization (ACO) and Hamilton's rule for evolutionary scenarios. The initial analysis of the algorithm showed an appreciated performance in handling the dynamic attributes of the DICOM images. This is successively enhanced with the parallelism topology, as multi-processor environment is considered which has shown an improved speed and efficiency.

Keywords: Edge detection, ACO, Hybrid PACO, Mutation Analysis, As Built Critical Path (ABCP), Genetic Algorithm, Evolution

INTRODUCTION

The medical standard digital imaging paradigm, DICOM befits a best fitting solution for the paradox in image edge detection. Many algorithms and techniques were proposed for computer vision systems, for this essential analysis application. The process of detecting an edge of an image yields ample amount of data at a reduced rate. The quantification of the evolving image data, specifically among the DICOM standard medical images, the need for an enhanced performance in rendering the solution is necessary. This was duly addressed by the proposal of an enhanced, hybrid effective parallelism topology for ACO algorithm with critical Path methodology by Chetan S et al. [2]. This technique takes into consideration the very essential factors of heterogeneous computation techniques and algorithms in solving the NP-hard scenarios as addressed by Chetan S et al. [1]. Increasing complexities in the paramount metrics within DICOM medical images, their data, intensity variations around the local region and its integrity & restructuring relating to the edge of an image are integrated parts of edge detection. In all these handling and processing of medical images and its derivatives & standards are real hard tasks. These kind of images are dynamically low contrast, complex to analyze and discontinuous with intensity variations. The advanced qualifying value of evolution, to be evaluated, was prominently provided by Hamilton rule [3]. The social behavior exhibited, is synthesized with the purview of this behavior as a genetically cohered issue.

The genetic evolution being considered as a fundamental and enduring problem for which various quantitative tests have been quantified manipulations justified by the equation, as given in [4],

$$rb - c > 0$$

r – genetic relatedness

c – fitness cost of PACO-CPM edge detection algorithm

b – fitness benefit for the heuristic behavior of the ants and the evolving feature of the DICOM image

This befitting solution shows that the behavior of the ants in the ACO algorithm, even though resolves the metaheuristic

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A Heterogeneous Access Remote Integrating Surveillance Heuristic Model for a Moving Train in Tunnel

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***Abstract*—**Many number of real time applications are available for train monitoring using satellite based navigation system with high level of speed and precision. But these systems have faced lot of issues such as multipath loss and line of sight which results in lesser accuracy measurements. When the train is moving in low satellite visible areas such as tunnels, mountains, forest etc, then no position information is available. The service failure in tunnel made big challenge to demonstrate a self supporting innovative platform for navigation of train. This paper is focused on designing a novel approach by integrating Wireless Sensor Network (WSN) and Radio Frequency Identification (RFID) system for continuous monitoring of train moving in tunnel. The wireless tracking controller based on quadratic optimal control theory is considering for analysis. Overall performance of the control design is based on Liapunov approach, where quadratic performance index is directly related to Liapunov functions. By minimizing and maximizing the performance index value corresponding to control inputs will trace the tracking error inaccuracies. As maximizing the performance index, the tracking error produces 0.04% inaccuracy. The data loss is 0.06% when minimizing the performance value. Simulation is carried out using Mat lab.

***Index Terms*—**WSN, RFID, Surveillance Integration model, Quadratic Optimal Control.

I. Introduction

The train tracking, controlling and monitoring system is an emerging technology in the rail sector. In minimum budget railways, the reliability, accuracy, driver assistance, cost efficient technique, availability and integrity are the major factor. The signaling of train and rail traffic play significant role in the wireless communication solution. Real time information of the train movement in satellite visible areas are acquired from satellite based positioning system [1] [2].These systems are more accurate, precise, efficient, low cost and less economic maintenance. But line of sight between transmitter and receiver as well as multipath loss in the low satellite visible areas such as mountains, tunnel, valleys, deep cuttings etc. completely shadowing information. The navigation information cannot be relay completely on the basis of satellite based positioning systems alone [3]. Some of the expensive surveying technique such as unmanned aerial vehicle surveillance, interferometric synthetic aperture radar, laser scanning can also be used to acquire the geographical data. But these systems are highly restricted with cost, area and duration. The above explained factors enable us to focus on designing sensor based technology. The integration of satellite based navigation system with sensor technology can bring communication diversity [4][5] This paper attempts to build useful approach by integrating Wireless Sensor Network with Radio Frequency Identification system. The sensor network supply us general navigation data where as RFID gives precision information near the targeted object.

Nowadays the use of WSN has been adopted in many applications such as surveillance, measurement of temperature, humidity and other environmental parameters, building maintenance, pollution monitoring etc. WSN technology is very useful for autonomous sensor data collection process. It is a group of heterogeneous sensor nodes capable of sensing, identifying, positioning the objects to monitor and control in distributed manners [6]. In our research it is employed to monitor the rail and its surrounding environment with sensing function rather than identifying the train. To overcome this limitation, RFID is the best choice because it detects and identifies the moving train with precise navigation. By integrating two important wireless technologies like WSN-RFID, it is possible to improve sensing capacity as well as navigation system even more [7]. This is fully automated wireless model located on moving train to provide train's location, speed, velocity and other parameters. The fused information from sensors is expected to improve the train detection and tracking accuracy in tunnel. One major objective of the fusion technology referred is mainly because each

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Performance Analysis of Multi-Source Data Fusion Tracking Algorithm for Ground Based Surveillance Model to Monitor the Moving Locomotive

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Abstract: *Multi source data fusion has an emerging technology that received core attraction for maneuvering and non-maneuvering application. Data fusion observation has improved reliability and it could be easy for the user to detect, recognize and identify the targets and increase user's situational awareness. The fused data should preserve all relevant information contained in the source data .Based on current trend of data fusion process, this paper presents a novel methodology to increase tracking accuracy of locomotive using Square Root Information Filter Algorithm (SRIFA).The tracking algorithm at decision level fusion, merges the information of Differential Global Positioning System (DGPS) and Wireless Sensors. The simulation results clearly shows the tracking accuracy that provide by multi-source data fusion process better than could be provide by single source alone.*

Keyword: *Ground based surveillance mod; DGPS; WSN; Data fusion; Information Filter; SRIFA;*

1. INTRODUCTION

In an intelligent vehicle system, the development of sensor technology and signal processing methodology plays major role in modern technology. The multi-source data fusion system is combining data from multiple sources to achieve significant accuracies results than using single source alone [1]. By using more advanced signal processing technique and data fusion process gives contribution towards multi sensor data fusion concept. The main application of multi sensor data fusion are automated target tracking, remote sensing, battlefield surveillance, guidance and control of autonomous vehicles, smart building, robotics and medical application [2]. The principle process of data fusion involves Identity fusion, data level fusion, and decision level fusion. The decision level fusion follows the merging information from multiple algorithms performed by multiple sources to yield resultant fused decision [4].

The current paper explains the fusion tracking algorithm for moving locomotives. The locomotive tracking is observed by Differential Global Positioning System (DGPS) measurements. The DGPS provides the ability to determine accurately the locomotive's location in the satellite visible area, but has limited ability to determine the location of the moving locomotive in the tunnel. By contrast, the Wireless Sensor can accurately determine the location even in tunnel, but is unable to measure the range. If these two calculations are correctly matched, then the combination of these data supplies more improved version for determination of location than could be obtained by single source alone [7]. We will focus on two types of situations for the fusion. (a) Fusion of location data to determine the position and velocity of moving train in satellite visible areas; Kalman filter based algorithm is applied. (b) Fusion of location data to determine the kinematics of moving train in tunnel, Quadratic Optimal Control algorithm is used for analysis.

In filtering the modified processing of measurements values, the computation of coefficients smoothing, the accumulation of the results are taking place. The Information Filter is advanced version of the discrete-time Kalman filter. The state estimates and the estimation covariance in Kalman filter are replaced by the information matrices and information vector [8]. Information filter is one of the best methods to deal with multi-source data fusion problems. It has special advantage in supplying direct

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The Impact of Hybrid Data Fusion Based on Probabilistic Detection Identification Model for Intelligent Rail Communication Highway

Tanuja P. Patgar[1] and Shankaraiah[2]

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Abstract

Data fusion has an emerging technology that received core attraction for maneuvering and non-maneuvering application. The multiple sources in the data fusion process are distributed accuracy based systems that differ from traditional single source in many ways; these have suppressed the irrelevant data and noise, better numerical precision, reliable, stable and accurate. The end-to-end basic probabilistic models have been proposed for different architectures in data fusion to manage sensor information. This paper proposes probabilistic detection identification model based on Bayes theorem and compare its performance with traditional single source network. Subsequently, it is cross validated using various data folds of kinematics measurements available from Differential GPS, Wireless Sensor and Radio Frequency Identification. This study proves the probabilistic model offers significant detection performance accuracy level of 95% for moving locomotives across wide range of operational scenarios.

Key words: *Data fusion, Bayes theorem, Probability identification model*

1. Introduction

Data fusion technology is of highly special significance in multiple real time application where group of data are combined, fused and modify to generate data information of appropriate quality. It is the process of combing information from multiple similar or dissimilar sources to provide robust and complete description of an environment or process of interest [1]. It finds many applications in military systems, in civilian surveillance and monitoring targets, in autonomous and process control system etc. The principle process of data fusion involves Identity fusion, data level fusion, and decision level fusion. The decision level fusion follows the merging information from multiple algorithms performed by multiple sources to yield resultant fused decision [2]. There are many constraints that need to be coined in order to achieve re-implementation of certain technological enhancement of the current system. The maximum extent to get better result numerical precision, reliable, stable and accuracy are to be considered. For such reason the data fusion methods are preferably considered in the drive toward autonomous systems. In principle, automated data fusion processes allow required measurements and information are to be combined to give knowledge of sufficient precision and integrity that problem may be formulated and executed autonomously [3].

The most important problem in data fusion technology is the development of sensor models associated with both the state and observation process. The focus is highlight on the use of probabilistic and information-theoretic methods for sensor modeling and for data fusion. Probability theory provides an extensive and unified set of methods for describing and manipulating uncertainty. It explains clearly how basic probability models can be used to fuse information, to describe different architectures for data fusion and to

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Design of Fixed One-Bit Latency Serdes Transceiver

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[3] *Professor, UTL VTU Extension center, Bengaluru, Karnataka, India.*

Abstract- *Today's communication world experiences a maximum amount of problems linked with serial interconnects since they occupy the entire communication field, therefore the serializer/deserializer (SerDes) devices make huge changes in the market with large differences in cost and performance. But they fail to maintain constant communication latency throughout the transmission after each reset or power up. In this paper a fixed one bit latency serdes transceiver is proposed which is built using delay tuning and phase shifting technologies. It overcomes the shortcomings of buffering and delays generated by clocks. A specific implementation based on Xilinx Spartan 6 FPGA is presented in this paper. The results indicate that the device achieves a constant latency with improvements in buffering each time after reset.*

Key words: - Changeable Delay Tuning, Dynamic clock phase shifting, fixed one bit latency, FPGA, Serializer/deserializer.

I. INTRODUCTION

Serializer/Deserializer devices embedded in the GTP transceivers though seem to be much advantageous in the field of communication for their high speed transfer capabilities, face much problems when they undergo processes like reset, relock and when powered up.[1] In order to overcome these problems a solution in the form of designing an external dedicated circuitry was introduced. But this design was not actually needed for telecom and Datacom communications. However today's SerDes Devices replace the parallel connectors due to their high speed multi gigabit transfers because of the huge developments involved in bandwidths.Serdeses today are not only meant for their high speeds alone but show great improvements in device parameters like information formatting ,device topology, protocol overheads etc.Serdeses are also associated with maintaining clocking, timing ,latencies, buffering and logic which increased their cost and performance parameters linked to data acquisition and manipulation.[2] The problem associated with the serdes chips is that they do not actually maintain the same latency after few operations like reset, power up and relock.[1],[2]. Therefore a need for extra circuitry had to be implemented in the presently used transceivers in GTP in order to overcome the problem to improve the parameters linked with communication overhead.[3] Therefore an extra circuitry named as clock and data slider block is designed and implemented in the present work. The principle goal is layout of a fixed one bit latency serial transceiver based on delay tuning which is changeable and phase transfer of clock technology. As compared with the roulette approach it processes all clock phase offsets produced in serializing and parallelizing conversion. Subsequently, it removes out the reset-relock crisis. [7]

This paper stresses on usage of a rigid and fast serial transceiver designed on the principle of changeable delay tuning and dynamic clock phase shifting technologies. It facilitates to overcome all the problems posed by buffering and clocking mechanisms involved for transmissions with the development of phase offset values between the clocks of the transmitter and receiver. It also focuses in removing out the reset-relock problem.[1] This paper speaks approximately excessive-speed, constant-latency serial links in dispensed information acquisition and manipulation structures, inclusive of the timing trigger and control (TTC) device for excessive energy physics experiments.[2] This paper describe how to make use of the inner alignment circuit of the SerDes transceivers to put off the clock phase offset, which results in a variation in connection latency.[3] This paper speaks approximately of utilizing source and data acquisition for transfer of data. It focuses on implementing a high speed transceiver in FPGAs with a clocking scheme and two configurations. It pressurizes on implementing pipelining mechanism for the serial link to improve the latency and performance.[4] This paper stress on a vast development in the field of radiation tolerance, limited area for hardware, and synchronization mechanism.CBM network protocol uses fiber connection which is bidirectional and single ended to achieve good latency and synchronization and thus helping to build a new network topology.[5] This paper reports on the examine-out device of the future KM3NeT undersea area of numerous synchronized optical detecting nodes.[6] This paper speaks about the Compressed Baryonic matter (CBM) experiment which were used For identifying the prototypes to improve performance in serial links. The DAQ software discusses about using various data inputs, optical connections reading through USB and Ethernet etc.[7]

II.Serdes devices undergoing latency variations in existing technique.

The Xilinx FPGA which embeds a GTX transceiver is used to explain the latency overheads. The simplified

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INVITAION LETTER

Subject: INVITATION to be a subject expert for screening of faculty applications.

Ref: Commissionerate office Letter no.ADMIOEST/10/2021-JD-DEPT dated 04/10/2021

With respect to above subject and letter under reference, I would like to invite you as a subject expert member in the Screening cum Evaluation committee for Electronics and Communication Engineering to scrutinize / screen the faculty applications for the promotion under CAS. The meeting of Screening cum Evaluation committee scheduled on 18/10/2021 at 11.00 AM in the office Principal Government Engineering College Ramanagara.

Kindly accept our invitation and oblige.

Principal
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Govt. Engineering College
Ramanagara - 562159

To,
Dr. Ramesh S
Professor and HOD
Department of E & C Engineering
Dr AIT Nagarabhavi Bangalore

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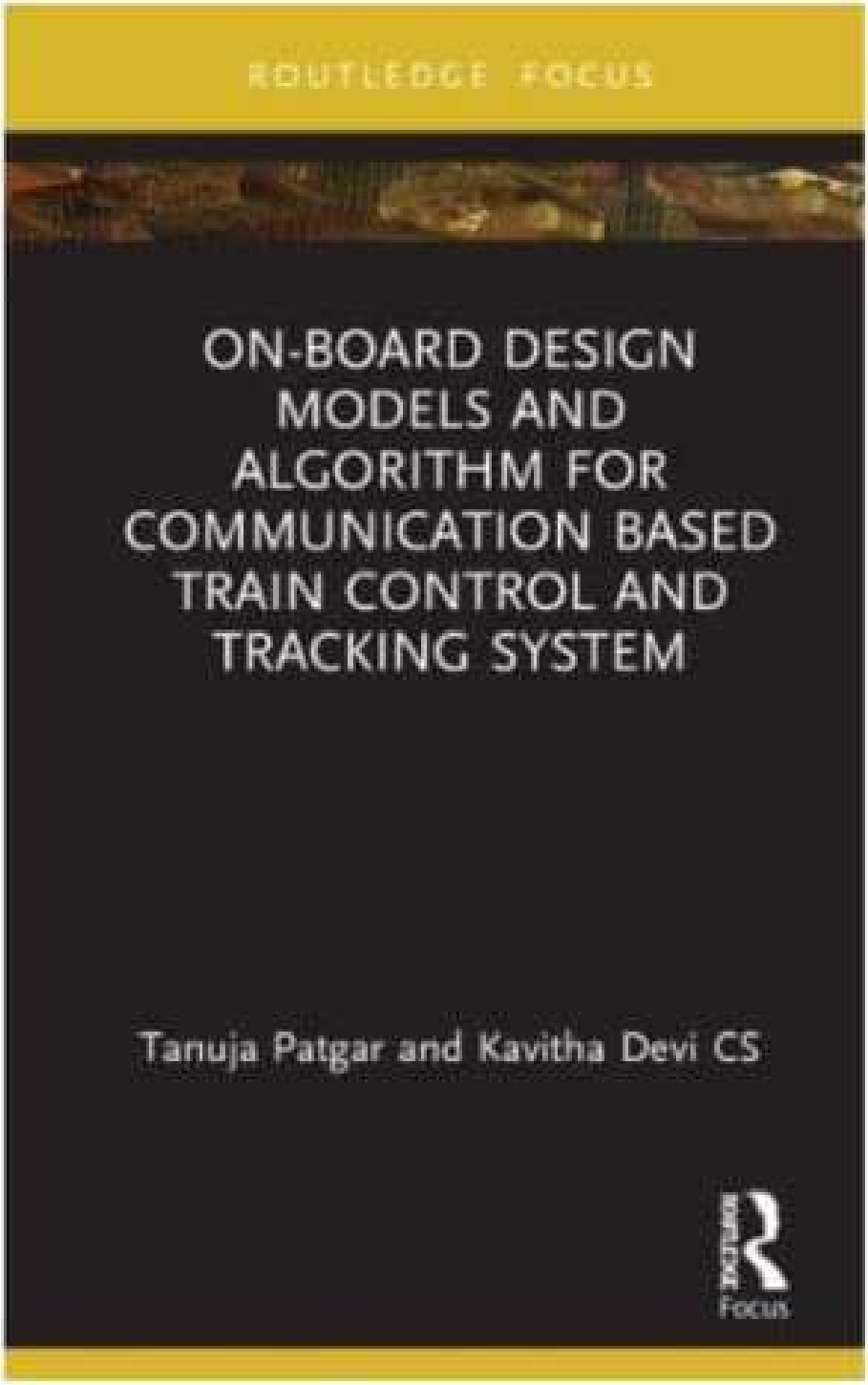

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I am a PC member of CSITSS - 2021. Could you please write a review for me on the following paper submitted to CSITSS - 2021:

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The instructions on how to answer this review request can be found at the bottom of this letter.

I need to receive the review by 10.9.2021

If you cannot review this paper, could you please suggest names and email addresses of 2-3 possible reviewers?

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Respected Madam

Sub: Invite to attend the External BOS meeting on July 23, 2022

I am writing on behalf of the Dr. Ambedkar Institute of Technology, Bengaluru to invite you as a **Faculty Member bearing specialization of the Board of studies (BOS)** in Electronics and Communication Engineering. The **External Board of studies meeting will be held on Saturday 23rd July 2022 at 10:00 AM.** The focus of the meeting will be to discuss and approve the scheme and syllabus of the Electronics and Communication Engineering for the **Academic year 2022-23 for both UG and PG programs**.
We are expecting about **20** members to attend the Board of studies meeting. Hence I request you to kindly attend the meeting on 23rd July 2022 Positively.

Sincerely,

Dr. Ramesh S
BOS Chairman
Prof. & Head of Department of Electronics and Communication Engineering
Dr. Ambedkar Institute of Technology
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Mobile No: 97435355359/8660797115

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Subject: Research Collaboration
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Good Morning Sir,

Sorry for the late reply, as I was on medical leave for a week.

We are interested in your ongoing project on Image Processing and guide us in which way we can collaborate with you. We can process " MOU" between two institutions.

Thank you,
With regards,
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Fwd: Research Collabaration

1 message

Tanuja Harish <tanujaharish13@gmail.com> Mon, Nov 1, 2021 at 11:18 AM
To: rajgroup71@gmail.com

---------- Forwarded message ---------
From: **Tanuja Harish** <tanujaharish13@gmail.com>
Date: Tue 6 Oct, 2020, 1:16 PM
Subject: Re: Research Collabaration
To: <vasudvr@unisa.ac.za>

Respected Sir,

Season greeting!

Hope everything is fine at your end during the pandemic. Earlier, I have sent you mine and one of my colleague's curriculum vitae for your reference. I request you to go through them once and revert if you are interested to collaborate in any research activity with us.

Anticipating for positive reply,

Thanking you,

On Tue, 25 Aug 2020 at 09:59, Tanuja Harish <tanujaharish13@gmail.com> wrote:

Good Morning Sir,

Thank you for your mail. For your referance i am sending my biodata along with my friend biodata.
Both are interested to do research togrther. We two working for same Institute.
Eagerly waiting for your reply.

With warm regards,
Dr. Tanuja Patgar
ph- 6360373101

On Mon, 10 Aug 2020 at 11:37, Tanuja Harish <tanujaharish13@gmail.com> wrote:

---------- Forwarded message ---------
From: **Veeredhi, Vasudeva** <vasudvr@unisa.ac.za>
Date: Mon, 10 Aug 2020 at 11:21
Subject: RE: Research Collabaration
To: Tanuja Harish <tanujaharish13@gmail.com>

Dear Dr. Tanuja Patgar,

Thank you for your e-mail and hope this mail finds you well.

I was bit tied-up with other assignments and could not reply you immediately.

I appreciate your interest in research collaborations.

From your e-mail, I could not understand your research strengths.

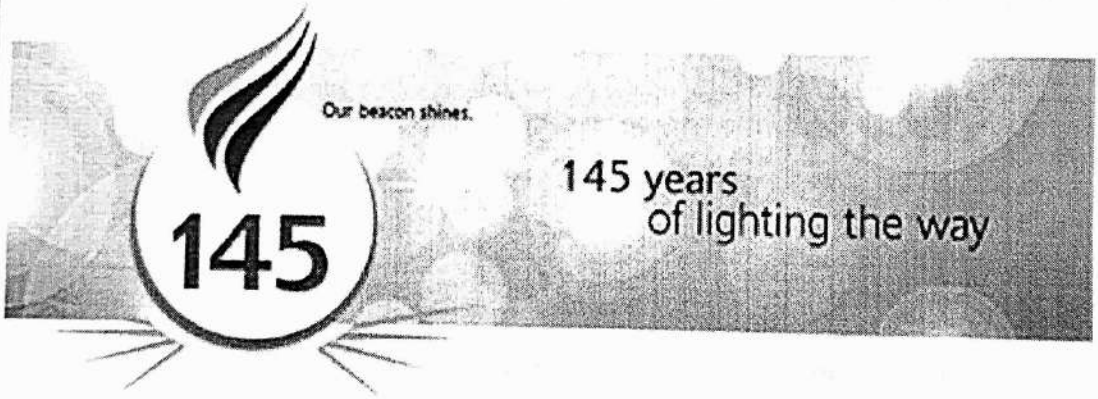
You have mentioned one on "health-care" and the other one on "water management".

May you please send me your CV, so that I can suggest appropriately.

Best Regards

Prof. Veeredhi.Vasudeva Rao
Ph.D, MASME, MISTE, MSESI, MISOI.
Associate Directror School of Engineering
Mechanical and Industrial Engineering
CSET, University of South Africa

UNISA university of south africa



From: Tanuja Harish <tanujaharish13@gmail.com>
Sent: 04 August 2020 6:24 AM
To: Veeredhi, Vasudeva <vasudvr@unisa.ac.za>
Subject: Research Collabaration

Respected Sir,

I am Dr.Tanuja Patgar, working as an Assistant professor in Dr.Ambedkar institute of technology, Bangalore. I had attended your expert lecture in STTP on "Nanotechnology and Functional Materials" organised by SVCE, Tirupati and you had mentioned in your lecture for research project collaboration UNISA for theme like water, health and education.

Recently, I have published a book chapter in heath-care using machine learning domain and another my research work has been accepted in the domain of water management.

Technology

Bengaluru

Dear Prof.

DR. S. Ramesh.

On behalf of Jain (Deemed to be University), I take this opportunity to invite you to attend the Board of Studies meeting for Ph.D. Course of Department of **Electronics and Communication Engineering** scheduled to be held on **Day: Saturday, Date: 21th September 2019, 11.00am onwards Place:** Jain (Deemed to be University), JP Nagar Campus, Behind Zaitoon Hotel, Bangalore to finalize the course work syllabus of Ph.D. August 2019 Batch. In this connection I request you to kindly make it convenient to attend the same and oblige.

Thanking you,

IEEE BANGALORE SECTION

CONECCT 2022

IEEE

CERTIFICATE OF

APPRECIATION

This is to recognise the contribution of

Kavitha Devi CS

as **REVIEWER** for the 8th **International Conference on Electronics, Computing and Communication Technologies**, IEEE CONECCT (July 08-10, 2022) organized by IEEE Bangalore Section

Dr. P Deepa Shenoy
GENERAL CHAIR, IEEE CONECCT 2022
CHAIR, IEEE BANGALORE SECTION

Dr. Muralidhara V N
TPC CO-CHAIR
IEEE CONECCT 2022

Dr. Navin
TPC CO-CHAIR
IEEE CONECCT 2022

Dr. Ramakrishnan Raman
TPC CO-CHAIR
IEEE CONECCT 2022

publons

Dear Kavitha Devi C S,

We're writing to let you know that Plasma cleaning under low pressures based on the domestic microwave oven, which you reviewed for Journal of Microwave Power & Electromagnetic Energy, was published on May 6 by Journal of Microwave Power and Electromagnetic Energy. This was 175 days since your review.

As an expert involved in the peer review process, we thought you'd like to know what happened with this paper.

What do you think of the published version? Let the world know by writing a post-publication review of or scoring the article.

Got a question?
Check out our FAQ

Gmail ripal patel <ripalpatel315@gmail.com>

Invitation to become a Reviewer for the 2022 IEEE International RF and Microwave Conference (RFM)

1 message

RFM 2022 (contact@apmttemc.org) <contact=apmttemc.org@edas.info> Wed, Aug 17, 2022 at 2:13 PM
Reply-To: RFM 2022 <contact@apmttemc.org>
To: Ripal Patel <ripalpatel315@gmail.com>

Dear Ms. Ripal Patel,

Based on your expertise, you are cordially invited to become a Reviewer of the 2022 IEEE International RF and Microwave Conference (RFM) (RFM 2022). We hope that your technical expertise matches the scope of the conference, ensuring the quality of the conference technical program.

Please visit the conference website at: http://rfm2022.apmttemc.org for further info on the conference.

- Please indicate your decision whether or not to accept this invitation within two weeks, by following this link: https://edas.info/Tyn.php?tpc=1001179396

- In order to be given review assignment in your area, you are encouraged to choose your topics of interest here: https://edas.info/editInterest.php?tpc=1001179396

You may recommend other experts to be part of the reviewers team of RFM 2022 by providing their name, affiliation, email address that is used for EDAS, and relevant track, to contact@apmttemc.org.

Best Regards,
Azremi Abdullah Al-Hadi
Chair
RFM2022

2021 IEEE IAS 4th International Conference on Computing, Power and Communication Technologies (GUCON)

September 24-26, 2021

Certificate of
Technical Program Committee Member

This is certify that Prof. /Dr. ***RIPAL PATEL***

of *Dr.Ambedkar Institute of Technology, Bangalore*

has contributed as TPC member of IEEE IAS GUCON 2021.

His/ Her Certificate No. is *GUCON/AFDT2R87*

Technical Chair

IEEE
Advancing Technology for Humanity

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IEEE INDUSTRY APPLICATIONS SOCIETY
Linking Research to Practice

Technical Chair

Gmail ganga raj <rajgroup71@gmail.com>

Fwd: Invitation to be a Technical Committee Member of IFERP

1 message

Tanuja Harish <tanujaharish13@gmail.com> Mon, Nov 1, 2021 at 9:21 AM
To: rajgroup71@gmail.com

---------- Forwarded message ---------
From: **Tanuja Harish** <tanujaharish13@gmail.com>
Date: Sat, 30 Oct 2021 at 11:52
Subject: Fwd: Invitation to be a Technical Committee Member of IFERP
To: Tanuja Harish <tanujaharish13@gmail.com>

---------- Forwarded message ---------
From: **Tanuja Harish** <tanujaharish13@gmail.com>
Date: Fri, 13 Aug 2021 at 15:49
Subject: Fwd: Invitation to be a Technical Committee Member of IFERP
To: Tanuja Harish <tanujaharish13@gmail.com>

---------- Forwarded message ---------
From: **Tanuja Harish** <tanujaharish13@gmail.com>
Date: Thu, 27 Jun 2019 at 15:53
Subject: Re: Invitation to be a Technical Committee Member of IFERP
To: Prabhu E <prabhu@technoarete.org>

Dear Sir,

I am very honour to accept your invitation.

with regards
Dr. Tanuja

On Thu, 27 Jun 2019 at 15:10, Prabhu E <prabhu@technoarete.org> wrote:

> Dear Dr Tanuja,
>
> Greetings from IFERP - Karnataka chapter
>
> Being a valuable member of IFERP, we would like to nominate you as our **Technical Committee Member** for Institute for Engineering Research and Publication (IFERP), **Karnataka Chapter.**
>
> As you know, Institute for Engineering Research and Publication (IFERP) is one of India's largest Non-profitable professional association working on research & development with promotion in the field of Engineering and Technology.
>
> IFERP conducts Technical Conferences (International), Summits, and Meetings at different parts of the country to reduce the gap between curriculum and their practical implementation among students and research scholars.
>
> **As a Technical Committee member the benefits would be**
>
> - Recognition from IFERP
> - Special Benefits in International conferences organized by IFERP
> - Benefits in research articles for publications
> - Exposure to scientific Community across state as well country level
> - Benefits in Professional Membership

CSITSS - 2021 submission review request

Inbox ×

EasyChair <noreply@easychair.org> Wed, Sep 15, 2021, 9:49 AM

to me

Dear Kavithadevi,

I am a PC member of CSITSS - 2021. Could you please write a review for me on the following paper submitted to CSITSS - 2021:

Paper id: 20
Title: Multipurpose Vertical Plotter Machine – MVPM

The instructions on how to answer this review request can be found at the bottom of this letter.

I need to receive the review by 20.9.2021

If you cannot review this paper, could you please suggest names and email addresses of 2-3 possible reviewers?

CSITSS - 2021 submission review request

Inbox x

EasyChair <noreply@easychair.org> Fri, Sep 3, 2021, 11:26 AM
to me

Dear Kavithadevi,

I am a PC member of CSITSS - 2021. Could you please write
a review for me on the following paper submitted to CSITSS - 2021:

Paper id: 26
Title: Smart Traffic Management System using Internet of Things (IoT)

The instructions on how to answer this review request
can be found at the bottom of this letter.

I need to receive the review by 10.9.2021

If you cannot review this paper, could you please suggest names and
email addresses of 2-3 possible reviewers?

ICRISET-2020

International Conference
on
RESEARCH AND INNOVATIONS IN
SCIENCE, ENGINEERING & TECHNOLOGY
4th - 5th September, 2020

Certificate of Appreciation

This Certificate is Awarded to

Dr. Tanuja Patgar

For her outstanding service rendered as the

Reviewer

at

2ND INTERNATIONAL CONFERENCE (DIGITAL) ON RESEARCH AND INNOVATIONS IN SCIENCE, ENGINEERING & TECHNOLOGY ICRISET - 2020

held at

BIRLA VISHVAKARMA MAHAVIDYALAYA ENGINEERING COLLEGE,
VALLABH VIDYANAGAR, GUJARAT, INDIA
during 4th - 5th SEPTEMBER, 2020

DR. INDRAJIT N. PATEL
PRINCIPAL, BVM &
CONFERENCE CHAIR

UMBER OF
REVIEWED : 2

IEEE
Advancing Technology for Humanity

IEEE Malaysia AP/MTT/EMC Joint Chapter

Certificate of Appreciation

This certificate is hereby granted to

Ms. Ripal Patel

for his/her outstanding support and contribution as

REVIEWER

in

2021 IEEE Asia-Pacific Conference on Applied Electromagneti (APACE2021)

Chair
IEEE Malaysia AP/MTT/EMC Joint Chapter

2021 APACE

Gmail Tanuja Harish <tanujaharish13@gmail.com>

Invitation to be a Technical Committee Member of IFERP

5 messages

Prabhu E <prabhu@technoarete.org> 27 June 2019 at 15:11
To: tanujaharish13@gmail.com

Dear Dr Tanuja,

Greetings from IFERP - Karnataka chapter

Being a valuable member of IFERP, we would like to nominate you as our **Technical Committee Member** for Institute for Engineering Research and Publication (IFERP), **Karnataka Chapter**.

As you know, Institute for Engineering Research and Publication (IFERP) is one of India's largest Non-profitable professional association working on research & development with promotion in the field of Engineering and Technology.

IFERP conducts Technical Conferences (International), Summits, and Meetings at different parts of the country to reduce the gap between curriculum and their practical implementation among students and research scholars.

As a Technical Committee member the benefits would be

- Recognition from IFERP
- Special Benefits in International conferences organized by IFERP
- Benefits in research articles for publications
- Exposure to scientific Community across state as well country level
- Benefits in Professional Membership

As a Technical Committee member you shall lend your support in

- Support in Activities plan (Conference, Students Chapter, Workshops)
- Promoting activities to other faculty members.
- Foster good relations with the local Section and encourage students to establish regular liaison with the Sections.
- Increasing new student members, professional Members & Institutional members.
- Promoting all the activities of IFERP.

We hope your association with IFEPR will bring growth and development to Scientific Research and Development.

Thank you.

Regards,
E. Prabhu M.Sc., M. Phil.,
+91 9962691866
Scientific Relations Executive
Membership & Association Department

IFERP®
connecting engineers... developing research

Ministry of Education
Government of India

MoE's INNOVATION CELL
(GOVERNMENT OF INDIA)

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Azadi Ka Amrit Mahotsav

SMART INDIA HACKATHON 2022

#SIH Senior Software Edition

GRAND FINALE 2022 August 25-26

Expert

Certificate

This Certificate is awarded to

Dr. Tanuja P Patgar

for exceptional contribution as a Expert in Smart India Hackathon, 2022

Sh. K Sanjay Murthy
Secretary, Higher Education,
Ministry of Education

Prof. Anil D. Sahasrabudhe
Chairman, AICTE
Ministry of Education

Dr. Abhay Jere
Chief Innovation Officer
Ministry of Education's Innovation Cell

Dr. Anand Deshpande
Chairman and MD,
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Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY

(An Autonomous Institute, Affiliated to VTU, Belgaum)
Outer Ring Road, Mallathalli, Bangalore - 560 056.

THE WORLD BANK
NPIU

Department of Electronics and Instrumentation Engineering

Certificate of Appreciation

This Certificate is awarded to Dr./Prof./Mr./Mrs./Ms. Tanuja P Palsar
of Dr. AIT, Bangalore chaired the technical session
for the Project Exhibition Competition in the
Fifth National Conference on Computational Control Systems & Optimization (CCSO-2019)
under TEQIP-III held on 25th & 26th April 2019 at Dr. AIT, Bangalore-56.

Dr. M. Meenakshi, Dean (A)
Convener, Prof. & Head, EIE

Dr. C. Nanjunda Swamy
Principal, Dr. AIT

Kammavari Sangham (R) 1952
K.S. GROUP OF INSTITUTIONS
ಕೆ.ಎಸ್. ತಾಂತ್ರಿಕ ಮಹಾವಿದ್ಯಾಲಯ
K.S. INSTITUTE OF TECHNOLOGY
Approved by AICTE, New Delhi; Affiliated to VTU, Belagavi, Karnataka; Accredited by NAAC
14, Raghuvanahalli, Kanakapura Road, Bengaluru - 560 109.
Tel : 080 28435722 / 24, Fax : 080 28435723
E-mail : principal.ksit@gmail.com / principal@ksit.edu.in | Website : www.ksit.edu.in

Date: 25/6/2022

To

Dr. Rangaswamy Y
Asst. Professor
Dr. Ambedkar Institute of Technology
Bangalore.

Dear Sir,

On behalf of K.S. Institute of Technology I would like to thank you for gracing the occasion as Judge for project exhibition Contest in ECE department on 25th June 2022.

We would like to thank you for your precious time and valuable comments to our students.

Looking forward for your cooperation in future as well.

Sincerely,

HEAD OF THE DEPARTMENT
Dept. of Electronics & Communication Engg
K.S. Institute of Technology
Bengaluru - 560 109

CERTIFICATE OF APPRECIATION

This Certificate is proudly presented to

Dr. Chetan S

of Institute

NCET, Bengaluru

for role of ***Session Chair***

in

2020 IEEE International Conference for Innovation in Technology (INOCON)

Technically Cosponsored by IEEE Bangalore Section

06th - 08th November 2020

Dr. Anitha Patil
Convener

Dr. Jitendranath Mungara
Conference Chair

Dr. S G Gopala Krishna
General Chair

NAGARJUNA

IEEE

Gmail

Mahalinga V Mandi <mvmandi@gmail.com>

nvitation to National conference on "Digital Technologies for Smart Cities", as a session :hair-reg

messages

TELECOMMUNICATION ENGINEERING RVCE <hod.tc@rvce.edu.in> 12 May 2022 at 11:08
To: mvmandi@gmail.com

Dear Sir,

To mark the celebrations of "World Telecommunication and Information Society Day –WTISD" a national conference on ***"Digital Technologies for Smart Cities"*** is scheduled during 17th & 18th, May 2022. The Conference is organized by the Department of Electronics and Telecommunication Engineering of RV College of Engineering, Bengaluru. It is an annual event of the institution to spread awareness, research opportunities and enhance technical interaction among faculty, students and technical experts.

We request you kindly to be the session chair in conference on **17th May**, 2022, between **2.00 noon to 3.15 pm**. Also we invite you to grace the inauguration of the conference.

Invitation of the program are enclosed with this letter.

Thanking you
With Thanks and Regards

Dr. K. Sreelakshmi
Professor and HoD
Dept.of Telecommunication Engg.
RVCE, Bangalore
PH: 9845530311
Off:080-68188213/14

Conference Invitation-2022.pdf
141K

Mahalinga V Mandi <mvmandi@gmail.com> 12 May 2022 at 13:05
To: TELECOMMUNICATION ENGINEERING RVCE <hod.tc@rvce.edu.in>

Dear Madam,

Thank you for the invitation and will be there on time.

Regards, Mandi
[Quoted text hidden]

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RV College of Engineering ®
Autonomous Institution Affiliated to Visvesvaraya Technological University, Belagavi
Approved by AICTE, New Delhi
RVE/ EI/ /20 -20

Go, change the world
Department of Electronics and Telecommunication Engineering
Ph: 080-6718 8213, 8214
e-mail: hod.tc@rvce.edu.in

17.05.2022

To

Prof Mahalinga Mandi
Professor,
Dr AIT

Dear Sir/Madam,

We extend our sincere thanks to you for accepting our invitation to be a session chair at the 2-day National conference on "Digital Technologies for Smart Cities" during 17th - 18th, May 2022, celebrated on the occasion of World Telecommunication and Information Society Day -2022". We request your association and support in our future endeavors.

Thanking You

Sreelakshmi.b 17/5/22

Dr. Professor & Head
Dept. of Electronics and Telecommunication Engg
RV College of Engineering
Bengaluru-59

Dept. of ETE, RVCE,
Bengaluru-59

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Approved by AICTE, New Delhi

Dr. [illegible] Sadashivappa
Controller of Examination

Ref: RVCE/CIE-M/[illegible]/22-23

Date: 11.08.2022

Attendance Certificate

This is to certify that Dr. Mahalinga V Mandi, Professor & Head, Department of Electronics & Communication Engineering, Dr. Ambedkar Institute of Technology, Bengaluru has attended the question paper scrutiny meeting of RV Autonomous Scheme held at RV College of Engineering on 11.08.2022.

Controller of Examinations

RV College of Engineering®

Autonomous Institution Affiliated to Visvesvaraya Technological University, Belagavi

Approved by AICTE, New Delhi

Dr.G. Sadashivappa
Controller of Examination

Ref: RVE/EXAM/[illegible]/22-23

Date: 08.08.2022

To,
Mahalinga V Mandi,
Professor, Department of ECE,
Dr. Ambedkar Institute of Technology,
BDA, Outer Ring Road, Near Gnana BHarati,
Bengaluru-560056
Mobile:85535101910
Email ID:mvmandi@yahoo.com

Dear Sir,

Sub: UG Question Paper Scrutiny meeting.

A meeting of the Board of Examiners of Autonomous UG exams of our Institution is convened on Thursday, 11.08.2022 at 10.30 AM in the Library Block, RVCE, Mysuru Road, Bengaluru to scrutinize the question papers for the Examinations of Even Semester. Kindly make it convenient to attend the meeting as an external member of BoE in Electronics & Communication Engineering.

You will be paid TA/DA as per the RVCE norms.

Thanking you

Yours sincerely

CONTROLLER OF EXAMINATIONS

Controller of Examinations
RV College of Engineering (Autonomous)
Mysore Road, Bengaluru-[illegible]

Gmail Dr Umadevi H <umadevi.ait@gmail.com>

BOE Meeting Invitation

1 message

ec_Office - <ec_office@bmsce.ac.in> Fri, Jul 1, 2022 at 10:03 AM
To: Umadevi H <umadevi.ait@gmail.com>
Cc: Hod Ece <hod.ece@bmsce.ac.in>

To
Dr. Umadevi
Professor, .Dept of ECE,
Dr. A.I.T. Bangalore
Ph: 9880324895,
umadevi.ait@gmail.com

Respected Madam,

We are glad to invite your kind self for the BOE Meeting of Electronics & Communication Engineering Department scheduled on 01/07/2022 from 10.00am to 5pm in the COE office, BMS College of Engineering, Bull Temple Road, Bangalore.

Regards,

Vani T S
ECE-OFFICE
Extn: 2089

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Technological
University, Belagavi

Approved by AICTE,
New Delhi

Dr.G. Sadashivappa
Controller of Examination

Ref: RVC/EXAM/455/21-22

Date: 08.02.2022

Attendance Certificate

This is to certify that Dr. Mahalinga V Mandi, Professor & Head, Department of Electronics & Communication Engineering, Dr. Ambedkar Institute of Technology, Bengaluru has attended the question paper scrutiny meeting of RV Autonomous Scheme held at RV College of Engineering on 08.02.2022.

8/2/22

Controller of Examinations

Controller of Examinations
RV College of Engineering (Autonomous)
Mysore Road, Bengaluru - 560 059

RV College of Engineering®

Autonomous Institution Affiliated to Visvesvaraya Technological University, Belagavi

Approved by AICTE, New Delhi

Dr.G. Sadashivappa
Controller of Examination

Ref: RVE/EXAM/441/21-22

Date: 31.01.2022

To,
Dr. Mahalinga V Mandi
Professor, Department of ECE
Dr. Ambedkar Institute of Technology
BDA, Outer Ring Road, Near Gnana Bharathi
Bengaluru 560056
Mobile: 8553510190
Email: mvmandi@yahoo.com

Dear Sir,

Sub: Question Paper Scrutiny meeting.

A meeting of the Board of Examiners of Autonomous UG exams of our Institution is convened Tuesday, 08-02-2022 at 10.30 AM in the Library Block of RVCE, Mysore Road, Bangalore to scrutinize the question papers for February/March-2022 Examinations. Kindly make it convenient to attend the meeting as an external member of BoE in Electronics and Communication Engineering.

You will be paid TA/DA as per the RVCE norms.

Thanking you

Yours sincerely

2/2/22

CONTROLLER OF EXAMINATIONS
Controller of Examinations
RV College of Engineering (Autonomous)
Mysore Road, Bangalore - 560 059

Visvesvaraya Technological University
EXAMINATION SECTION
Belagavi – 590 018.

Dr. B. E. Rangaswamy Ph.D.
Registrar (Evaluation)

Phone : (0831) 2498136
Fax : (0831) 2405464

Ref.No./VTU/Exam/BOE/Subject Experts/2020-2021/525 Date : 07/09/2021

To,

EC/TE /TC/MT (COMPOSITE) BOARD

Sl. No.	Name of the Chairman/Members	College	C / M
1	Dr. Mrityunjaya V. Latte	JSSATE, B'luru	Chairman
2	Dr Veena Desai	GIT, Belagavi	Member
3	Dr.Satish Shet	JSSATE,B'luru	Member
4	Dr.Vijayprakash M	DIT,B'luru	Member
5	Dr.Sathyanarayan S V	JNNCE,Shimogga	Member
6	Dr.Sridhavmurthy	UBDT,Davangere	Member
7	Dr.H.S Manjunath Reddy	Global,B'luru	Member
8	Dr.Sridhar H.R.	NIE,Mysuru	Member
9	Dr.Suresh D.	RNSIT,B'luru	Member
10	Dr.Mallikarjuna Anandhalli	GIT, Belagavi	Member
11	Dr.Aruna Sadanand Tigadi	KLE,Belagavi	Member
12	Dr.Girish Attimarad	KSSEM,B'luru	Member
13	Dr.Datthatrey	Alva's,Moodbidri	Member
14	Dr.Satish Kumar H.C.	Sapthagiri,B'luru	Member
15	Dr.Mahalingmandi	Dr.AIT,B'luru	Member
16	Dr.Ravi J.	Global,B'luru	Member
17	Dr.Rangaiah	RRCE,B'luru	Member
18	Dr.M.C.Hanumanthraju	BMSIT, B'luru	Member
19	Dr.Manjunath	JNNCE,Shimogga	Member
20	Dr.Lakshman Naik	UBDT,Davangere	Member

Sir,

Sub: Ph.D./M.sc.(Engg.) by Research Question Papers Scrutiny meeting -reg.

By the Directions of the Honorable Vice-Chancellor, a meeting of Subject Experts is scheduled to Scrutinize the Ph.D./M.sc.(Engg.) by Research Question Papers for Sept./Octo.-2021 Examinations on 22nd September- 2021. The Details of the Meeting are as under:

Date	Time	Purpose	Venue
22nd Sept.-2021	10.30am	Scrutiny of Question Papers	U.B.D.T. College of Engineering, DAVANGERE – 577 006

You are requested to make it convenient to attend the meeting. Please note it is mandatory to attend the meeting.

Thanking you,

Yours Sincerely,

Registrar (Evaluation)

Copy FWCS to :

1.The Honorable Vice-Chancellor, VTU Belagavi, through Sec., to VC, for information.
2.The Registrar, VTU Belagavi, for information.
3.The Finance Officer, VTU Belagavi, for information.

RV College of Engineering®

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Approved by AICTE, New Delhi, Accredited by NAAC, Bengaluru

Dr.G. Sadashivappa
Controller of Examination

Ref: RVE/EXAM/008/20-21

Date: 25.06.2020

To,

Dr. Mahalinga V Mandi
Professor, Department of ECE
Dr. Ambedkar Institute of Technology
BDA, Outer Ring Road
Bengaluru-560056
Mobile: 8553510190
Email:mvmandi@yahoo.com

Dear Sir,

Sub: PG Question Paper Scrutiny meeting.

A meeting of the Board of Examiners of Autonomous PG exams of our Institution is convened on Friday, 10.07.2020 at 10.30 AM in office of the Controller of Examinations, II Floor, Admin Block, RVCE, Mysuru Road, Bengaluru to scrutinize the question papers for even semester PG Examinations. Kindly make it convenient to attend the meeting as an external member of BoE in Electronics and Communication Engineering.

You will be paid TA/DA as per the RVCE norms.

Thanking you

Yours sincerely

25.06.2020

CONTROLLER OF EXAMINATIONS
Controller of Examinations
RV College of Engineering (Autonomous)
Mysore Road, Bengaluru - 560 059

RASHTREEYA SIKSHANA SAMITHI TRUST

RV COLLEGE OF ENGINEERING®

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Approved by the All India Council for Technical Education, New Delhi.

Dr. G. Sadashivappa
Controller of Examinations

Ref: RVC/EXAM/...131...../20-201

Date: 25.01.2021

Attendance Certificate

This is to certify that Dr. Mahalinga V Mandi, Professor, Department of Electronics and Communication Engineering, Dr. Ambedkar Institute of Technology, Bengaluru has attended the question paper scrutiny meeting of RV Autonomous Scheme held at RV College of Engineering on 25.01.2021.

25-01-2021

Dr. G. Sadashivappa
Controller of Examinations
Controller of Examinations
RV College of Engineering (Autonomous)
Mysore Road, Bengaluru - 560 059

R.V. Vidyaniketan Post, Mysore Road, Bengaluru – 560 059. INDIA.
Phone: +91-080-67178163/66, Mobile: 9845934591, Fax: +91-080-28600337, e-mail: sadashivappag@rvce.edu.in
Website: www.rvce.edu.in; www.rvinstitutions.com

RASHTREEYA SIKSHANA SAMITHI TRUST

RV COLLEGE OF ENGINEERING®

(Autonomous Institution affiliated to Visvesvaraya Technological University, Belagavi)
Approved by the All India Council for Technical Education, New Delhi.

Dr. G.Sadashivappa
Controller of Examinations

Ref: RVE/EXAM/...../20-21 **Date: 19.01.2021**

To
Dr. Mahalinga V Mandi
Professor, Department of ECE
Dr Ambedkar Institute of Technology
Mallathalli,
Bengaluru 560056
Mobile: 8553510190
Email: mvmandi@yahoo.com

Dear Sir,

Sub: Question Paper Scrutiny meeting.

A meeting of the Board of Examiners of Autonomous UG exams of our Institution is convened on Monday, 25.01.2021 at 10.00 AM in the Library Block of RVCE, Mysore Road, Bangalore to scrutinize the question papers for Jan/Feb-2021 Examinations. Kindly make it convenient to attend the meeting as an external member of BoE in Electronics and Communication Engineering. You will be paid TA/DA as per the RVCE norms.

Thanking you

Yours sincerely

CONTROLLER OF EXAMINATIONS

19-01-2021
Controller of Examinations
RV College of Engineering (Autonomous)
Mysore Road, Bengaluru - 560 059

BMS COLLEGE OF ENGINEERING, BENGALURU-19

(Autonomous Institute, Affiliated to VTU)

Department of Electronics and Communication Engineering

Date: 06/12/2019

To
Dr. Umadevi
Professor, ,Dept of ECE,
Dr. A.I.T, Bangalore
Ph: 9880324895,
umadevi.ait@gmail.com

Respected Sir,

We are glad to invite your kind self for the BOE Meeting of Electronics & Communication Engineering Department scheduled on on 10/12/2019 & 11/12/2019 at 10.00am in the COE office, BMS College of Engineering, Bull Temple Road, Bangalore.

HOD ECE
Dr. Arathi R Shankar
Professor & HOD
Department of Electronics and Communication
BMS College of Engineering
Bull Temple Road, Bangalore

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Dr. G.Sadashivappa
Controller of Examinations

Ref: RVE/EXAM/2035/19-20 **Date: 26.10.2019**

To
Dr. Mahalinga V Mandi
Professor, Department of ECE
Dr. Ambedkar Institute of Technology
BDA, Outer Ring Road, Near Gnana Bharathi
Bengaluru 560056
Mobile: 8553510190
Email: mvmandi@yahoo.com

Dear Sir,

Sub: Question Paper Scrutiny meeting.

A meeting of the Board of Examiners of Autonomous UG exams of our Institution is convened on Tuesday, 12.11.2019 at 10.30 AM in the Library Block of RVCE, Mysore Road, Bangalore to scrutinize the question papers for Nov/Dec-2019 Examinations. Kindly make it convenient to attend the meeting as an external member of BoE in Electronics and Communication Engineering. You will be paid TA/DA as per the RVCE norms.

Thanking you

Yours sincerely

26-10-19

CONTROLLER OF EXAMINATIONS

Controller Of Examinations
R.V. College Of Engineering (Autonomous)
Mysore Road, Bangalore - 560 059

R.V. Vidyaniketan Post, Mysore Road, Bengaluru – 560 059. INDIA.
Phone: +91-080-67178163 Fax: +91-080-28600337 e-mail: sadashivappag@rvce.edu.in
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Dr. G.Sadashivappa
Controller of Examinations

Ref: RVE/EXAM/2213/19-20

Date: 22.05.20

To
Dr. Mahalinga V Mandi
Professor, Department of ECE
Dr. Ambedkar Institute of Technology
BDA, Outer Ring Road, Near Gnana Bharathi
Bengaluru 560056
Mobile: 8553510190
Email: mvmandi@yahoo.com

Dear Sir,

Sub: Question Paper Scrutiny meeting.

A meeting of the Board of Examiners of Autonomous UG exams of our Institution is convened on Friday, 29.05.2020at 10.00 AM in the Office of CoE RVCE, Mysore Road, Bangalore to scrutinize the question papers for even semester UG Examinations. Kindly make it convenient to attend the meeting as an external member of BoE in Electronics and Communication Engineering.

You will be paid TA/DA as per the RVCE norms.

Thanking you

Yours sincerely

22-05-2020

CONTROLLER OF EXAMINATIONS
Controller of Examinations
RV College of Engineering (Autonomous)
Mysore Road, Bengaluru - 560 059

R.V. Vidyaniketan Post, Mysore Road, Bengaluru – 560 059. INDIA.
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