Dr Ambedkar Institute of Technology, Bengaluru-56

Department of VLSI Design and Technology

Third and Fourth Scheme & Syllabus

Scheme & Syllabus - CBCS – 2025 -2026 Regulation

Academic Year 2026-2027

Dr. Ambedkar Institute of Technology, Bengaluru-560056
Outcome Based Education(OBE) and Choice Based Credit System
B.E. in Electronics and Communication Engineering (VLSI Design and Technology)
Scheme of Teaching and Examinations 2025 Scheme

III SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Department (TD) and Question	Teaching & Learning Scheme					Examination				Credits
					CI		LI	TW/SL	TH/S	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S						
1	ASC/PCC	1BMAT301D	Transform and Statistical Techniques	TD/PSB: Maths	42	28	0	50	120	03	50	50	100	4
2	IPCC	1BSESU302	Digital System Design using Verilog	TD: VL PSB:EC	42	0	28	50	120	03	50	50	100	4
3	PCC	1BSEST303	Network Analysis	TD: VL PSB:EEE	42	28	0	50	120	03	50	50	100	4
4	PCC	1BSEST304	Analog Electronics and Linear Integrated Circuits	TD: VL PSB:TE	42	0	0	48	90	03	50	50	100	3
5	PCC	1BVLP305	Fundamentals of Signal Processing	TD/PSB: VL	42	0	0	48	90	03	50	50	100	3
6	PCCL	1BSESL306	Analog Electronics and Linear Integrated Circuits Lab	TD/PSB: VL	0	0	28	2	30	02	50	50	100	1
7	AEC	1BVLL307X	Ability Enhancement Course Laboratory**	TD/TSB: VL	0	0	28	2	30	02	50	50	100	1
8	SDC	1BCP308	Community Project (Project-Based Learning) / Societal Project	TDTSB: VL	0	0	0	30	30	02	50	50	100	1
9	MC	1BCDN309	Placement	Placement	2	0	0	0	-	-	50	-	50	NP/PP
9	NCMC	1BNSN310	National Service Scheme (NSS)	CAMPUS: NSS coordinator	2	0	0	28	28	---	100	---	100	PP
		1BPEN310	Physical Education (PE) (Sports and Athletics)	CAMPUS: Physical Education Director										
		1BYON310	Yoga	CAMPUS: Yoga Teacher										
		1BMUN310	Music	CAMPUS: Music Teacher										
TOTAL					210	56	84	308	658		500	400	900	21

10	**NCMC**	**1BMATDIP310**	**Mathematics course for lateral entry**	**TD: Maths/ CIE online VTU**	**14**	**0**	**0**	**14**	**28**	**3**	**100**	**---**	**100**	**PP**
				Total	**224**	**56**	**84**	**322**	**686**		**600**	**400**	**1000**	**21**
	PCC: Professional Core Course, PCCL: Professional Core Course laboratory, UHV: Universal Human Value Course, MC: Mandatory Course (Non-credit), AEC: Ability Enhancement Course, SEC: Skill Enhancement Course, L: Lecture, T: Tutorial, P: Practical, S= Self-Study, CIE: Continuous Internal Evaluation, SEE: Semester End Evaluation. K: This letter in the course code indicates common to all the streams of Engineering. ESC: Engineering Science Course, ETC: Emerging Technology Course, PLC: Programming Language Course														

****Ability Enhancement Course (Laboratory) 1BVLL307x**			
1BVLL307A	**Data Structures using Python**	**1BVLL307C**	**Linux Fundamentals and Introduction to Python Programming**
1BVLL307B	**Simulation of Circuits and Devices**	**1BVLL307D**	**Numerical Computing Laboratory using GNU Octave / SCI lab**

Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.

National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first Week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the Degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course is mandatory for the award of Degree.

Dr. Ambedkar Institute of Technology, Bengaluru-560056
Outcome Based Education(OBE) and Choice Based Credit System
B.E. in Electronics and Communication Engineering (VLSI Design and Technology)
Scheme of Teaching and Examinations 2025 Scheme

IV SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)		Teaching & Learning Scheme					Examination				Credits
						CI		LI	TW/SL	TH/S	Duration in hours	CIE Marks	SEE Marks	Total Marks	
						L	T	P	S						
1	ASC/PCC	1BMAT401D	Complex Analysis and Numerical Techniques	TD/PSB: Maths		42	0	0	48	90	03	50	50	100	3
2	IPCC	1BSESU402	Microcontrollers	TD: VL PSB: EI		42	0	28	50	120	03	50	50	50	4
3	PCC	1BSEST403	Control Systems	TD: VL PSB:EEE		42	28	0	50	120	03	50	50	100	4
4	PCC	1BVLP404	CMOS Digital VLSI Design	TD/TSB: VL		42	0	0	48	90	03	50	50	100	3
5	PCCL	1BVLPL405	Design for Test Lab	TD/TSB: VL		0	0	28	02	30	02	50	50	100	1
6	AEC	1BVLL406x	Ability Enhancement Course Laboratory**	TD/TSB: VL		0	0	28	02	30	02	50	50	100	1
7	BSC	1BBIT407	Biology for Electrical and Electronics Engineers	TD: VL PSB: ETE		28	0	0	32	60	03	50	50	100	2
8	SDC	1BEP408	Environmental Science Project	TDTSB: CIVIL		0	0	0	30	30	03	50	50	100	1
9	PCC	1BVLP409	Design for Test	TD/TSB: VL		42	0	0	48	90	03	50	50	100	3
10	MC	1BCDN409	Placement	Placement		2	0	0	0	-	-	50	-	50	NP/PP
10	NCMC	1BNSN410	National Service Scheme (NSS)	CAMPUS	NSS coordinator	0	0	0	28	28	---	100	---	100	PP/ NP
		1BPEN410	Physical Education (PE) (Sports and Athletics)		Physical Education Director										
		1BYON410	Yoga		Yoga Teacher										
		1BMUN410	Music		Music Teacher										
Total						212	56	84	366	688		550	450	1000	22

11	**NCMC**	**1BMATDIP410**	**Mathematics course for lateral entry**	**TD: Maths/ CIE online VTU**	**14**	**0**	**0**	**14**	**28**	**3**	**100**	**---**	**100**	**PP**
				Total	**226**	**56**	**84**	**380**	**716**		**650**	**450**	**1100**	**22**

PCC: Professional Core Course, PCCL: Professional Core Course laboratory, UHV: Universal Human Value Course, MC: Mandatory Course (Non-credit), AEC: Ability Enhancement Course, SEC: Skill Enhancement Course, L: Lecture, T: Tutorial, P: Practical, S= Self-Study, CIE: Continuous Internal Evaluation, SEE: Semester End Evaluation. K : This letter in the course code indicates common to all the stream of engineering.

****Ability Enhancement Course (Laboratory) 1BVLL406x**

1BVLL406A	**Python for Measurement & Data Analysis**	**1BVLL406C**	**RTL to GDS Flow**
1BVLL406B	**SPICE Programming for Electronic Circuits**	**1BVLL406D**	**Power Electronics**

 # TH/S- Total Hours per Semester, TW& SL- Term Work & Self Learning

Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.

National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first Week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the Degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses is mandatory for the award of Degree

Dr Ambedkar Institute of Technology, Bengaluru-56

Department of VLSI Design and Technology

Third and Fourth Syllabus

Syllabus - CBCS – 2025 -2026 Regulation

Academic Year 2026-2027

Course Title	Transforms and Statistical Techniques (EE, EC, ET, EI, VLSI)						
Course Code	1BMAT301D						
Course Category	ASC (Applied Science Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	3	2	0	4	5	42+28+50=120	4
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:

This course is proposed to impart to the students the skills of employing the basic tools of Fourier series, Fourier transform, Z-transform, probability distributions, and Statistical techniques to solve basic and complex engineering problems with related applications.

SYLLABUS	No. of Hours	BTLs
UNIT 1	**10**	**L1-L4**
Statistical techniques: Curve fitting by method of least squares: $y = ax + b$, $y = ax^2 + bx + c$ and $y = ab^x$. Correlation–Karl Pearson's coefficient of correlation, Regression analysis – lines of regression (without proof), angle between regression lines-problems.		
SELF-STUDY COMPONENTS: Rank correlation, Growth modeling.		
UNIT 2	**10**	**L1-L4**
Probability Distributions: Random variables (discrete and continuous), probability mass and density functions. Mathematical expectation and variance. Binomial, Poisson, normal and exponential distributions- only problems.		
SELF-STUDY COMPONENTS: Geometric and Gamma distributions, Application to transmission errors in noise media.		
UNIT 3	**10**	**L1-L4**
Fourier series: Periodic function, Dirichlet's condition, conditions for a Fourier series expansion, Fourier series of functions with arbitrary period and half range Fourier series (without proof). Practical harmonic analysis.		
SELF-STUDY COMPONENTS: Typical waveforms, complex form of Fourier series.		
UNIT 4	**10**	**L1-L4**
Fourier Transforms: Definition, infinite Fourier transforms, inverse Fourier transforms, Fourier sine and cosine transforms, inverse Fourier sine and cosine transforms.		
SELF-STUDY COMPONENTS: Fourier transform of derivatives, solution of boundary value problems. Parseval's identity.		
UNIT 5	**10**	**L1-L4**
Z-Transforms: Definition, Z-transforms of basic sequences and standard functions. Properties-linearity, scaling, first and second shifting, multiplication by n (without proof), initial and final value theorems. Inverse Z-transforms. Application to solve first order difference equation using Z-transforms		

SELF-STUDY COMPONENTS:
Formation of linear difference equations with constant coefficients.

TEXT BOOKS:

1. B. S. Grewal, Higher Engineering Mathematics Khanna Publishers, New Delhi.
2. E. Kreyszig, Advanced Engineering Mathematics, John Wiley and Sons.
3. Glyn James, Advanced modern Engineering Mathematics, Pearson Publications,
4. H.C. Taneja, Advanced Engineering Mathematics, volume I & II, I.K. International Publishing House Pvt. Ltd., New Delhi.

REFERENCE BOOKS:	
1	B. V. Ramana, Higher Engineering Mathematics, McGraw–Hill Education..
2	Srimanta Pal & Subodh C. Bhunia, Engineering Mathematics, Oxford University Press
3	C. Ray Wylie, Louis C. Barrett, Advanced Engineering Mathematics, McGraw Hill Book Co., New York
4	H.K. Dass and Er. Rajnish Verma, Higher Engineering Mathematics, S. Chand Publication
e-LEARNING RESOURCES:	
1	http://nptel.ac.in/courses.php?disciplineID=111
2	http://www.class-central.com/subject/math(MOOCs)
3	VTU e-Shikshana Program
4	VTU EDUSAT Program

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.

CIE: The CIE has three components – CIE - theory component, assignment and group activity. Students have to score a minimum of 40% Marks in the total of CIE - theory, assignment and group activity components put together to take SEE.

SEE: Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.

****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)		**Max. Marks**	**Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)**
Theory	**Weightage of CIE1 and CIE2 Tests or CIE3**	**50**	**20**
	TOTAL	**50**	**20**

QUESTION PAPER PATTERN (SEE)										
Q. No.	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**	**Q9**	**Q10**
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Apply the Statistical techniques to obtain or fit a curve for the specified data. This helps the students to learn the numerical part of estimating the curve
CO2	Employ the knowledge of probability models arising in the engineering field using basic concepts of probability, random variables and probability distributions
CO3	Develop the Fourier series to study the behavior of periodic functions and domain related applications.
CO4	Learn Fourier transforms and its applications to solve boundary value problem.
CO5	Analyze Z-transforms and its properties and apply the same to solve difference equations.

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	1	0	0	0	0	0	0	0	0	0	2	1	0
CO2	3	2	1	0	0	0	0	0	0	0	0	2	2	0
CO3	2	3	1	0	0	0	0	0	0	0	0	2	2	0
CO4	3	2	1	0	0	0	0	0	0	0	0	2	2	0
CO5	2	3	1	0	0	0	0	0	0	0	0	2	2	0

Mapping of CO's with Knowledge and Attitude Profile (WK)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	3	3	2	0	0	0	0	0	0
CO2	3	3	2	0	0	0	0	0	0
CO3	3	3	2	0	0	0	0	0	0
CO4	3	3	2	0	0	0	0	0	0
CO5	3	3	2	0	0	0	0	0	0

Mapping of CO's with Sustainable Development Goals (SDG)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1	0	0	0	3	0	0	0	0	1	0	0	0	0	0	0	0	0
CO2	0	0	0	3	0	0	0	0	1	0	0	0	0	0	0	0	0
CO3	0	0	0	3	0	0	0	0	2	0	0	0	0	0	0	0	0
CO4	0	0	0	3	0	0	0	0	2	0	0	0	0	0	0	0	0
CO5	0	0	0	3	0	0	0	0	2	0	0	0	0	0	0	0	0

Course Title	**DIGITAL SYSTEM DESIGN USING VERILOG**						
Course Code	**BSESVU302**						
Course Category	**IPCC (Integrated Professional Core Course)**						
Teaching - Learning Scheme & Credit	**L**	**T**	**P**	**S**	**Total**	**Total Teaching Hours**	**Credit**
	3	**0**	**1**	**0**	**4**	**42+0+28+50=120**	**4**
CIE Marks: 50	**SEE Marks: 50**		**Total Max. Marks: 100**			**Duration of SEE: 03 Hrs**	

Course Learning Objectives:	
CLO1	**Analyze and simplify** combinational logic circuits using Boolean algebra, Karnaugh maps, Quine-McCluskey minimization, and Don't Care conditions, and explain the basic Verilog design flow, data types, modules, and ports
CLO2	**Design and analyze** combinational logic circuits using MSI components such as adders, subtractors, comparators, decoders, encoders, and multiplexers, and describe them using Verilog data-flow modeling.
CLO3	**Analyze and design** sequential circuits using latches, master-slave JK flip-flops, characteristic equations, and registers, and implement procedural assignments using Verilog behavioral modeling.
CLO4	**Analyze and design** binary ripple counters, synchronous binary counters, and shift-register-based counters, and develop their Verilog behavioral descriptions using conditional statements, multiway branching, and loops.
CLO5	**Design and implement** synchronous mod-n counters using T, JK, D, and SR flip-flops, and model sequential circuits using Verilog structural description with gate-level constructs.

SYLLABUS	**No. of Hours**	**BTLs**
UNIT 1	**9**	**L1-L4**
PRINCIPLES OF COMBINATIONAL LOGIC: Definition of combinational logic, Generation of switching equations from truth tables, Karnaugh maps- up to 4 variables, Quine-McCuskey Minimization Technique. Quine-McCuskey using Don't Care Terms. **INTRODUCTION TO VERILOG**:Typical Design Flow, Data types, Modules, Ports.		
SELF-STUDY COMPONENTS: Boolean Algebra, De Morgan's theorem, Truth table, Canonical forms (SOP and POS). Basics about different Hardware Description Languages.		
UNIT 2	**9**	**L1-L4**
LOGIC DESIGN WITH MSI COMPONENTS AND PROGRAMMABLE LOGIC DEVICES: Binary Adders and Subtractors, Ripple Carry Adder, BCD Adder, Comparators, Decoders, Encoders, multiplex **VERILOG DATA FLOW DESCRIPTION:** Continuous assignments, Delays, Expressions, Operators, and operands, operator types, Examples.		
SELF-STUDY COMPONENTS: Practice designing logic functions using Decoders, Encoders, Multiplexers. Basics about Data flow modelling		
UNIT 3	**9**	**L1-L4**
FLIP-FLOPS: The basic Bistable Element, Latches, JK, SR T and D Flip-Flops, The Master-Slave Flip-flops (Pulse-Triggered flip-flops): JK Flip Flop, Characteristic equations. **VERILOG BEHAVIORAL DESCRIPTION:** Introduction, Procedural Assignments.		
SELF-STUDY COMPONENTS: Design of 4-bit Synchronous Counters using T, JK, D, SR Flip-Flops. Basics of Behavioral Modelling.		
UNIT 4	**9**	**L1-L4**
FLIP-FLOPS AND ITS APPLICATIONS: Registers-SISO,SIPO,PISO,PIPO, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers- Ring and Johnson Counter **VERILOG BEHAVIORAL DESCRIPTION:** Conditional statements, Multiway branching, Loops, eg.		
SELF-STUDY COMPONENTS: Learn to write Verilog code for Sequential circuits using Behavioral Modelling.		

UNIT 5	9	L1-L4
DESIGN OF SYNCHRONOUS COUNTER: Design of Synchronous Mod-N Counter using clocked T, JK, D and SR flip-flops. **VERILOG STRUCTURAL DESCRIPTION**: Gate types, Examples. (Gate level description only)		
SELF-STUDY COMPONENTS: Learn to write Verilog code for Sequential circuits using Behavioral & Structural Modelling.		
PRACTICAL COMPONENTS OF IPCC Using suitable simulation software, demonstrate the operation of the following circuits		
Experiments		
1.To simplify the given Boolean expressions and realize using Verilog program. 2.To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description. 3.To realize 4-bit ALU using Verilog program. 4.To realize the following Code converters using Verilog Behavioral description a) Gray to binary b) Binary to Gray 5.To realize using Verilog Behavioral description: 4:1 mux, 8:3 encoder, Priority encoder 6.To realize using Verilog Behavioral description: 1:4 Demux, 3:8 decoder, 2-bit Comparator 7.To realize using Verilog Behavioral description: Flip-flops: a) JK b) SR 8.To realize using Verilog Behavioral description: Flip-flops: a) T b) D		
Demonstration Experiments		
9.Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps). 10.Verilog programs to interface a Relay or ADC to the FPGA/CPLD and demonstrate its working. 11.Verilog programs to interface DAC to the FPGA/CPLD for Waveform generation. 12.Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.		
TEXT BOOKS:		
1	Digital Logic Applications and Design by John M Yarbrough, Thomson Learning,2006.	
2	Digital Principles and Design by Donald D Givone, McGraw Hill, 2017.	
3	Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar, 2nd Edition 2003, Prentice Hall.	

REFERENCE BOOKS:	
1	Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning,2013.
2	Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2010.
3	Fundamentals of HDL, by Cyril P R, Pearson/Sanguine, 2010.
e-LEARNING RESOURCES:	
1	Hardware Modeling using Verilog https://nptel.ac.in/courses/106105165
2	Digital Design with Verilog https://nptel.ac.in/courses/106103358

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each.
The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.
CIE: The CIE has two components – CIE - theory component and CIE – laboratory component.
Students have to score a minimum of 40% Marks in the total of CIE - theory and CIE – laboratory components put together, provided students have to score a minimum of 40% marks in CIE laboratory component alone to qualify to take SEE.
Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.
****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)		**Max. Marks**		Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Theory	**Weightage of CIE1 and CIE2 Tests or CIE3**	**30**		**12**
Laboratory components	Rubrics for experiment are added, then taken average	**10**	**20**	**08**
	Lab CIE	**10**		
	TOTAL	**50**		**20**

QUESTION PAPER PATTERN (SEE)										
Q. No.	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**	**Q9**	**Q10**
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	**Analyze and simplify** combinational logic circuits using Boolean algebra, Karnaugh maps, and Quine-McCluskey minimization techniques, and understand the fundamentals of Verilog HDL.
CO2	**Design and analyze** combinational logic circuits using MSI components such as adders, subtractors, comparators, decoders, encoders, and multiplexers, using Verilog data-flow modeling.
CO3	**Analyze and design** sequential circuits using latches, flip-flops, and registers, and implement sequential logic using Verilog behavioral modeling.
CO4	**Design and analyze** ripple counters, synchronous counters, and shift-register-based counters using appropriate sequential design techniques and Verilog behavioral constructs.
CO5	**Design and implement** synchronous mod-n counters using different types of flip-flops and describe sequential circuits using Verilog structural modeling at the gate level.

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	**PO 1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	2		1							2	2	
CO2	3	3	3	1	3							2	3	
CO3	3	3	3	1	3							2	3	
CO4	3	3	3	2	3				1		1	2	3	
CO5	3	3	3	2	3				1		2	2	3	

Mapping of CO's with Knowledge and Attitude Profile (WK)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	**WK1**	**WK2**	**WK3**	**WK4**	**WK5**	**WK6**		**WK7**		**WK8**		**WK9**		
CO1	0	3	3	2	0	1		0		0		0		
CO2						0	2	3	3	3	2	0	0	0
CO3	0	2	3	3	3	2	0		0		0			
CO4	0	3	3	3	2	3	0		0		0			
CO5	0	2	3	3	3	3	0		0		0			

Mapping of CO's with Sustainable Development Goals (SDG)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO/SDG	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**
CO1	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0
CO2	0	0	0	2	0	0	0	0	1	0	0	0	0	0	0	0	0
CO3	0	0	0	2	0	0	0	0	1	0	0	0	0	0	0	0	0
CO4	0	0	0	2	0	0	0	0	1	0	0	0	0	0	0	0	0
CO5	0	0	0	2	0	0	0	0	1	0	0	0	0	0	0	0	0

Course Title	NETWORK ANALYSIS						
Course Code	1BSEST303						
Course Category	PCC (Professional Core Course)						
Teaching - Learning Scheme & Credits	L	T	P	S	Total	Total Teaching Hours	Credits
	3	2	0	0	5	42+28+0+50=120	4
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	Understand and apply fundamental circuit laws and theorems, such as Ohm's Law, Kirchhoff's Laws, and network theorems, in the analysis of both DC and AC circuits
CLO2	Analyze and solve electrical networks systematically using mesh and nodal analysis techniques.
CLO3	Examine the transient behavior of RL,RC and RLC circuits under DC excitation and determine initial and final conditions
CLO4	Apply Laplace Transform methods for the analysis of electrical circuits and the solution of circuit-related differential equations
CLO5	Evaluate and interpret two-port network parameters (Z, Y, h, and T) and understand the relationships among them in various electrical systems.

SYLLABUS	No. of Hours	BTLs
UNIT 1	**(9L + 5T)**	**L1-L4**

BASIC NETWORK ANALYSIS

Active and passive elements, Ideal and practical voltage and current sources, Independent and dependent (controlled) sources, Source transformation and source shifting techniques, **Network reduction methods**: Star–Delta (Y–Δ) and Delta–Star (Δ–Y) transformation.

Loop (Mesh) and Node analysis for DC and AC circuits with independent and dependent sources, Super-mesh and Super-node concepts and applications.

SELF-STUDY COMPONENTS:

- Applications of active and passive circuit elements in electrical systems.
- Practical implementation of dependent (controlled) sources.
- Software-based analysis of DC and AC networks using MATLAB/Simulink, LTspice, or PSpice.
- Applications of Star–Delta transformation in power distribution networks.
- Comparative study of Mesh Analysis and Node Analysis techniques.
- Real-world applications of Super-mesh and Super-node methods in electrical circuit analysis.

UNIT 2	*(8L + 5T)*	L1-L4

NETWORK THEOREMS:

Superposition Theorem, Reciprocity Theorem, Thevenin's Theorem, Norton's Theorem, Maximum Power Transfer Theorem, Millman's Theorem. Analysis of linear DC and AC electrical networks using network theorems with independent and dependent sources.

SELF-STUDY COMPONENTS:

- Applications of Superposition, Thevenin's and Norton's Theorems in practical electrical circuits.
- Millman's Theorem and its applications in multi-source electrical networks.
- Comparison of different network theorems and their suitability for circuit analysis.
- Application of Maximum Power Transfer Theorem in electrical and electronic systems.
- Analysis of DC and AC networks using simulation tools such as MATLAB/Simulink, LTspice or PSpice.
- Real-time applications of network theorems in power systems and electrical engineering circuits.

UNIT 3	(9L+9T)	L1-L4

TRANSIENT BEHAVIOUR AND INITIAL CONDITIONS:

Concept of initial conditions in electrical networks, Initial conditions of resistor, inductor and capacitor, Continuity conditions of inductor current and capacitor voltage, procedure for evaluating initial conditions, Behaviour of circuit elements under DC switching conditions and their representation, Evaluation of initial and final values in R-L, R-C and R-L-C circuits, transient response of series R-L, R-C and R-L-C circuits for DC excitation with initial conditions, classical solutions for first and second order differential equations for series R-L, R-C and R-L-C electrical networks.

SELF-STUDY COMPONENTS:

- Applications of transient response in electrical and electronic systems.
- Use of MATLAB/Simulink, LTspice or PSpice for transient analysis of electrical circuits.
- Comparison of first-order and second-order circuit responses.
- Effect of circuit parameters (R, L and C) on transient response.
- Practical applications of charging and discharging circuits.
- Analysis of natural and forced responses of electrical networks.

UNIT 4	(9L+5T)	L1-L5

LAPLACE TRANSFORMATION AND ITS APPLICATIONS TO ELECTRIC CIRCUITS:

Introduction, properties of Laplace transform, Laplace transform of a derivative, integral, common forcing functions, initial value and final value theorems, time displacement theorem, Laplace Transform of a network and time domain solution for R-L, R-C, and R-L-C networks for DC excitations, and pulse input.

Waveform Synthesis: Introduction, Basic types of special signals, Laplace transformation of special signal waveforms, Problems.

SELF-STUDY COMPONENTS:

- Analyse the transient response of an RL circuit using both classical and Laplace methods and compare the results.
- Simulate an RC charging circuit under step and pulse excitation using MATLAB or LTspice.
- Develop a MATLAB program to compute Laplace and inverse Laplace transforms of common functions.
- Generate and analyse unit step, ramp, impulse, and pulse waveforms using MATLAB.
- Compare analytical and simulation results for first-order and second-order circuits.
- Prepare a summary chart of important Laplace transform pairs and theorems.

UNIT 5	(7L+4T)	L1-L4

TWO PORT NETWORK:

Introduction to two-port networks, Characterization in terms of impedance, admittance, hybrid, and transmission parameters, parameter conversions, Interconnection of two-port networks – Symmetry and Reciprocity.

SELF-STUDY COMPONENTS:

- Study the concept, classification, and applications of two-port networks.
- Simulate a two-port network using MATLAB, LTspice, or Multisim and compare the results with analytical calculations.

TEXT BOOKS:

1	Hayt, Kemmerly and Durbin, "Engineering Circuit Analysis",10th Edition, TMH Publication, 2024.
2	M. E. Van Valkenburg,"Network Analysis",3rd Eedition, PHI publisher, 2009.
3	Charles K Alexander Matthew N O Sadiku, "Fundamentals of Electric Circuits",Mc Graw Hill, 5th Edition, 2022.

REFERENCE BOOKS:

1	Roy Choudhury,"Networks and systems", 2nd Edition, New Age International Publications, 2016.
2	Robert L and Boylestad "Introductory Circuit Analysis", 4TH edition, Pearson publisher, 2010.
3	M Nahvi and J A Edminister, "Electric Circuits", 2nd Edition, Schaum's Series , 2002.

e-LEARNING RESOURCES:

1	NPTEL (National Programme on Technology Enhanced Learning) o Website: https://nptel.ac.in o Courses: – *Basic Electrical Circuits* by Prof. Nagendra Krishnapura (IIT Madras) – *Network Analysis* by Prof. M. B. Patil (IIT Bombay)
2	MIT Open CourseWare o Website: https://ocw.mit.edu o Course: *Circuits and Electronics* (6.002)
3	All About Circuits • Website: https://www.allaboutcircuits.com • Features: In-depth tutorials, forum discussions, circuit simulation tools, calculators.

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.

CIE: The CIE has three components – CIE - theory component, assignment and group activity. Students have to score a minimum of 40% Marks in the total of CIE - theory, assignment and group activity components put together to take SEE.

SEE: Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.

****Self-Study** The self-study component shall not be included in the SEE. For the CIE, a **5-mark question** from the self-study component may be included as either **Question 2(b)** or **Question 2(c)**.

CONTINUOUS INTERNAL EVALUATION (CIE)		**Max. Marks**	**Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)**
Theory	**Weightage of CIE-1 and CIE-2 Tests or CIE-3**	**50**	**20**
TOTAL		**50**	**20**

QUESTION PAPER PATTERN (SEE)										
Q. No.	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**	**Q9**	**Q10**
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Apply Kirchhoff's laws to perform loop and nodal analysis for resistive and reactive networks.
CO2	Apply the basic electrical laws and theorems to simplify and analyse the complex electric circuits
CO3	Analyse and evaluate the initial and final conditions of RL, RC and RLC circuits and determine the transient response of electrical circuits.
CO4	Apply Laplace Transform techniques to solve first and second-order electrical circuits in the s-domain and analyze the electrical waveforms using standard test signals
CO5	Determine the parameters of two-port networks (Z, Y, h, and T) and analyse their behaviour in interconnected networks.

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	1	1	2							3	2	1
CO2	3	3	2	2	2							3	2	1
CO3	3	3	2	2	2							3	3	1
CO4	3	2	2	2	2							3	3	2
CO5	3	3	2	2	2		1					3	3	2

Mapping of CO's with Knowledge and Attitude Profile (WK)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO/SDG's	**WK1**	**WK2**	**WK3**	**WK4**	**WK5**	**WK6**	**WK7**	**WK8**	**WK9**
CO1	3	3	2	1					1
CO2	3	3	3	2	1				1
CO3	3	3	3	2	2	1			1
CO4	3	3	2	2	2	1	1		1
CO5	3	3	3	3	2	1	1	1	2

Course Title	ANALOG ELECTRONICS AND LINEAR INTEGRATED CIRCUITS						
Course Code	1BSEST304						
Course Category	PCC (Professional Core Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	3	0	0	3	3	45+0+0+45=90	3
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	Examine the AC behavior and frequency response of BJT amplifiers and hybrid equivalent model, including the qualitative study frequency effects such as Miller effect.
CLO2	Analyze Power amplifier circuits in different modes of operation.
CLO3	Understand types of MOSFET biasing and demonstrate the use of MOSFET amplifiers.
CLO4	Construct various electronic circuits using OPAMPs and different types of active filters.
CLO5	Explain the working principle, block diagram, and pin configuration of IC 565 PLL, and analyze its applications.

SYLLABUS	No. of Hours	BTLs
UNIT 1	**09**	**L1-L4**
BJT AC Analysis: Voltage Divider Configuration, hybrid Equivalent model. **BJT Frequency Response:** Low frequency analysis, low frequency response of BJT amplifier, Miller effect capacitance, High frequency response of BJT amplifiers- study of capacitors affecting frequency response. (Qualitative analysis).		
SELF-STUDY COMPONENTS: **BJT AC** Analysis **– Voltage Divider Configuration:** BJT (basic transistor amplifier model) and its comparison with hybrid model. Effect of load impedance and source resistance on gain. Cascaded BJT amplifier configurations (brief overview).		
UNIT 2	**09**	**L1-L4**
Feedback Amplifier: Feedback concepts, feedback amplifier types-- Voltage series, Voltage-shunt, Current Series, and Current Shunt Feedback. **Oscillator**: Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator. **Power Amplifiers**: Introduction and amplifier types, Transformer – Coupled class A Amplifier, Transformer – coupled Push – Pull circuits, Complementary –Symmetry Circuits, Amplifier distortion, Class C Amplifier.		
SELF-STUDY COMPONENTS: Effect of feedback on input/output impedance (qualitative). Comparison of Class A, B, AB, C amplifiers with efficiency calculations. Heat sinks and thermal considerations in power amplifiers.		
UNIT 3	**09**	**L1-L4**
MOSFET Biasing in MOS Amplifier Circuits: Fixing VGS, Fixing VG, Drain to Gate Feedback Resistor. **Small Signal Operation and Modelling:** The DC Bias Point, Signal Current in Drain, Voltage Gain, Small Signal Equivalent Circuit Models, Transconductance, The T Equivalent Circuit Model. **MOSFET Amplifier Configuration:** Basic Configurations, Characterizing Amplifiers, CS Amplifier with And Without Source Resistance, The Common Gate Amplifier, Source Follower.		
SELF-STUDY COMPONENTS: JFET biasing techniques (fixed bias, self-bias, voltage-divider bias). FET small-signal model and parameters (gm, rd). Applications of MOSFET as a switch in digital circuits.		
UNIT 4	**09**	**L1-L4**
Operational amplifier: Introduction, block diagram and parameters definition. **Op- amp applications:** Difference amplifier, instrumentation amplifier. Sample and Hold circuit, Active filters- LP, HP, BP, BR.		
SELF-STUDY COMPONENTS:		

Ideal vs practical op-amp characteristics (CMRR, slew rate, offset voltage). Summing and integrator/differentiator circuits. Design considerations for instrumentation amplifiers in sensor applications.		
UNIT 5	**09**	**L1-L4**
Op-amp comparator: Zero crossing detectors and Schmitt trigger-inverting mode. Converter: A/D – Successive approximation, flash ADC, D/A - Weighted R-2R ladder DAC. **IC 565 – Phase Locked Loop (PLL):** Introduction to PLL, Block diagram, Pin diagram and description, Operating Principle, Operation of Principle, Applications.		
SELF-STUDY COMPONENTS: Comparator circuit and applications. Dual-slope ADC working principle (brief). IC 565 PLL pin configuration and practical applications such as Free running Oscillator and FM applications.		

TEXTBOOKS:	
1	Robert L. Boylestad and Louis Nashelsky, "Electronic Devices and Circuit Theory", 11th Edition, Pearson Education, 2015.
2	D. Roy Choudhury, Shail B Jain," Linear Integrated Circuits", 4th Edition, New Age International limited, 2019.
3	Adel S. Sedra & Kenneth C. Smith, "Micro Electronic Circuits", 7th Edition, Oxford University Press, 2017.

REFERENCE BOOKS:	
1	Muhammad Rashid, "Microelectronics Circuits Analysis and Design", 2nd edition, Cengage Learning, 2014.
2	S. Salivahanan N. Suresh, "Electronic Devices and Circuits",3rd edition, Mc Graw Hill publisher, 2013.
3	Millman and Halkias, "Electronic Devices and Circuits", 4th Edition, Mc Graw Hill, 2015.
4	Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, Pearson, 4th Edition 2015
e-LEARNING RESOURCES:	
1	https://www.tutorialspoint.com/electronic_circuits/electronic_circuits_introduction.htm
2	https://www.electronicshub.org/tutorials/4.
3	https://nptel.ac.in/courses/108102112
4	http://nptel.vtu.ac.in/econtent/courses/EEE/10EE54/index.php

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.

CIE: The CIE has three components – CIE - theory component, assignment and group activity. Students have to score a minimum of 40% Marks in the total of CIE - theory, assignment and group activity components put together to take SEE.

SEE: Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.

****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)		**Max. Marks**	**Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)**
Theory	**Weightage of CIE1 and CIE2 Tests or CIE3**	**50**	**20**
	TOTAL	**50**	**20**

QUESTION PAPER PATTERN (SEE)										
Q. No.	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**	**Q9**	**Q10**
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Describe the working principle, fundamental characteristics of various semiconductors devices such as BJT, FET, MOSFETs, and operational amplifiers in electronic circuits.
CO2	Understand and Analyze various Power Amplifiers and FET biasing Techniques, evaluate performance parameters.

CO3	Analyze and Design FET Amplifier Circuits using Small Signal Models and appropriate Biasing Techniques and Evaluate Parameters.
CO4	Analyze various filter circuits using linear integrated circuits.
CO5	Understand the Structure and Parameters of Op-amp and Analyze its applications in Analog Signal Processing.

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	**3**	**2**	0	**2**	0	0	**1**	0	0	**1**	**1**	0	0	**1**
CO2	**3**	**2**	0	**2**	0	**1**	0	**2**	0	0	0	**2**	0	0
CO3	0	0	**3**	0	**2**	0	**1**	0	0	0	**1**	0	0	0
CO4	0	0	**3**	**2**	0	0	0	0	**1**	0	0	0	**3**	0
CO5	**3**	**3**	**2**	**2**	0	0	0	0	0	0	**2**	**1**	**3**	0

Mapping of CO's with Knowledge and Attitude Profile (WK)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	**2**	**2**	**3**	**3**	**1**	**1**	0	0	**2**
CO2	**2**	**2**	**3**	**3**	**2**	**1**	0	0	**2**
CO3	**2**	**1**	**3**	**3**	**1**	**1**	0	0	**2**
CO4	**1**	**2**	**2**	**3**	**3**	**2**	**1**	**1**	**1**
CO5	**1**	**1**	**2**	**3**	**3**	**2**	**1**	**1**	**1**

Mapping of CO's with Sustainable Development Goals (SDG)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1	0	0	0	**3**	0	0	**1**	0	**2**	0	0	0	0	0	0	0	0
CO2	0	0	0	**3**	0	0	**1**	**1**	**2**	0	0	0	0	0	0	0	0
CO3	0	0	0	**3**	0	0	**2**	0	**2**	0	0	0	0	0	0	0	0
CO4	0	0	0	**3**	0	0	**2**	0	**3**	0	0	**1**	0	0	0	0	0
CO5	0	0	0	**3**	0	0	**2**	**1**	**3**	0	0	**1**	0	0	0	0	0

Course Title	Fundamentals of Signal Processing						
Course Code	1BVL305						
Course Category	PCC (Professional Core Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	3	0	0	3	3	45+0+0+45=90	3
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	Identify and characterize different classes of signals and systems
CLO2	Analyze the signals in time and frequency domain for non-periodic signals
CLO3	Characterize LTI systems in the frequency domain
CLO4	Compute discrete Fourier transform efficiently
CLO5	Implement discrete time systems and basic signal processing algorithms

SYLLABUS	No. of Hours	BTLs
UNIT 1	**8**	**L1-L4**
Introduction to Signals and Systems: Definition of signals and systems, Classification of signals, Basic Operations on signals, Elementary signals, Overview of Specific Systems, Properties of Systems, The convolution sum Convolution sum evaluation procedure (Sections 1.1 to 1.8, 2.1-2.3 of Textbook 1)		
SELF-STUDY COMPONENTS: convolution sum Convolution problems		
UNIT 2	**8**	**L1-L4**
Frequency Analysis of Signals: The concept of frequency in continuous time and discrete time signals, The Fourier Transform for Discrete Time Aperiodic Signals, Energy Density Spectrum of Aperiodic Signals, Relationship of the Fourier Transform to the z-transform (Sections 4.1, 4.3.3, 4.3.6 of Textbook 2)		
SELF-STUDY COMPONENTS: The Fourier Transform for Discrete Time Aperiodic Signals and periodic signal problems		
UNIT 3	**8**	**L1-L4**
Frequency Domain Analysis of LTI Systems: Frequency Response of a system with a rational system function, Computation of frequency response function, Ideal Filter Characteristics, Lowpass, Highpass, and Band pass filters, Digital Resonators, Notch Filters, Comb Filters, All pass filters (Sections 5.2-5.3, 5.4.1-5.4.5 of Textbook 2)		
SELF-STUDY COMPONENTS: Problems on Low pass, High pass and other filter.		
UNIT 4	**10**	**L1-L4**
Discrete Fourier Transform: Ideal sampling and reconstruction of continuous-time signals, Discrete-Time Processing of Continuous-Time Signals, Frequency-Domain Sampling and Reconstruction of discrete-time signals, Discrete Fourier Transform, DFT as a linear transformation, properties of DFT: Time & Frequency shift, time scaling, convolution, Parsevals theorem, Spectral analysis using DFT. Fast Fourier Transform: Radix-2 four point DIT (Sections 7.1-7.2, 8.1.1, 8.1.2, 8.1.3 of Textbook 2)		
SELF-STUDY COMPONENTS: Problems on DFT properties and FFT algorithms		
UNIT 5	**9**	**L1-L4**
Implementation of Discrete-Time Systems: Structures for realization of discrete-time systems, Structures for FIR systems: Direct form, cascade form, Structure for IIR Systems: Direct-Form, Cascade form and Parallel form (Sections 9.1, 9.2.1, 9.2.2, 9.3.1, 9.3.3, 9.3.4)		
SELF-STUDY COMPONENTS: Examples on Filter realizations		

TEXT BOOKS:	
1	**Simon Haykin & Barry Van VeenJohn,** "Signals and Systems**",** 2nd Edition, Wiley & Sons
2	**John G. Proakis and Dimitris G. Manolakis**, "Digital Signal Processing: Principles, Algorithms, and Applications", 4th Edition, Pearson / Prentice Hall.

REFERENCE BOOKS:	
1	**Alan V. Oppenheim, Alan S. Willsky, and S. Hamid Nawab** – "*Signals and Systems"*, Pearson / Prentice Hall.
2	**Alan V. Oppenheim and Ronald W. Schafer** – "*Discrete-Time Signal Processing"*, Pearson.
e-LEARNING RESOURCES:	
1	**MIT OpenCourseWare (Res.6-007)** **Instructor:** Prof. Alan V. Oppenheim (author of the standard textbook on the subject). **Highlights:** Original video lectures, lecture notes, assignment sets, and solutions covering continuous and discrete-time signals..
2	**NPTEL (India)** **Instructors:** Professors from IIT Bombay, IIT Kharagpur, and IIT Delhi. **Highlights:** Deep, exam-oriented lecture series covering the full engineering curriculum with detailed mathematical derivations.

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.

CIE: The CIE has three components – CIE - theory component, assignment and group activity. Students have to score a minimum of 40% Marks in the total of CIE - theory, assignment and group activity components put together to take SEE.

SEE: Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.

****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)		Max. Marks	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Theory	**Weightage of CIE1 and CIE2 Tests or CIE3**	**50**	**20**
	TOTAL	**50**	**20**

QUESTION PAPER PATTERN (SEE)										
Q. No.	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**	**Q9**	**Q10**
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:

CO1	**Analyze basic signals and system properties in the time domain.***Classify continuous and discrete-time signals and systems, perform basic signal operations, and evaluate system responses using the linear convolution sum.* **(Bloom's Level: L1–L4)**
CO2	**Apply frequency-domain techniques to discrete-time signals.***Analyze discrete-time signals using the Discrete-Time Fourier Transform (DTFT), determine the energy density spectrum, and evaluate relationships between the Fourier Transform and the z-transform.* **(Bloom's Level: L1–L3)**
CO3	**Design and evaluate frequency response characteristics of LTI systems.***Analyze system responses using rational system functions, evaluate ideal filter behavior, and synthesize specific filter structures such as lowpass, highpass, bandpass, resonators, notch, comb, and all-pass filters.* **(Bloom's Level: L2–L4)**
CO4	**Implement Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT) algorithms.***Apply sampling and reconstruction principles, leverage DFT properties for spectral analysis and linear filtering, and compute DFT efficiently using Radix-2 DIT-FFT algorithms.* **(Bloom's Level: L2–L4)**
CO5	**Realize structural representations for discrete-time LTI systems.***Construct and compare Direct Form, Cascade Form, and Parallel Form realizations for FIR and IIR digital filter structures.* **(Bloom's Level: L2–L4)**

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	0	0	0		0	0	0	0	3	1	0
CO2	3	3	2	0	0	0	0	0	0	0	0	3	2	0
CO3	3	3	3	0	0	0	0	0	0	0	0	3	3	0
CO4	3	3	3	0	0	0	0	0	0	0	0	3	2	0
CO5	3	3	3	0	0	0	0	0	0	0	0	3	3	0

Mapping of CO's with Sustainable Development Goals (SDG)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CO2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CO3	0	0	1	3	0	0	0	2	3	0	1	0	0	0	0	0	1
CO4	0	0	2	3	0	0	1	2	3	0	2	0	1	1	0	0	1
CO5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mapping of CO's with Knowledge and Attitude Profile (WK)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	0	3	3	00	0	0	0	0	0
CO2	0	3	3	0	0	0	0	0	0
CO3	0	2	3	0	0	0	0	0	0
CO4	0	3	3	0	0	0	0	0	0
CO5	0	2	2	0	0	0	0	0	0

Course Title	ANALOG ELECTRONICS AND LINEAR INTEGRATED CIRCUITS LAB LABORATORY						
Course Code	1SESTL306						
Course Category	PCCL (Professional Core Course Laboratory)						
Teaching - Learning Scheme & Credit	L	T	P	TW+SL	Total	Total Teaching Hours	Credit
	00	00	02	28	30	02	01
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	To provide practical exposure to design, setting up, and analyze various analog electronic and Op-Amp circuits.
CLO2	To design, set up, and analyze RC-coupled and feedback BJT amplifiers, and determine their gain, bandwidth, frequency response, and input/output impedance.
CLO3	To design and analyze power amplifier circuits (Class A and Class B) and characterize JFET amplifiers through their input/output characteristics.
CLO4	To measure and evaluate the performance of Op-Amp based circuits such as the difference amplifier and instrumentation amplifier.
CLO5	To design, test, and plot the frequency response of active filters and Examine the working of IC 565 PLL, and analyze its lock range and capture range for applications in FM.

Syllabus	
PART: A - CONVENTIONAL EXPERIMENTS	
1	**BJT Amplifiers:** Design and Verification of RC-Coupled amplifier, Determine gain, frequency response, input and output impedance.
2	**Feedback Amplifiers:** Design and Set-up the BJT Common Emitter Voltage Amplifier with Feedback and Determine the Gain, Bandwidth.
3	**Power Amplifiers:** Design and analysis of power amplifier circuits (Class A, Class B).
4	**Characteristics and design of JFET amplifier:** Plotting the input/output characteristics of JFET and Design of amplifier.
5	**Measurement of Op-Amp parameters:** Difference Amplifier and Instrumentation amplifier.
6	**Comparators:** i) Zero crossing detectors ii)Schmitt trigger circuit using Op–Amps.
7	**Converters:** Analog to Digital (ADC) i) Successive approximation ii)Flash ADC
8	**Converters:** Digital to Analog (DAC) Weighted R-2R ladder DAC
9	**Active filters:** Design and Test the Second Order Active Filters and Plot the Frequency Response: i) Low Pass Filter, ii) High Pass Filter
10	**Active filters:** i) Band Pass, ii) Band Reject.
11	**IC 565:** Frequency synthesis using IC 565.
12	**IC 565:** Applications of IC 565.
PART: B - TYPICAL OPEN-ENDED EXPERIMENTS	

Open-ended experiments are a type of laboratory activity where the outcome is not predetermined and students are given the freedom to explore, design, and conduct the experiment based on the problem statements as per the concepts defined by the course coordinator. It encourages creativity, critical thinking, and inquiry-based learning. **Course Project**: Students must do a mandatory course project (group size not more than 4 students) using to realize a functional analog circuit on PCB. A maximum of 5 marks shall be awarded for this project (to be evaluated along with the final internal test). Report to be submitted.	
1	Audio amplifier.
2	Electronic Pest Repellent Circuit.
3	Electronic Siren, Audiometer.

Teaching & Learning Process (Innovative Delivery Methods):	
1	Active Learning Techniques
2	Problem-Based Learning (PBL)
3	Team-Based Learning (TBL)
4	Hands-On Experiments and Simulations

TEXT BOOKS:	
1	Boylestad R. L. and L. Nashelsky, Electronic Devices and Circuit Theory, 10/e, Pearson Education India, 2009
2	Choudhury R., Linear Integrated Circuits, New Age International Publishers. 2008.

REFERENCE BOOKS:	
1	Millman J. and C. C. Halkias, Integrated Electronics: Analog and Digital Circuits and Systems, Tata McGraw-Hill, 2010.
2	Gayakward R. A., Op-Amps and Linear Integrated Circuits, PHI Learning Pvt. Ltd.,2012.
e-LEARNING RESOURCES:	
1	Analog Electronic Circuits Virtual Lab, IIT Kharagpur – Studies on BJT CE Amplifier — https://be-iitkgp.vlabs.ac.in/exp/ce-amplifier/simulation.html
2	Electronic Devices and Circuits Virtual Lab, IIT Kharagpur — http://vlabs.iitkgp.ac.in/ssd/index.html
3	Analog Electronic Circuits" by Prof. Shanthi Pavan, IIT Madras — https://onlinecourses.nptel.ac.in/noc26_ee65/preview
4	Multisim / PSpice – for BJT, FET, and Op-Amp circuit design and analysis
5	Proteus Design Suite – for circuit design, PCB layout, and simulation

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each.
The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.
CIE: The CIE has two components – CIE - theory component and CIE – laboratory component.
Students have to score a minimum of 40% Marks in the total of CIE - theory and CIE – laboratory components put together, provided students have to score a minimum of 40% marks in CIE laboratory component alone to qualify to take SEE.
Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.
****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)		**Max. Marks**	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Laboratory components	Rubrics for each experiment are added, then taken average	**30**	**20**
	Lab CIE	**20**	
	TOTAL	**50**	**20**

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Design and test simple Analog electronic circuits as per the specifications using discrete electronic components
CO2	Design and analyze Power Amplifiers.
CO3	Understand the FET circuits.
CO4	Measure the performance parameters of Op-Amp based difference and instrumentation amplifiers. Design and test the Op-amp applications.
CO5	Implement Timer circuits using IC Timer NE555

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	**3**	**2**	**2**	**1**	**3**	0	0	0	**2**	**2**	0	**2**	0	**1**
CO2	**3**	**2**	**3**	**2**	**2**	0	0	0	**1**	**1**	0	**2**	0	0
CO3	**2**	**2**	**3**	**2**	**2**	0	0	0	**1**	**1**	0	**1**	**2**	0
CO4	**2**	**2**	**2**	**3**	**2**	0	0	0	**1**	**1**	0	**1**	**3**	0
CO5	**2**	**2**	**3**	**2**	**3**	0	**1**	0	**2**	**2**	0	**1**	**1**	**2**

Mapping of CO's with Knowledge and Attitude Profile (WK)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	**1**	**1**	**2**	**2**	**2**	**3**	0	**1**	**1**
CO2	**1**	**1**	**2**	**3**	**3**	**3**	0	**1**	**1**
CO3	**1**	**1**	**2**	**3**	**3**	**3**	0	**1**	**1**
CO4	**1**	**1**	**2**	**3**	**2**	**3**	0	**1**	**1**
CO5	**1**	**1**	**2**	**3**	**3**	**3**	0	**2**	**1**

Mapping of CO's with Sustainable Development Goals (SDG)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1	0	0	0	**3**	0	0	0	0	**2**	0	0	0	0	0	0	0	0
CO2	0	0	0	**3**	0	0	**1**	0	**2**	0	0	0	0	0	0	0	0
CO3	0	0	0	**3**	0	0	**2**	0	**3**	0	0	0	0	0	0	0	0
CO4	0	0	0	**3**	0	0	0	0	**2**	0	0	0	0	0	0	0	0
CO5	0	0	0	**3**	0	0	**1**	0	**2**	0	0	0	0	0	0	0	0

Course Title	Simulation of Circuits and Devices						
Course Code	1BVLL307B						
Course Category	PCCL (Professional Core Course Laboratory)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	00	00	28	02	30	30	01
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objective	
CL01	Introduce EDA software tools for schematic capture, circuit entry, and spice-based simulation techniques.
CL02	Provide hands-on virtual experience in verifying foundational electrical laws and analyzing non-linear semiconductor device characteristics (Diode, Zener, BJT, MOSFET).
CL03	Enable students to design, simulate, and analyze active amplifier circuits, power conversion circuits (rectifiers), and passive frequency selective networks (filters).
CL04	Foster problem-solving, design thinking, and collaborative project development skills through a circuit design mini-project.

Syllabus

1. Familiarization with the schematic capture and circuit simulation software interface.
2. Draw the schematic of a resistor network and simulate it to verify Ohm′s Law.
3. Draw and simulate the schematic of a PN junction diode circuit to obtain its V–I characteristics.
4. Draw and simulate the schematic of a Zener diode circuit to study its characteristics.
5. Draw and simulate the schematic of a BJT circuit to obtain its output characteristics.
6. Draw and simulate the schematic of a MOSFET circuit to obtain its transfer characteristics.
7. Draw and simulate the schematic of a common-emitter amplifier and analyze its performance.
8. Draw and simulate the schematic of a common-source MOSFET amplifier and analyze its performance.
9. Draw and simulate the schematics of RC low-pass and high-pass filters and study their frequency and transient responses.
10. Draw and simulate the schematic of a half-wave rectifier and analyze its output waveform.
11. Draw and simulate the schematic of a full-wave bridge rectifier and analyze its output waveform.
12. Mini Project: Design, draw, simulate, and analyze a simple electronic circuit using schematic capture and circuit simulation software.

Teaching & Learning Process (Innovative Delivery Methods):
Simulation-Based Experiential Learning using SPICE tools for circuit analysis and verification.
Problem-Based Learning through parameter variation and performance evaluation of electronic circuits.
Collaborative Learning involving team-based circuit design, simulation, and result analysis.
Mini Project-Based Learning for application-oriented electronic circuit development and validation.

TEXT BOOKS:	
1	A. S. Sedra and K. C. Smith, Microelectronic Circuits, 7th ed. New York, NY, USA: Oxford University Press,2015.
2	R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory, 11th ed. Noida, India:Pearson Education, 2015

e-LEARNING RESOURCES:	
1	https://www.youtube.com/watch?v=_uQrJ0TkZlc
2.	https://www.youtube.com/watch?v=nLRL_NcnK-4
3.	https://www.youtube.com/playlist?list=PLdo5W4Nhv31bbKJzrsKfMpo_grxuLl8LU

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each.
The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.
CIE: The CIE has two components – CIE - theory component and CIE – laboratory component.
Students have to score a minimum of 40% Marks in the total of CIE - theory and CIE – laboratory components put together, provided students have to score a minimum of 40% marks in CIE laboratory component alone to qualify to take SEE .

Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks. **Self-Study Component should be not included for SEE & CIE.			
CONTINUOUS INTERNAL EVALUATION (CIE)		**Max. Marks**	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Laboratory components	Rubrics for each experiment are added, then taken average	**30**	**20**
	Lab CIE	**20**	
	TOTAL	**50**	**20**

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	**Apply** schematic capture software tools to draw electrical networks and verify fundamental laws and passive filter frequency responses.
CO2	**Analyze** the V–I characteristics and operational behaviors of fundamental semiconductor devices (PN junction diode, Zener diode, BJT, and MOSFET) through virtual simulation.
CO3	**Evaluate** the performance parameters (gain, transient, and frequency response) of single-stage BJT and MOSFET amplifier configurations and rectifier circuits.
CO4	**Design**, simulate, and troubleshoot a complete electronic circuit application to meet specified functional requirements for a mini-project.

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2	1	2	3	0	0	0	1	1	0
CO2	3	3	2	2	3	0	0	0	1	1	0
CO3	3	3	2	3	3	0	0	0	2	1	0
CO4	3	3	3	3	3	1	1	1	3	2	2

Mapping of CO's with Knowledge and Attitude Profile (WK)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	0	3	2	0	0	3	0	0	0
CO2	3	0	3	3	0	2	0	0	0
CO3	0	3	0	3	0	2	0	2	0
CO4	0	0	3	3	2	2	0	1	1

Mapping of CO's with Sustainable Development Goals (SDG)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1	0	0	0	2	0	0	0	0	2	0	0	1	0	0	0	0	0
CO2	0	0	0	2	0	0	0	0	2	0	0	1	0	0	0	0	0
CO3	0	0	0	3	0	0	0	0	3	0	0	2	0	0	0	0	0
CO4	0	0	0	3	0	0	0	0	3	0	0	3	0	0	0	0	0

Course Title	Complex Analysis and Numerical Techniques (EE,EC, ET, EI, VLSI)						
Course Code	1BMAT401D						
Course Category	ASC (Applied Science Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	03	0	0	4	3	42+0+50=92	3
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:
This course is proposed to impart to the students the skills to identify and solve problems in their field of study involving the application of numerical and probability distribution techniques.

SYLLABUS	No. of Hours	BTLs
UNIT 1	**8**	**L1-L4**
Functions of a Complex Variable: Definitions of continuity, differentiability and analytic functions, Cauchy-Riemann equations in Cartesian and polar forms, properties of analytic functions: Harmonic functions and orthogonality. Construction of analytic functions (Milne-Thomson method).		
SELF-STUDY COMPONENTS: Complex potential**.** Flow problems.		
UNIT 2	**8**	**L1-L4**
Conformal Transformation: Bilinear Transformations, Discussion of transformations: $w = z^2$, $w = e^z$ and $w = z + 1/z \ (z \neq 0)$. **Complex Integration:** Complex line integrals-Cauchy's theorem and Cauchy's integral formula. Poles and Residues, Residue theorem (without proof).		
SELF-STUDY COMPONENTS: Complex integration in fluid dynamics.		
UNIT 3	**8**	**L1-L4**
Numerical Methods: Numerical solution of simultaneous first order ordinary differential equations using Picard's method and Runge-Kutta method, Numerical solution of ordinary differential equations of second order using Runge-Kutta method and Milne's method (No derivations).		
SELF-STUDY COMPONENTS: Runge-Kutta method of third-order.		
UNIT 4	**8**	**L1-L4**
Numerical Solutions of Partial Differential Equations: Solutions of Laplace and Gauss-Seidel method, one-dimensional heat equation-Bendre-Schmidt method and Crank-Nicholson method. Wave Equation-Finite difference method.		
SELF-STUDY COMPONENTS: Solutions of Laplace and Poisson equations- Jacobi's method.		
UNIT 5	**10**	**L1-L4**
Joint Probability Distributions and Markov Chains: Introduction, Joint probability and Joint distribution of discrete random variables, Classification of Stochastic processes, Probability vector, Stochastic matrix, Regular stochastic matrix, Transition probabilities and Transition probability matrix, Markov chains.		
SELF-STUDY COMPONENTS: Joint probability and Joint distribution of continuous random variables. Joint Probability distribution in Mathematical modelling.		

TEXT BOOKS:
1. B. S. Grewal, Higher Engineering Mathematics, Khanna Publishers, New Delhi. 2. B. S. Grewal, Numerical methods in engineering and science, Khanna Publishers, New Delhi. 3. E. Kreyszig, Advanced Engineering Mathematics, John Wiley and Sons. 4. S.S. Sastry, Introductory methods of numerical analysis, PHI learning Pvt. Ltd. 5. H.C. Taneja, Advanced Engineering Mathematics, Volume I & II, I.K. International Publishing House Pvt. Ltd., New Delhi.

REFERENCE BOOKS:	
1	B. V. Ramana, Higher Engineering Mathematics, McGraw–Hill Education..
2	Srimanta Pal & Subodh C. Bhunia, Engineering Mathematics, Oxford University Press
3	C. Ray Wylie, Louis C. Barrett, Advanced Engineering Mathematics, McGraw Hill Book Co., New York
4	H.K. Dass and Er. Rajnish Verma, Higher Engineering Mathematics, S. Chand Publication
e-LEARNING RESOURCES:	
1	http://nptel.ac.in/courses.php?disciplineID=111
2	http://www.class-central.com/subject/math(MOOCs)
3	VTU e-Shikshana Program
4	VTU EDUSAT Program

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.

CIE: The CIE has three components – CIE - theory component, assignment and group activity. Students have to score a minimum of 40% Marks in the total of CIE - theory, assignment and group activity components put together to take SEE.

SEE: Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.

****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)		Max. Marks	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Theory	**Weightage of CIE1 and CIE2 Tests or CIE3**	**50**	**20**
	TOTAL	**50**	**20**

QUESTION PAPER PATTERN (SEE)										
Q. No.	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**	**Q9**	**Q10**
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Understand basic concepts of Complex functions, analytic functions, harmonic functions and orthogonality of complex valued functions.
CO2	Analyze the concept of conformal mappings and Integrals of complex valued functions.
CO3	Demonstrate the existence of errors in numerical calculations and understand the methods to solve simultaneous and second order ODE's numerically

CO4	Apply numerical methods to identify and solve problems related to vibrations, automatic control systems, design etc.
CO5	Identify and solve problems involving random variables, probability distributions and Markov chains connected to digital signal processing, information code theory and structural engineering

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	1	0	0	0	0	0	0	0	2	1	0
CO2	3	2	2	1	0	0	0	0	0	0	0	2	2	0
CO3	3	3	2	2	2	0	0	0	0	0	0	2	2	1
CO4	3	3	3	2	2	0	0	0	0	0	1	3	2	1
CO5	3	3	2	2	2	0	0	0	0	0	1	2	3	1

Mapping of CO's with Knowledge and Attitude Profile (WK)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	2	3	2	1	0	0	0	1	0
CO2	2	3	2	2	0	0	0	1	0
CO3	1	3	2	2	1	1	0	2	0
CO4	2	3	3	2	2	1	0	2	0
CO5	1	3	2	2	1	1	0	2	0

Mapping of CO's with Sustainable Development Goals (SDG)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1	0	0	0	3	0	0	0	0	2	0	0	0	0	0	0	0	0
CO2	0	0	0	3	0	0	0	0	2	0	0	0	0	0	0	0	0
CO3	0	0	0	3	0	0	0	0	3	0	0	0	0	0	0	0	0
CO4	0	0	0	3	0	0	0	0	3	0	0	0	0	0	0	0	0
CO5	0	0	0	3	0	0	0	0	3	0	0	0	0	0	0	0	0

Course Title	CMOS Digital VLSI Design						
Course Code	1BVL404						
Course Category	IPCC (Integrated Professional Core Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	3	0	1	0	4	45+0+30+45=120	4
CIE Marks: 50	SEE Marks:50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	Understand MOSFET device operation and CMOS fabrication technologies.
CLO2	Analyze CMOS circuits using RC models and estimate delay and power consumption.
CLO3	Model interconnects and design CMOS combinational circuits.
CLO4	Design CMOS sequential circuits.
CLO5	Analyze and design CMOS memory circuits and memory subsystems.

SYLLABUS	No. of Hours	BTLs
UNIT 1	**9**	**L1-L4**
Introduction to VLSI and MOS Transistor Theory Introduction to VLSI design: History and trends in VLSI, overview of CMOS logic, design abstraction and partitioning. MOS transistor fundamentals: MOS structure, operation of MOSFET, Enhancement mode, Depletion mode of a MOSFET. **Textbook 1: Chapter 1:** 1.1 to 1.4 and 1.6; **Chapter 2:** 2.1, 2.2, 2.3.1, 2.5		
SELF-STUDY COMPONENTS: Basic semiconductor fabrication steps (photolithography, oxidation, ion implantation, etching, and n-well/p-well processes). SPICE simulation of the MOSFET and CMOS inverter DC response or long-channel V-I plot		
UNIT 2	**8**	**L1-L4**
CMOS Fabrication and Layout Basics DC transfer characteristics of CMOS inverter. Overview of CMOS fabrication technology, n-well and p-well processes, twin-well technology. Basic fabrication steps in CMOS IC manufacturing. Layout design rules and stick diagrams. **Textbook 1: Chapter 1:** 1.5; **Chapter 3**: 3.1, 3.3.1 to 3.3.2		
SELF-STUDY COMPONENTS: Advanced Fabrication Technologies (Beyond Planar CMOS) , Silicon-on-Insulator (SOI) Technology, Bi-CMOS Technology, Photolithography & Etching Details, drawing stick diagrams and running DRC/LVS on standard gates CMOS Fabrication and Layout Basics		
UNIT 3	**9**	**L1-L4**
Delay and Power in CMOS Circuits Transient response of CMOS circuits: RC delay model for MOS circuits. Linear delay model and logical effort. Delay in logic gates. Power dissipation in CMOS Circuits: dynamic power, static power, leakage power. **Textbook 1: Chapter 4:** 4.1, 4.2, 4.3.1 to 4.3.6, 4.4.1 to 4.4.3; **Chapter 5:** 5.1. to 5.3		
SELF-STUDY COMPONENTS: Advanced delay optimization techniques, specialized power reduction strategies, or low-power design paradigms that extend beyond basic gate delay and dynamic/static power formulas.		
UNIT 4	**8**	**L1-L4**
Interconnect and Combinational Circuit Design Interconnect fundamentals: wire geometry, parasitic resistance, capacitance and inductance. Interconnect modeling and its impact on delay and energy. Cross-talk and signal integrity issues. CMOS combinational circuit design: static CMOS logic, pass transistor logic, transmission gate logic, introduction to SOI circuits. **Textbook 1: Chapter 6**: 6.1, 6.2.1 to 6.2.3, 6.3.1 to 6.3.3, 6.4.1 to 6.4.2; **Chapter 9:** 9.1, 9.2.1 to 9.2.3, 9.2.5, 9.5		
SELF-STUDY COMPONENTS: Comparison of Bulk CMOS vs. SOI CMOS (Partially Depleted vs. Fully Depleted SOI / UTBB-FDSOI), Parasitic Capacitance Reduction: How burying the oxide layer (SiO_2) reduces junction capacitance and eliminates latch-up, Floating Body Effect & History Effect.		
UNIT 5	**8**	**L1-L4**

Sequential Circuits and Memory Subsystems Sequential circuit design: CMOS latches and flip-flops, pulsed latches, resettable and enabled flip-flops, dual edge triggered flip-flops. Incorporating logic into latches and flip-flops. Array subsystems: SRAM cells, row and column circuitry. Read-only memories, content addressable memories, programmable logic arrays. **Textbook 1: Chapter 10**: 10.1, 10.3.1 to 10.3.6 **Chapter 12:** 12.1, 12.2.1 to 12.2.3, 12.4, 12.6, 12.7
SELF-STUDY COMPONENTS: Pulsed Latches vs. Flip-Flops, Specialized Registers, 6T SRAM Cell Dynamics, VLSI Testing

TEXT BOOKS:	
1	Neil H. E. Weste, David Harris "CMOS VLSI Design A Circuits and Systems Perspective" Pearson Education Publisher, Fourth Edition, 2015.
REFERENCE BOOKS:	
1	Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic "Digital Integrated Circuits A Design Perspective" Pearson Education Publisher, Second Edition, 2010.
2	John P Uyemura "Introduction to VLSI Circuits and Systems" Wiley Publication, 2002.
3	R. Jcob Baker, Harry W. Li and David E Boyce "CMOS Circuit Design, Layout, and Simulation" PHI, 1998
E-LEARNING RESOURCES:	
1	https://nptel.ac.in/courses/108107129
2	https://nptel.ac.in/courses/117106149

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each.
The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.
CIE: The CIE has two components – CIE - theory component and CIE – laboratory component.
Students have to score a minimum of 40% Marks in the total of CIE - theory and CIE – laboratory components put together, provided students have to score a minimum of 40% marks in CIE laboratory component alone to qualify to take SEE.
Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.
****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)		**Max. Marks**		Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Theory	**Weightage of CIE1 and CIE2 Tests or CIE3**	**30**		**12**
Laboratory components	Rubrics for experiment are added, then taken average	**10**	**20**	**08**
	Lab CIE	**10**		
	TOTAL	**50**		**20**

QUESTION PAPER PATTERN (SEE)										
Q. No.	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**	**Q9**	**Q10**
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

PRACTICAL COMPONENTS OF IPCC	
PART – A: FIXED SET OF EXPERIMENTS	
1	Study of MOS Transistor Characteristics: Plot I–V characteristics of NMOS and PMOS transistors. Determine threshold voltage and operating regions.
2	CMOS Inverter – DC Analysis: Design a CMOS inverter and obtain Voltage Transfer Characteristics (VTC). Determine switching threshold and noise margins.

3	Transient Analysis of CMOS Inverter: Perform transient simulation. Measure propagation delay, rise time, and fall time.
4	Power Analysis of CMOS Inverter: Analyze dynamic and static power dissipation. Study the effect of switching activity and load capacitance.
5	Layout of CMOS Inverter: Draw layout of CMOS inverter. Verify layout using Design Rule Check (DRC)., Extract RC, simulate the Circuit
6	CMOS NAND gate. Verify logical functionality. CMOS NOR Gate Design and Simulation: Design and simulate a 2-input CMOS NOR gate. Verify logical functionality.
7	Visual identification of building materials:,Bricks, Stones, Tiles, M-Sand, Bitumen, Fly-Ash, GGBS, Steel Bars of Various Sizes.
8	Layout Design of CMOS NAND Gate: Draw the standard cell layout of a 2-input CMOS NAND gate. Perform DRC and parasitic extraction and simulate
9	Transmission Gate Design: Design and simulate a CMOS transmission gate. Analyze bidirectional switching characteristics.
10	Multiplexer using Transmission Gates: Implement 2:1 multiplexer using transmission gates. Verify functionality through simulation.
11	Interconnect Modeling and RC Delay Analysis: Model interconnect resistance and capacitance. Analyze the effect of wire length on delay.
12	Design of CMOS D Latch: Design and simulate CMOS D latch. Analyze timing parameters.
13	Design of CMOS D Flip-Flop: Design and simulate edge-triggered D flip-flop. Measure propagation delay. 14.
14	Design of 6T SRAM Cell: Design and simulate 6-transistor SRAM cell.

PART: B - TYPICAL OPEN-ENDED EXPERIMENTS

Open-ended experiments are a type of laboratory activity where the outcome is not predetermined, and students are given the freedom to explore, design, and conduct the experiment based on the problem statements as per the concepts defined by the course coordinator. It encourages creativity, critical thinking, and inquiry-based learning.

1. CMOS Inverter Optimization Design a CMOS inverter and optimize transistor sizing to achieve: Minimum propagation delay, Improved noise margins, Reduced power dissipation Students compare the effect of different W/L ratios and load capacitances.
2. Design and Layout of a CMOS Standard Cell Design a complete standard cell (such as NAND, NOR, or XOR gate) including: Schematic design, Layout following design rules, Functional verification and delay analysis.
3. CMOS Full Adder Design Design and simulate a CMOS full adder circuit using any logic style such as: Static CMOS logic, Transmission gate logic, Compare transistor count, delay, and power consumption.
4. SRAM Cell Design and Analysis Design a 6-transistor CMOS SRAM cell and analyze: Read and write operation, Static noise margin, Effect of transistor sizing on stability.

Teaching & Learning Process (Innovative Delivery Methods):	
1	Active Learning Techniques
2	Problem-Based Learning (PBL)
3	Team-Based Learning (TBL)
4	Hands-On Experiments and Simulations

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each.
The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.
CIE: The CIE has two components – CIE - theory component and CIE – laboratory component.
Students have to score a minimum of 40% Marks in the total of CIE - theory and CIE – laboratory components put together, provided students have to score a minimum of 40% marks in CIE laboratory component alone to qualify to take SEE.
Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.
****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)	**Max. Marks**	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)

Laboratory components	Rubrics for each experiment are added, then taken average	**30**	**20**
	Lab CIE	**20**	
	TOTAL	**50**	**20**

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Understands semiconductor device operation and fabrication technology.
CO2	Evaluates delay and power characteristics of CMOS circuits.
CO3	Designs combinational CMOS logic considering interconnect effects.
CO4	Designs sequential CMOS circuits for digital systems.
CO5	Analyzes and designs CMOS memories with emphasis on performance and reliability.

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	PO 1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	0	1	2	0	1	0	0	0	1			
CO2	3	3	2	2	3	0	2	0	0	0	2			
CO3	3	3	3	2	3	0	1	0	1	1	2			
CO4	3	3	3	2	3	0	1	0	1	1	2			
CO5	3	3	3	3	3	0	2	1	1	1	1			

Mapping of CO's with Knowledge and Attitude Profile (WK)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	3	2	3	2	2	0	0	0	0
CO2	0	2	3	3	2	0	1	2	2
CO3	0	3	2	3	3	0	3	2	1
CO4	0	3	2	3	3	0	2	3	1
CO5	0	2	3	3	2	3	3	3	2

Mapping of CO's with Sustainable Development Goals (SDG)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1	0	0	0	3	0	0	0	2	3	0	0	1	0	0	0	0	0
CO2	0	0	0	3	0	0	0	2	3	0	0	2	0	0	0	0	0
CO3	0	0	0	3	0	0	0	3	3	0	0	2	0	0	0	0	0
CO4	0	0	0	3	0	0	0	3	3	0	0	2	0	0	0	0	0
CO5	0	0	0	3	0	0	0	3	3	0	0	3	0	0	0	0	0

Course Title	CONTROL SYSTEM						
Course Code	1BSEST403						
Course Category	PCC (Professional Core Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	3	2	0	0	5	42+28+0+50=120	4
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	Learn the type of System, dynamics of physical systems, classification of control system, analysis and design objective.
CLO2	Represent the system by a transfer function, block diagram reduction method, and Mason's gain formula.
CLO3	Learn time response analysis and demonstrate their knowledge of frequency response.
CLO4	Learn stability analysis of the system using Root locus, bode plot and Nyquist plot.
CLO5	Learn the concept of Compensator and controller.

SYLLABUS	No. of Hours	BTLs
UNIT 1	**14**	**L1-L4**
Introduction to Control Systems: Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems – Mechanical Systems, Electrical Systems, Analogous Systems. Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra and Signal Flow graphs.		
SELF-STUDY COMPONENTS: AC Servomotor, DC servomotor, Synchro Transmitter and Receiver		
UNIT 2	**14**	**L1-L4**
Time Response of feedback control systems: Standard test signals, Unit step response of First and Second order Systems. Time response specifications, Time response specifications of second order systems, steady state errors and error constants. Introduction to PI, PD and PID Controllers (excluding design).		
SELF-STUDY COMPONENTS: On–Off (Two-Position) Controller, Feedback and Feedforward Control System		
UNIT 3	**14**	**L1-L4**
Stability analysis: Concept of stability, necessary conditions for Stability, Routh- stability criterion, Relative stability criterion Root-Locus Techniques: Root locus concepts, Construction of root loci, Stability of System.		
SELF-STUDY COMPONENTS: Effect of Addition of open loop poles and zeros on root locus and stability, Root contour		
UNIT 4	**14**	**L1-L4**
Frequency domain analysis and stability using Bode plots: Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function.		
SELF-STUDY COMPONENTS: Compensator- RC Lead compensator and RC Lag compensator.		
UNIT 5	**14**	**L1-L4**
Frequency domain analysis and stability: Introduction to Polar Plots, Mathematical preliminaries, Nyquist Stability criterion, Nyquist plots.		
SELF-STUDY COMPONENTS: Position control system and Speed Control System		

TEXT BOOKS:	
1	J. Nagarath and MGopa1," ControlSystemsEngineering", NewAge International(p) Limited Publishers, 5 th Edition- 2005, ISBN:81-224-2008-7
2	Analysis and design of Control system using MATLAB by Rao V Dukkipati, New Age international (p) Limited Publishers,2006 Publication.

REFERENCE BOOKS:

1	K.Ogata,"Modem Control Engineering" Pearson .Education Asia I PHI, 4th Edition,2002.
2	K.ChannaVenkatesh and D. Ganesh Rao, "Control Systems", Sanguine TechnicalPublishers.
3	Chi-Tsong Chen, "Analog and Digital Control System Design Transfer-Function, State-Space, and Algebraic Methods", OUP, 2006.
e-LEARNING RESOURCES:	
1	https://nptel.ac.in/courses/107106081
2	https://onlinecourses.nptel.ac.in/noc24_ee65/preview

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.

CIE: The CIE has three components – CIE - theory component, assignment and group activity. Students have to score a minimum of 40% Marks in the total of CIE - theory, assignment and group activity components put together to take SEE.

SEE: Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.

****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)		**Max. Marks**	**Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)**
Theory	**Weightage of CIE1 and CIE2 Tests or CIE3**	**50**	**20**
	TOTAL	**50**	**20**

QUESTION PAPER PATTERN (SEE)										
Q. No.	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**	**Q9**	**Q10**
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Analyze physical systems and their mathematical models using differential equations, transfer functions, and system analogies.
CO2	Evaluate the effect of feedback on control systems by examining block diagrams, signal flow graphs, and overall system behavior.
CO3	Analyze the time response characteristics and steady-state performance of first- and second order control systems, including the influence of basic controllers.
CO4	Assess the stability and relative stability of control systems using Routh–Hurwitz criterion and root locus techniques.
CO5	Analyze control system stability and performance in the frequency domain using Bode, Polar, and Nyquist plots.

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	1	2	1	0	1	2	2	3	1			
CO2	3	3	2	2	1	3	1	2	3	2	1			
CO3	3	3	3	2	2	3	3	1	2	3	3			
CO4	3	3	2	3	2	3	2	3	2	3	2			
CO5	3	3	2	3	3	3	2	1	3	3	1			

Mapping of CO's with Knowledge and Attitude Profile (WK) **Strength of correlation:** Strongly related-3, Moderately related-2, Weakly related-1, Not related-0									
CO	**WK1**	**WK2**	**WK3**	**WK4**	**WK5**	**WK6**	**WK7**	**WK8**	**WK9**
CO1	2	3	3	2	0	1	0	0	0
CO2	0	2	3	3	1	2	0	0	0
CO3	0	2	3	3	2	2	0	0	0
CO4	0	2	3	3	1	2	0	1	0
CO5	0	2	3	3	1	2	0	1	0

Mapping of CO's with Sustainable Development Goals (SDG) **Strength of correlation:** Strongly related-3, Moderately related-2, Weakly related-1, Not related-0																	
CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1	0	0	0	3	0	0	2	1	2	0	1	0	1	0	0	0	0
CO2	0	0	0	3	0	0	2	2	3	0	1	0	1	0	0	0	0
CO3	0	0	1	3	0	0	3	2	3	0	2	1	2	0	0	0	0
CO4	0	0	1	3	0	0	3	2	3	0	2	1	2	0	0	0	0
CO5	0	0	1	3	0	0	3	2	3	0	2	1	2	0	0	0	0

Course Title	MICROCONTROLLERS						
Course Code	1BSESU402						
Course Category	IPCC (Integrated Professional Core Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	3	0	1	0	4	42+0+28+50=120	4
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	Understand ARM design philosophy and ARM processor architecture and fundamentals
CLO2	Learn the ARM Instruction set of ARM microcontroller and to learn the assembly programming
CLO3	Understand Thumb instructions of ARM controller
CLO4	Understand Various Interrupts and exception handling in ARM controller
CLO5	Learn interfacing and to write C-program for LED, Keyboard, LCD, DC motor, Stepper motor

SYLLABUS	No. of Hours	BTLs
UNIT 1	**9**	**L1-L4**
Basic Structure of Computers: Basic Operational Concepts, Bus Structures, Basic Performance Equation, Clock Rate, Performance Measurement **Input/ Output Organization**: Accessing I/O Devices, Direct Memory Access, Standard I/O Interfaces–PCI Bus, SCSI Bus, USB **ARM Embedded Systems**: Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software–Initialization (BOOT)code, Operating System, Applications.		
ARM Processor Fundamentals: ARM core data flow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions. **Self Study:** • Study the evolution of ARM processors and compare ARM with other processor architectures(8051, AVR, PIC). • Explore different ARM Cortex series (M, R, A) and their applications. • Read about modern embedded system applications in IoT, automotive, and consumer electronics.		
UNIT 2	**9**	**L1-L4**
Introduction to the ARM Instruction set: Introduction, Data processing instructions, Load-Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5 Extensions, Conditional Execution. **Self Study:** • Practice additional ARM assembly programs using an ARM simulator/Keil IDE. • Study ARM addressing modes and compare them with other RISC processors. • Explore optimization techniques using conditional execution.		
UNIT 3	**9**	**L1-L4**
Introduction to the THUMB instruction set: Introduction, THUMB register usage, ARM– THUMB interworking, Other branch instructions, Data processing instructions, Stack instructions, Software interrupt instructions.		
Efficient C Programming: Overview of C Compilers and optimization, Basic C Data types, C looping structures. **Self Study:** • Compare ARM and Thumb instruction sets in terms of code size and execution speed. • Learn compiler optimization options in Keil/GCC. • Develop simple embedded C programs demonstrating loops, arrays, and functions.		
UNIT 4	**9**	**L1-L4**
General Purpose Parallel I/O: Interface of LED's and switches, Seven Segment Led Display, LCD, Keypad, Relay and Buzzer, DC motor, Stepper motor. **Self Study:**		

• Study the datasheets of LEDs, LCDs, keypads, relays, DC motors, and stepper motors. • Watch demonstrations of ARM-based interfacing using LPC2148 or similar development boards. • Explore real-world applications of GPIO interfacing in automation and robotics.

UNIT 5	9	L1-L4
TIMER, ADC, DAC, UARTs: Timers and its modes of operations, 10-bit ADC, 10-bit DAC,UARTs, Serial Communication, Interrupt Controller, Interrupt Sources, External Interrupt, I^2C interface, SPI **Self Study:** • Study communication protocols such as UART, SPI, and I^2C through manufacturer application notes. • Compare serial communication protocols (UART vs SPI vs I^2C vs CAN). • Explore ARM-based applications involving sensors, ADC/DAC, and Internet of Things (IoT).		

TEXT BOOKS:	
1	Andrew N S loss, Dominic System and Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publisher, 1st Edition,2008.
2	LPC 2148 User Manual

REFERENCE BOOKS:	
1	ARM Assembly Language – Fundamentals and Techniques, William Hohl, CRC Press,2009
2	ARM Assembly language An Introduction, J.R.Gibson, Cengage Learning, 2010
e-LEARNING RESOURCES:	
1	Videos and Lecture Notes: http://www.nptel.ac.in
2	https://www.arm.com/resources/education/online-courses

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.
CIE: The CIE has two components – CIE - theory component and CIE – laboratory component. Students have to score a minimum of 40% Marks in the total of CIE - theory and CIE – laboratory components put together, provided students have to score a minimum of 40% marks in CIE laboratory component alone to qualify to take SEE.
Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.
****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)		**Max. Marks**		Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Theory	**Weightage of CIE1 and CIE2 Tests or CIE3**	**30**		**12**
Laboratory components	Rubrics for experiment are added, then taken average	**10**	**20**	**08**
	Lab CIE	**10**		
	TOTAL	**50**		**20**

QUESTION PAPER PATTERN (SEE)										
Q. No.	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**	**Q9**	**Q10**
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Understand RISC and ARM design philosophy, ARM processor architecture and the exception/interrupt handling mechanism including the vector table.
CO2	Analyze and write ARM instruction set programs including data processing, load-store, software interrupt, and program status register instructions, applying conditional execution and constant-loading techniques.
CO3	Interface general-purpose I/O peripherals — LEDs, switches, seven-segment display, LCD, keypad, relay, buzzer, DC motor, and stepper motor — with an ARM-based microcontroller.

CO4	Configure and program on-chip peripherals (Timers, ADC, DAC, UART, Interrupt Controller, I2C, and SPI)
CO5	Design a system, component or process as per needs and specifications using ARM controller

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	1	0	0	0	0	0	1	0	1	0	3
CO2	3	2	2	1	1	0	0	0	0	1	0	1	0	3
CO3	2	2	3	2	2	0	0	0	1	1	0	1	0	3
CO4	2	1	2	3	3	0	0	0	1	1	2	1	1	2
CO5	2	2	2	3	3	0	0	0	1	1	2	1	1	2

Mapping of CO's with Knowledge and Attitude Profile (WK)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	0	1	2	3	0	1	0	0	0
CO2	0	1	2	3	1	2	0	0	0
CO3	0	1	2	3	1	2	0	0	0
CO4	0	0	2	2	2	3	1	0	0
CO5	0	0	2	2	2	3	1	0	0

Mapping of CO's with Sustainable Development Goals (SDG)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
CO2	0	0	0	1	0	0	0	0	2	0	0	0	0	0	0	0	0
CO3	0	0	0	1	0	0	0	1	2	0	0	1	0	0	0	0	0
CO4	0	0	0	1	0	0	1	1	2	0	1	1	0	0	0	0	0
CO5	0	0	0	1	0	0	1	1	3	0	1	1	0	0	0	0	0

Course Title	Design for Test Lab						
Course Code	1BVLL405						
Course Category	PCCL (Professional Core Course Laboratory)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	0	0	30	0	30	30	1
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	Understand the fundamentals of VLSI testing, fault modeling, testing methodologies, and Automatic Test Equipment (ATE) used in semiconductor manufacturing.
CLO2	Develop the ability to analyze logic simulation, fault simulation, and testability measures for evaluating the quality and reliability of digital VLSI circuits.
CLO3	Apply Automatic Test Pattern Generation (ATPG) techniques and fault analysis methods to generate efficient test vectors for combinational and sequential circuits.
CLO4	Evaluate Built-In Self-Test (BIST) architectures, LFSR/MISR-based test techniques, memory BIST, and emerging low-power testing methodologies used in modern VLSI systems.scan architectures for improving circuit testability.

Syllabus	
PART – A FIXED SET OF EXPERIMENTS	
1	Introduction to VLSI testing concepts and DFT tools. Demonstration of simulation environment using open source /free ware / Tessent/ Modus / any other commercial tools.
2	Modeling stuck-at faults in simple combinational circuits (AND/OR networks).
3	Fault simulation and fault coverage calculation for combinational circuits.
4	Implementation of path sensitization method for generating test vectors.
5	Test generation using D-Algorithm (ATPG concept demonstration).
6	Test generation using Boolean difference method.
7	Parallel and deductive fault simulation techniques.
8	Testing of sequential circuits using time-frame expansion concept.
9	Sequential circuit testing – state justification and propagation analysis.
10	Implementation of scan chain architecture in a simple digital circuit. Demonstrate the scan working within open source /free ware / Tessent/Modus/ any other commercial tools.
PART: B - TYPICAL OPEN-ENDED EXPERIMENTS	
Open-ended experiments are a type of laboratory activity where the outcome is not predetermined, and students are given the freedom to explore, design, and conduct the experiment based on the problem statements as per the concepts defined by the course coordinator. It encourages creativity, critical thinking, and inquiry-based learning.	
1	Study and demonstration of boundary scan (IEEE 1149.1 – JTAG) architecture. Insert Boundary scan and TAP for a design netlist using Boundary Scan and verify mandatory instructions over simulations. 2.. 3.
2	Explain any type of March algorithm. Implement the March algorithm by inserting BIST in a design netlist using Memory BIST Tool. Generate Memory BIST patterns and simulate.
3	Execute scan chain implementation for an 8-bit counter design in netlist. Execute ATPG on the scan-inserted design and verify the ATPG patterns in Questa. Estimate coverage for Stuck and delay test.

Teaching & Learning Process (Innovative Delivery Methods):	
1	Active Learning Techniques
2	Problem-Based Learning (PBL)
3	Team-Based Learning (TBL)
4	Hands-On Experiments and Simulations

TEXT BOOKS:	
1	Digital Systems Testing and Testable Design — Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman
2	Digital System Test and Testable Design — Zainalabedin Navabi
3	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits — Michael L. Bushnell and Vishwani D. Agrawal

e-LEARNING RESOURCES:	
1	https://www.youtube.com/watch?v=MgCFUO2BrkQ 2.
2	Videos and Lecture Notes: http://www.nptel.ac.in
3	https://www.youtube.com/watch?v=nX0XCD0ggHs&list=PLvd8d SyI7hjk_Ci0zpTqImAtpEjdK5JF

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each.
The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.
CIE: The CIE has two components – CIE - theory component and CIE – laboratory component.
Students have to score a minimum of 40% Marks in the total of CIE - theory and CIE – laboratory components put together, provided students have to score a minimum of 40% marks in CIE laboratory component alone to qualify to take SEE.
Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.
****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)		Max. Marks	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Laboratory components	Rubrics for each experiment are added, then taken average	**30**	**20**
	Lab CIE	**20**	
	TOTAL	**50**	**20**

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Demonstrate the use of VLSI testing and DFT tools to model faults, perform fault simulation, and evaluate fault coverage in combinational circuits.
CO2	Generate test vectors for combinational circuits using path sensitization, D-Algorithm, and Boolean difference methods
CO3	Analyze the testability of sequential circuits using time-frame expansion, state justification, state propagation, and scan-chain architectures.
CO4	Design and implement Design for Testability (DFT) techniques, including full scan design, boundary scan (JTAG), Built-In Self-Test (BIST) using LFSR and MISR, and basic memory testing concepts.

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	1	3	3	–	–	1	1	1	2			
CO2	3	3	2	3	3	–	–	–	1	1	–			
CO3	3	3	2	3	3	–	–	–	1	1	–			
CO4	3	3	3	3	3	–	1	1	2	2	1			

Mapping of CO's with Knowledge and Attitude Profile (WK)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	3	2	3	3	2	1	1	0	2
CO2	0	3	3	3	3	2	2	2	1
CO3	0	3	3	3	3	1	2	3	1
CO4	0	3	3	3	3	1	2	3	2
CO5	0	3	3	3	3	2	3	2	3

Mapping of CO's with Sustainable Development Goals (SDG)

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1	0	0	0	3	0	0	0	2	3	0	0	2	0	0	0	0	0
CO2	0	0	0	3	0	0	0	3	3	0	0	2	0	0	0	0	0
CO3	0	0	0	3	0	0	0	3	3	0	0	2	0	0	0	0	0
CO4	0	0	0	3	0	0	0	3	3	0	0	3	0	0	0	0	0

SPICE Programming for Electronic Circuits			
Course Code	**1BVLL406B**	Scheme	2025
Type of Course	Ability Enhancement Course (Laboratory)	Semester	IV
Teaching Hours/Week (L:T:P)	0:0:1	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL/TW	0:0:28:02	SEE Marks	50
Credits	01	Total Marks	100
Type of Examination	Practical	Exam Hours	03

Course Outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the fundamentals of the SPICE simulation environment and circuit modeling.
2. Develop and execute SPICE netlists for basic electronic circuits.
3. Perform DC, AC, and transient analyses using SPICE simulation.
4. Analyze the behavior and performance of analog and digital electronic circuits through simulation.
5. Simulate and characterize MOSFET and CMOS-based circuits for VLSI applications.

SET OF EXPERIMENTS using

Simulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis **(SPICE)**

1. Familiarization with the LTspice/Ngspice environment and basic SPICE commands. Develop a SPICE netlist for a resistive network and perform DC sweep analysis and measure current through all elements voltage across all nodes.
2. Develop a SPICE netlist for resistor networks and verify circuit behavior through simulation. Validate Ohm's Law using simulation results.
3. Develop a SPICE netlists and analyze the transient response of an RC low pass and RC high pass circuits.
4. Develop a SPICE netlists and analyze the transient response of an RL low pass and RL high pass circuits.
5. Develop a SPICE netlists and perform AC analysis of an RL low pass and RL high pass circuits.
6. Develop a SPICE netlists and perform AC analysis of an RC low-pass filter with and without parasitic inductance.
7. Develop a SPICE netlist and perform AC analysis of an RC high-pass filter with and without parasitic inductance.
8. Develop a SPICE netlists and simulate a diode rectifier circuit and clipping circuits.
9. Develop a SPICE netlist and perform AC analysis of a RLC circuit.
10. Develop a SPICE netlist and study the frequency response and Bode plot of a circuit. Correlate the observed peak impedance characteristics with transient analysis results.

MOSFET-Based Experiments

11. Develop a SPICE netlist and simulate the drain characteristics (ID–VDS) of a MOSFET. Analyze the effect of gate voltage on device operation.
12. Develop a SPICE netlist and simulate the transfer characteristics (ID–VGS) of a MOSFET. Determine key device parameters from the simulation results.
13. Develop a SPICE netlist and simulate a common-source MOSFET amplifier. Analyze voltage gain and frequency response.
14. Develop a SPICE netlist and simulate a MOSFET inverter. Analyze its switching characteristics and transient response.
15. Develop a SPICE netlist and simulate a CMOS inverter. Plot and analyze its DC transfer characteristics (VTC).
16. Develop a SPICE netlist for a buffer by creating inverter sub-circuit.

Mini Project (Recommended)

Design, write SPICE netlist, simulate and analyze one of the following circuits:

- Implement 2-stage CMOS domino logic and measure the delay.
- Implement NMOS current mirror circuit for 1:1 and 1:2 scaling.
- Implement NMOS Opamp with unity gain (Voltage Follower) and gain-2.
- Implement CMOS high to low level shifter cell.
- Impedance profile of a simple power delivery network (frequency response)

Suggested Learning Resources: (Textbook/ Reference Book/ Manuals):

Textbooks:

1. SPICE for Circuits and Electronics Using PSpice, M. H. Rashid, SPICE for Circuits and Electronics Using PSpice. Upper Saddle River, NJ, USA: Pearson Education, 2004.
2. The SPICE Book, A. Vladimirescu, The SPICE Book. New York, NY, USA: John Wiley & Sons, 1994.

Reference books / Manuals:

1. **Purdue University, SPICE user manual: https://www.physics.purdue.edu/~jones105/phys536_Spring2008/Spice3F4_Manual.pdf**
2. **HSPICE® User Guide: Simulation and Analysis - https://cseweb.ucsd.edu/classes/wi10/cse241a/assign/hspice_sa.pdf**

Web links and Video Lectures (e-Resources):

- **IITR lecture – "Introduction to spice":**
  - **https://www.youtube.com/watch?v=KfBtduxuxCw**
- **IITR lecture – "SPICE Simulation":**
  - **https://www.youtube.com/watch?v=Z6Cfbs0ODpg**
  - **https://www.youtube.com/watch?v=tI5GLv1ipKw**

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1) **Hands-on Simulation-Based Learning:**

   Conduct guided laboratory sessions where students develop SPICE netlists, perform simulations, and analyze circuit behavior using LTspice, Ngspice, or equivalent tools. Encourage students to compare simulation results with theoretical calculations and expected circuit responses.

2) **Mini-Project and Problem-Based Learning (PBL):**

   Assign real-world circuit design problems and VLSI-oriented mini-projects involving MOSFETs, CMOS circuits, current mirrors, level shifters, and domino logic. Students shall design, simulate, validate, and present their solutions, fostering self-learning, critical thinking, and industry-relevant design skills.

Recommended Tools:

Free circuit simulation tools such as **LTspice and Ngspice**, or commercial VLSI ECAD software packages such as Siemens, Cadence, Altium etc..

Course Title	Design for Test						
Course Code	1BVL409						
Course Category	PCC **(Professional Core Course)**						
Teaching - Learning Scheme & Credit	**L**	**T**	**P**	**S**	**Total**	**Total Teaching Hours**	**Credit**
	3	**0**	**0**	**3**	**3**	**42+0+0+48=90**	**4**
CIE Marks: 50	**SEE Marks: 50**		**Total Max. Marks: 100**			**Duration of SEE: 03 Hrs**	

Course Learning Objectives:	
CLO1	Understand the importance of testing in VLSI circuits.
CLO2	Analyze fault models and test generation techniques.
CLO3	Apply Design for Testability (DFT) techniques such as scan design and Built-In Self-Test (BIST).
CLO4	Understand modern testing challenges in deep-submicron VLSI circuits.
CLO5	Analyze and evaluate the testability of digital VLSI circuits by applying fault modeling, ATPG, fault simulation, and scan-based Design for Testability (DFT) techniques

SYLLABUS	**No. of Hours**	**BTLs**
UNIT 1	**8**	**L1-L4**
INTRODUCTION: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing, Electrical Parametric Testing VLSI TESTING PROCESS ANDTEST EQUIPMENT: How to Test Chips, Types of Testing, Automatic Test Equipment. FAULT MODELING: Defects, Errors, and Faults, Functional Versus Structural Testing, Levels of Fault Models, A Glossary of Fault Models, Single Stuck-at Fault. Textbook 1: Chapter 1, Chapter 2and Chapter 4		
SELF-STUDY COMPONENTS: Digital and Analog VLSI Testing,		
UNIT 2	**8**	**L1-L4**
LOGIC AND FAULT SIMULATION: Simulation for Design Verification, Simulation for Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-Value Simulation, Algorithms for Fault Simulation, Statistical Methods for Fault Simulation TESTABILITY MEASURES: SCOAP Controllability and Observability, High-Level Testability Measures Textbook 1: Chapter 5 and Chapter 6		
SELF-STUDY COMPONENTS:		
UNIT 3	**8**	**L1-L4**
COMBINATIONAL CIRCUIT TEST GENERATION: Algorithms and Representations, Redundancy Identification (RID), Testing as a Global Problem, Significant Combinational ATPG Algorithms, Test Generation Systems, Test Compaction SEQUENTIAL CIRCUIT TEST GENERATION: ATPG for Single-Clock Synchronous Circuits, Time-Frame Expansion Method, Simulation-Based Sequential Circuit ATPG Textbook 1: Chapter 7 and Chapter 8		
SELF-STUDY COMPONENTS:		
UNIT 4	**9**	**L1-L4**
MEMORY TEST: Memory Density and Defect Trends, Faults, Memory Test Levels, March Test Notation, Fault Modeling, Memory Testing DIGITAL DFT AND SCAN DESIGN: Ad-Hoc DFT Methods, Partial-Scan Design, Variations of Scan Textbook 1: Chapter 9 and Chapter 14		
SELF-STUDY COMPONENTS:		
UNIT 5	**9**	**L1-L4**
Built-In Self-Test (BIST) and Memory Testing: Built-In Self-Test architecture, Test pattern generation using LFSR, Signature analysis and MISR, Logic BIST, Memory testing and memory fault models, March tests for memory testing, Introduction to low-power testing and modern DFT trends Textbook 1: Chapter 15		
SELF-STUDY COMPONENTS:		

TEXT BOOKS:	
1	M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed SignalVLSI Circuits. Boston, MA, USA: Kluwer Academic Publishers, 2002.

REFERENCE BOOKS:	
1	M. Abramovici, M. A. Breuer, and A. D. Friedman, Digital Systems Testing and Testable Design. New York, NY, USA: Computer Science Press, 1990.
2	Z. Navabi, Digital System Test and Testable Design: Using HDL Models and Architectures. Boston, MA, USA: Kluwer Academic Publishers, 1998.
3	L.-T. Wang, C.-W. Wu, and X. Wen, VLSI Test Principles and Architectures: Design for Testability. Burlington, MA, USA: Morgan Kaufmann, 2006.
e-LEARNING RESOURCES:	
1	Web links and Video Lectures (e-Resources): https://nptel.ac.in/courses/106103116
2	Videos and Lecture Notes: http://www.nptel.ac.in

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.

CIE: The CIE has three components – CIE - theory component, assignment and group activity. Students have to score a minimum of 40% Marks in the total of CIE - theory, assignment and group activity components put together to take SEE.

SEE: Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.

****Self-Study Component should be not included for SEE & CIE.**

CONTINUOUS INTERNAL EVALUATION (CIE)		Max. Marks	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Theory	**Weightage of CIE1 and CIE2 Tests or CIE3**	**50**	**20**
	TOTAL	**50**	**20**

QUESTION PAPER PATTERN (SEE)										
Q. No.	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**	**Q9**	**Q10**
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Explain the fundamentals of VLSI testing, fault modeling, testing methodologies, automatic test equipment (ATE), and the impact of technology scaling on testability.
CO2	Analyze logic simulation, fault simulation techniques, and testability measures to evaluate the test quality of combinational and sequential VLSI circuits.
CO3	Apply Automatic Test Pattern Generation (ATPG) algorithms and test compaction techniques for combinational and sequential digital circuits.
CO4	Analyze memory fault models, memory testing techniques, scan-based Design for Testability (DFT), and scan architectures for digital integrated circuits.
CO5	Evaluate Built-In Self-Test (BIST) architectures, LFSR-based test pattern generation, MISR-based signature analysis, and modern low-power testing techniques for reliable VLSI systems.

Mapping of CO's, PO's with PSO's

Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0

CO	PO 1	PO 2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	0	0	0	2	1	1	1	0			
CO2	3	3	2	0	0	0	2	1	1	1	0			
CO3	3	3	3	0	0	0	2	1	1	1	0			
CO4	3	3	3	0	0	0	2	1	1	1	0			
CO5	3	3	3	0	0	0	2	1	1	1	0			

Mapping of CO's with Knowledge and Attitude Profile (WK) **Strength of correlation:** Strongly related-3, Moderately related-2, Weakly related-1, Not related-0									
CO	**WK1**	**WK2**	**WK3**	**WK4**	**WK5**	**WK6**	**WK7**	**WK8**	**WK9**
CO1	0	3	2	2	2	0	2	2	0
CO2	0	3	3	3	1	0	1	3	0
CO3	0	3	2	3	3	0	3	2	0
CO4	0	3	3	2	2	0	2	3	0
CO5	0	2	2	3	3	0	1	2	0

Mapping of CO's with Sustainable Development Goals (SDG) **Strength of correlation:** Strongly related-3, Moderately related-2, Weakly related-1, Not related-0																	
CO/SDG	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**
CO1	0	0	0	3	0	0	0	2	3	0	0	1	0	0	0	0	0
CO2	0	0	0	3	0	0	0	2	3	0	0	2	0	0	0	0	0
CO3	0	0	0	3	0	0	0	3	3	0	0	2	0	0	0	0	0
CO4	0	0	0	3	0	0	0	3	3	0	0	3	0	0	0	0	0
CO5	0	0	0	3	0	0	0	3	3	0	0	3	0	0	0	0	0