Transistor Biasing

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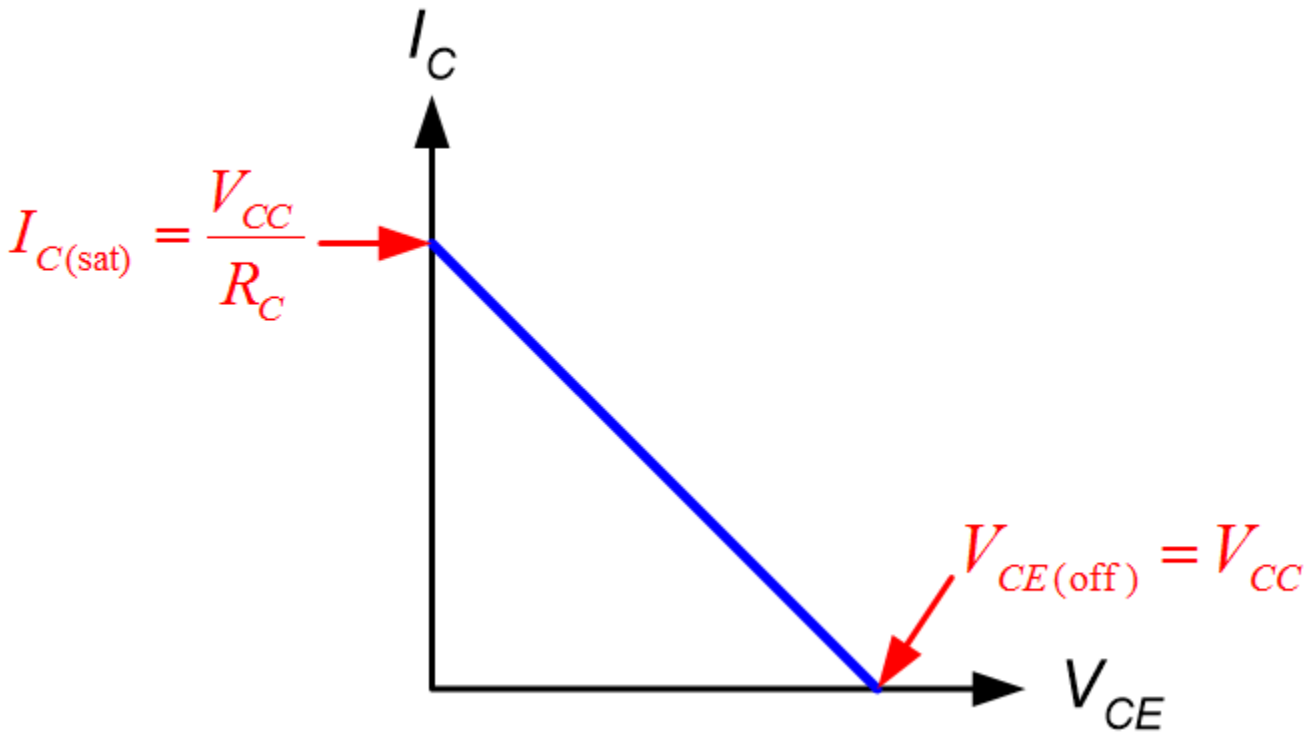
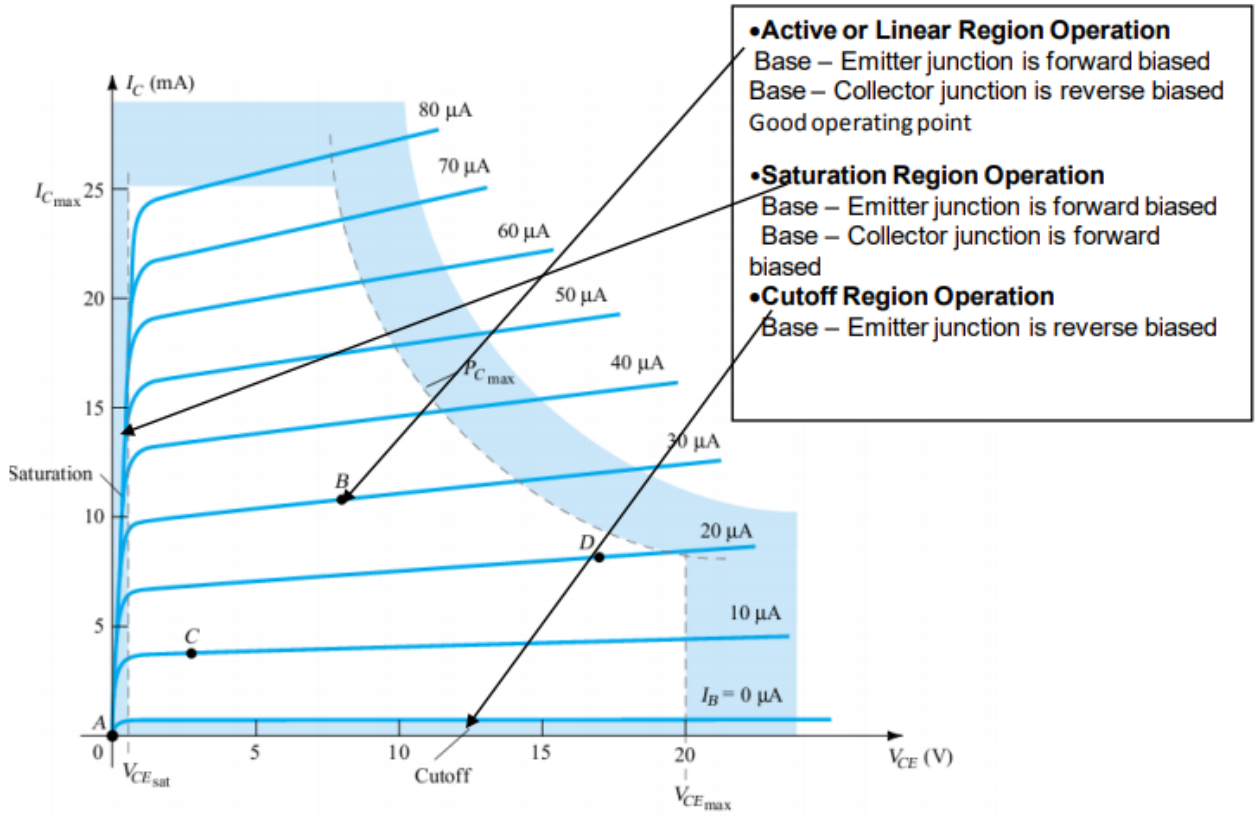
DC Load Line



Operating Point



Biasing

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. In fact, the amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal The analysis or design of any electronic amplifier therefore has two components:

- The dc portion and
- The ac portion

During the design stage, the choice of parameters for the required dc levels will affect the ac response.

Biasing: Application of dc voltages to establish a fixed level of current and voltage.

Purpose of the DC biasing circuit

- To turn the device “ON”
- To place it in operation in the region of its characteristic where the device operates most linearly .
- Proper biasing circuit which it operate in linear region and circuit have centered Q-point or midpoint biased
- Improper biasing cause Improper biasing cause
- Distortion in the output signal
- Produce limited or clipped at output signal

BIASING AND BIAS STABILITY

❖ Biasing refers to the establishment of suitable dc values of different currents and voltages of a transistor.

❖ Through proper biasing, a desired quiescent operating point of the transistor amplifier in the active region (linear region) of the characteristics is obtained.

❖ The selection of a proper quiescent point generally depends on the following factors:

(a) The amplitude of the signal to be handled by the amplifier and distortion level in signal

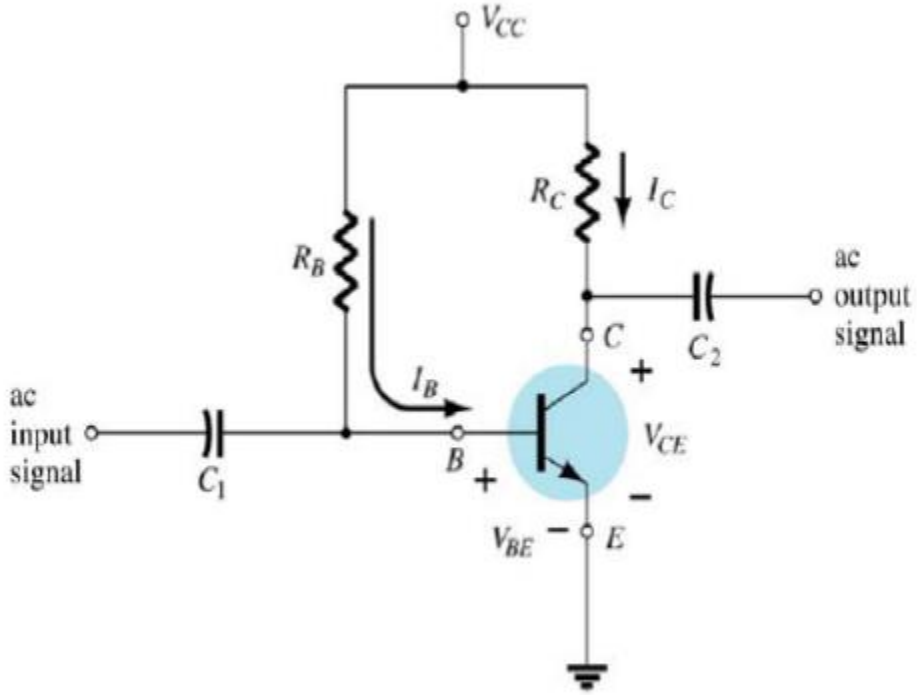
(b) The load to which the amplifier is to work for a corresponding supply voltage

❖ The operating point of a transistor amplifier shifts mainly with changes in temperature, since the transistor parameters — *β, I_{CO} and V_{BE} (where the symbols carry their usual meaning)—are functions of* temperature.

❖ **Circuit Configurations**

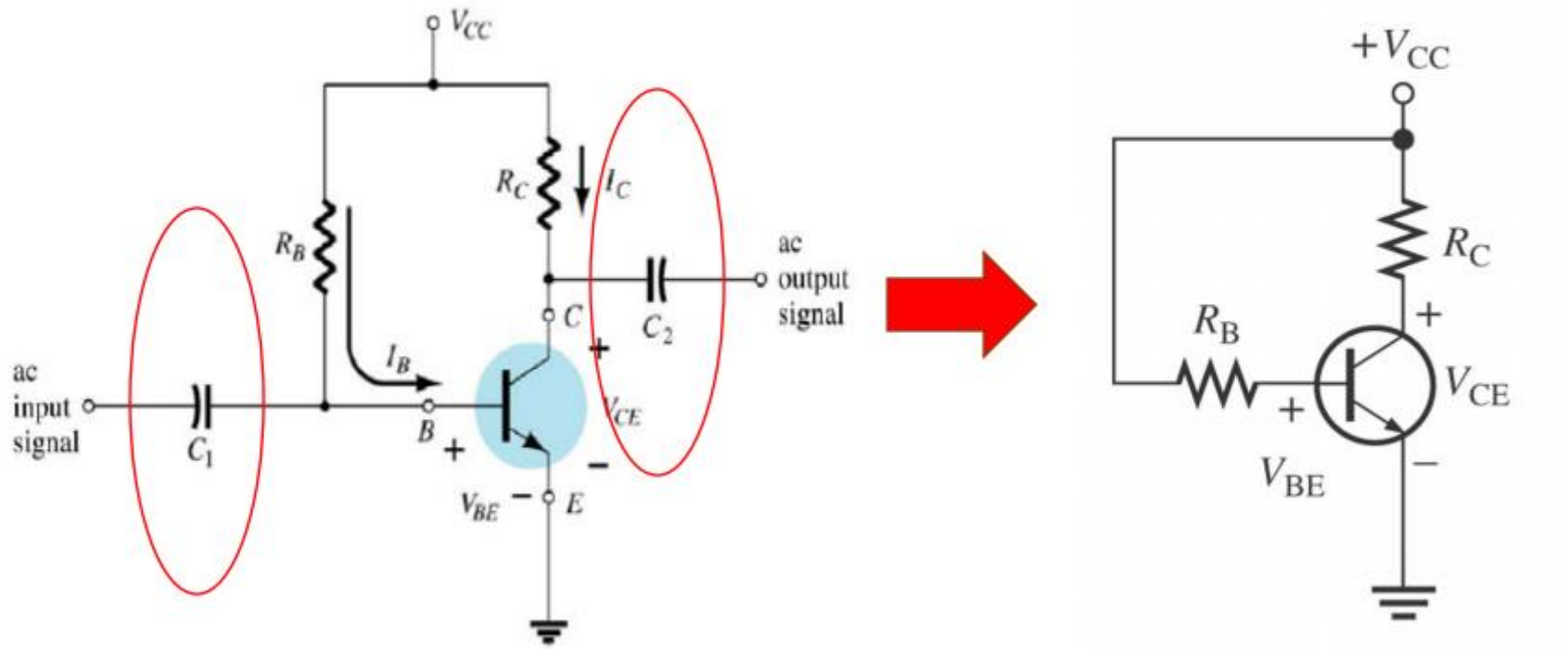
- **Fixed-bias circuit**
- **Fixed bias with emitter resistance**
- **Voltage-divider bias**
- **Voltage-feedback biasing**

Fixed Bias Circuit

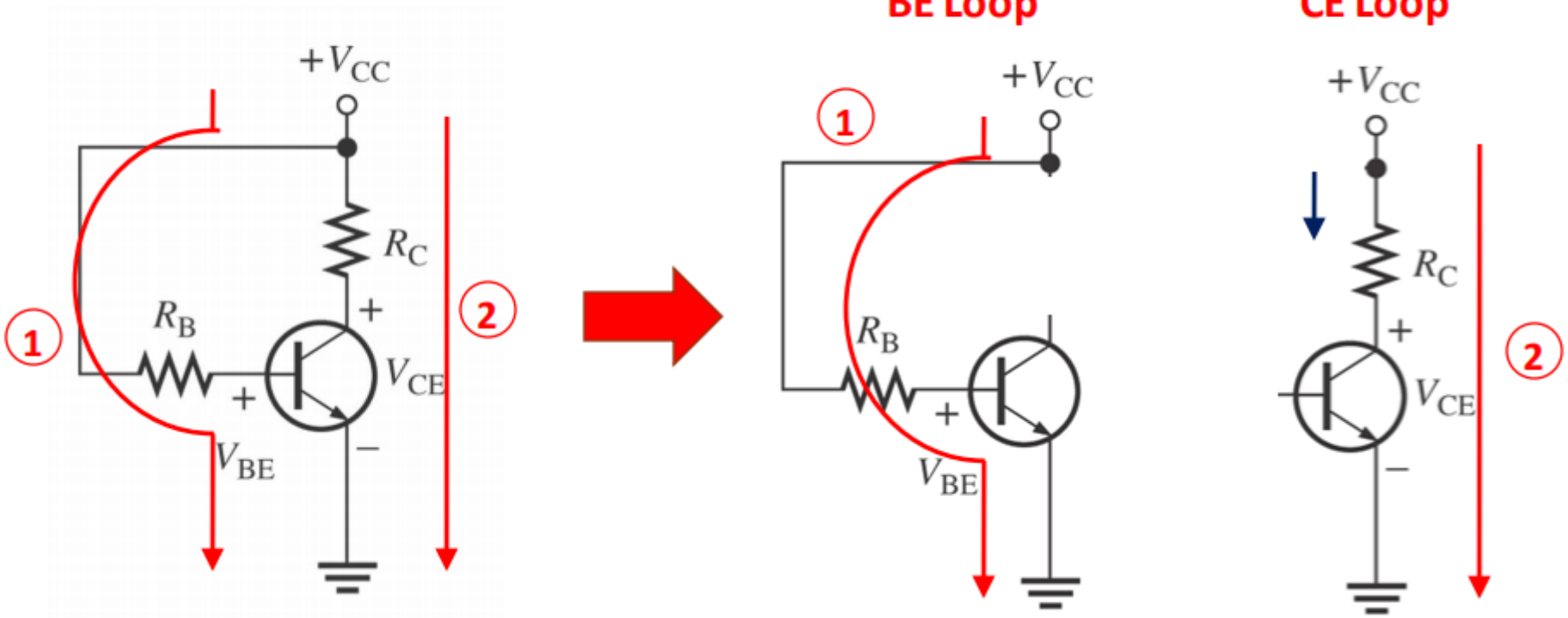


- This is common emitter (CE) configuration
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Locate 2 main loops which;
  - BE loop (input loop)
  - CE loop(output loop)

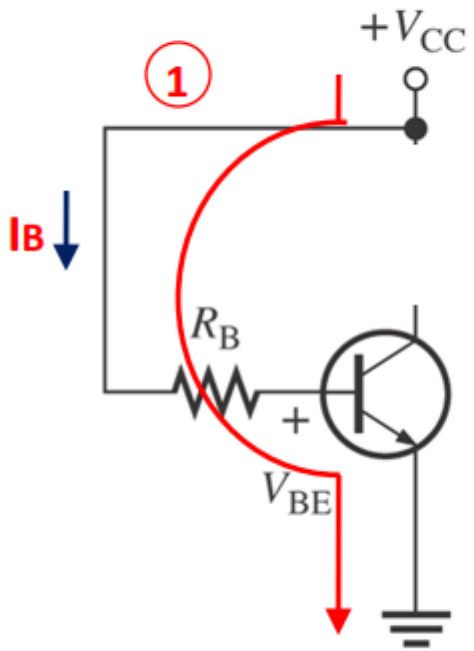
- 1st step: Locate capacitors and replace them with an open circuit



- 2nd step: Locate 2 main loops.



- BE Loop Analysis

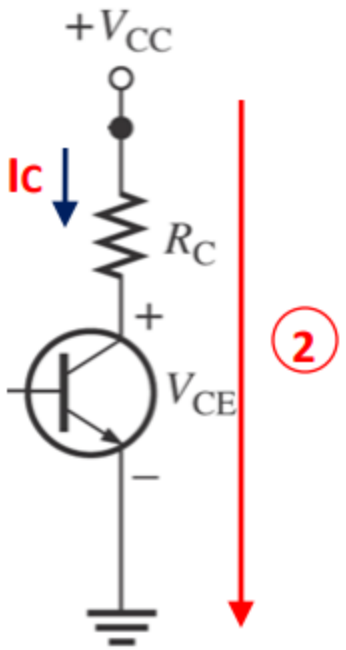


- From KVL;

$$-V_{CC} + I_B R_B + V_{BE} = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad (A)$$

- CE Loop Analysis



- From KVL;

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

$$\therefore V_{CE} = V_{CC} - I_C R_C$$

- As we known;

$$I_C = \beta I_B \quad (B)$$

- Substituting (A) with (B)

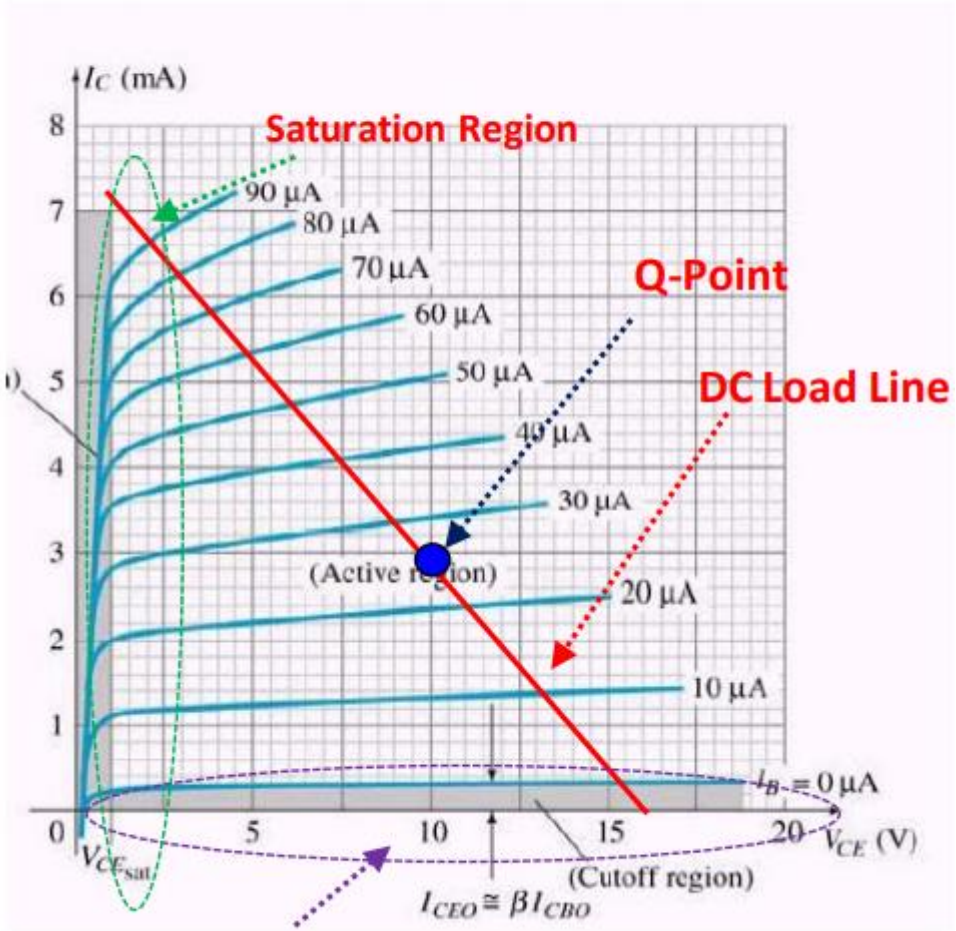
$$I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

Note that R_C does not affect the value of Ic

Load line analysis

A fixed bias circuit with given values of V_{CC}, R_C and R_B can be analyzed (means, determining the values of I_{BQ}, I_{CQ} and V_{CEQ}) using the concept of load line also.

Here the input loop KVL equation is not used for the purpose of analysis, instead, the output characteristics of the transistor used in the given circuit and output loop KVL equation are made use of.



- Plot load line equation

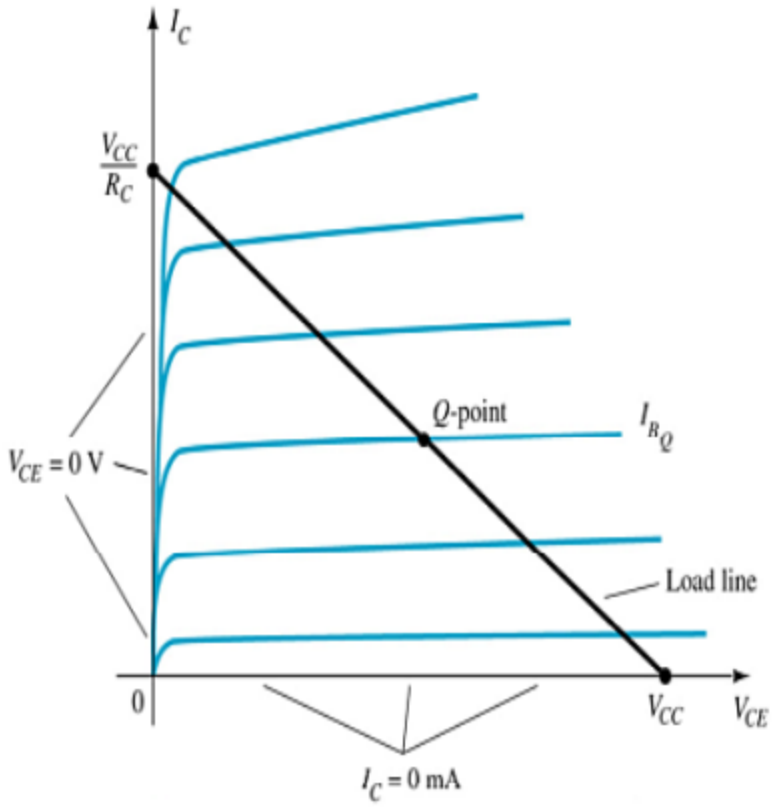
$$V_{CE} = V_{CC} - I_C R_C$$

- $I_{C(sat)}$ occurs when transistor operating in *saturation region*

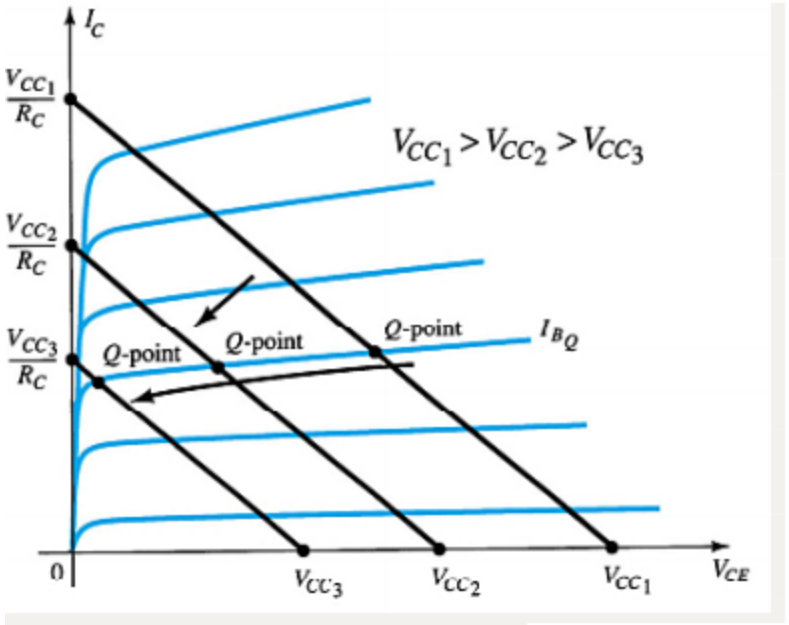
$$I_{C_{sat}} = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0}$$

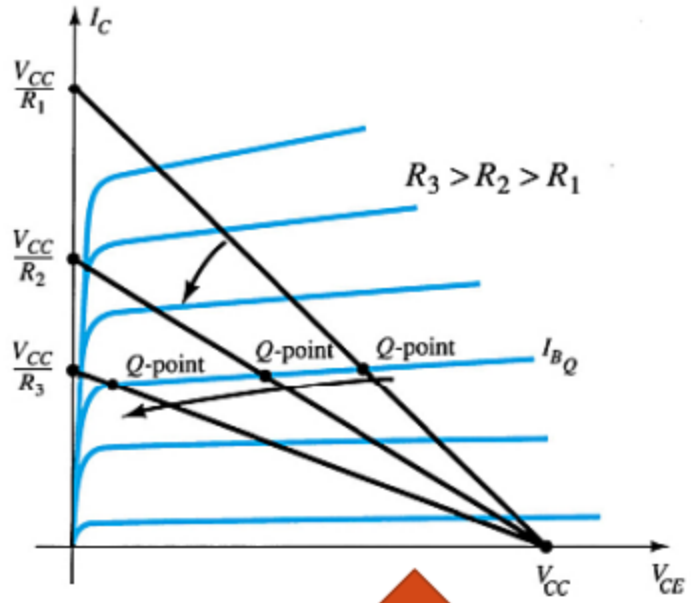
- $V_{CE(off)}$ occurs when transistor operating in *cut-off region*

$$V_{CE_{(off)}} = V_{CC} - I_C R_C\big|_{I_C=0}$$



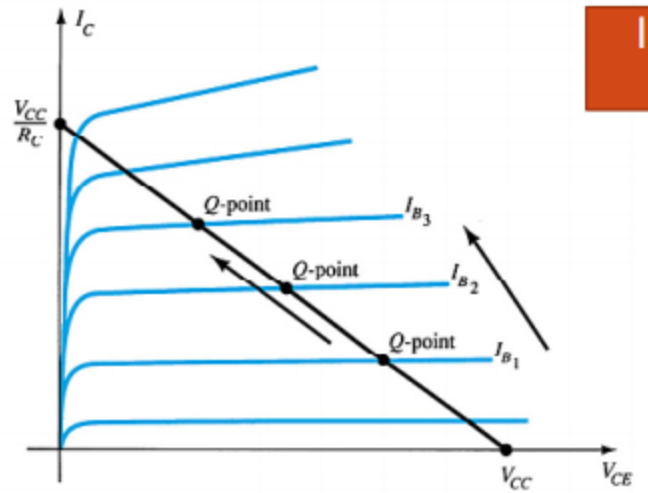
Circuit Values Affect the Q-Point





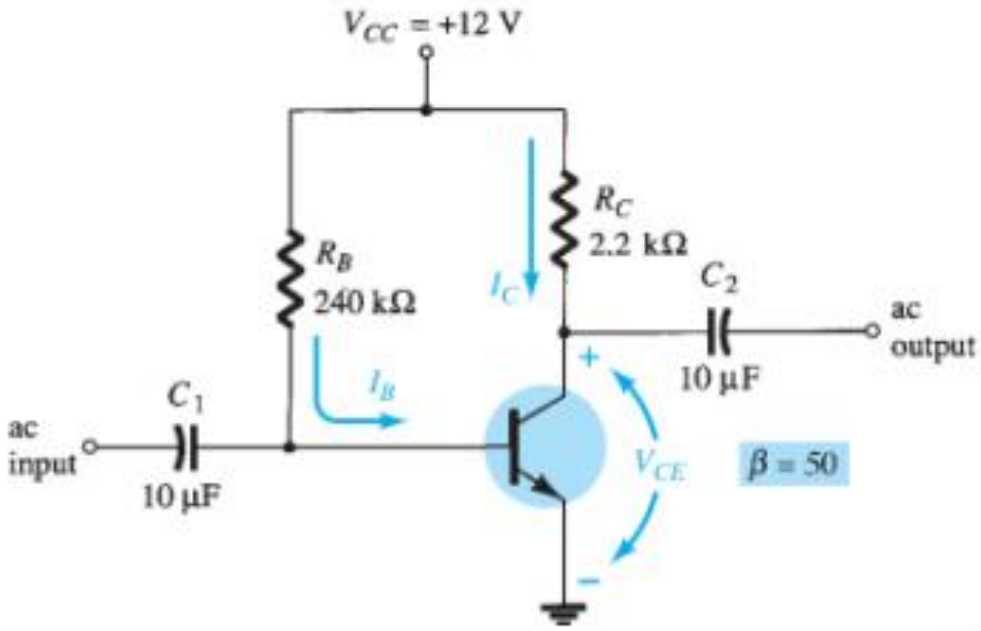
Increasing Rc

Decreasing Vcc



Varying Ib

Problem



Determine the following for the fixed-bias configuration

a. I_{B_Q} and I_{C_Q}.
b. V_{CE_Q}.
c. V_B and V_C.
d. V_{BC}.

solution

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\,\text{V} - 0.7\,\text{V}}{240\,\text{k}\Omega} = \mathbf{47.08\,\mu A}$$

$$I_{C_Q} = \beta I_{BQ} = (50)(47.08\,\mu\text{A}) = \mathbf{2.35\,mA}$$

$$\begin{aligned} V_{CE_Q} &= V_{CC} - I_C R_C \\ &= 12\,\text{V} - (2.35\,\text{mA})(2.2\,\text{k}\Omega) \\ &= \mathbf{6.83\,V} \end{aligned}$$

$$V_B = V_{BE} = \mathbf{0.7\,V}$$

$$V_C = V_{CE} = \mathbf{6.83\,V}$$

$$\begin{aligned} V_{BC} &= V_B - V_C = 0.7\,\text{V} - 6.83\,\text{V} \\ &= \mathbf{-6.13\,V} \end{aligned}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Fixed Bias Circuit

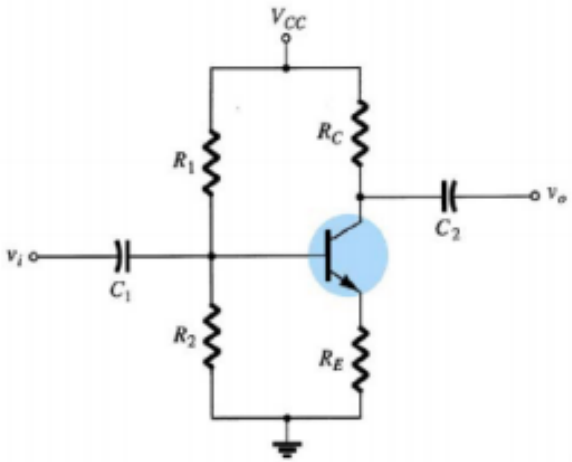
DISADVANTAGE

- Unstable – because it is too dependent on β and produce width change of Q-point
- For improved bias stability , add emitter resistor to dc bias.

VOLTAGE DIVIDER BIAS CIRCUIT

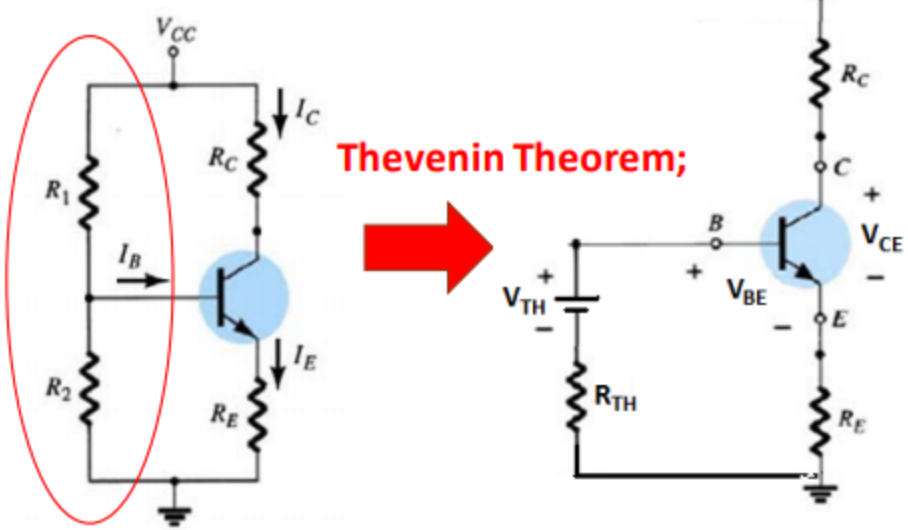
- Provides good Q-point stability with a single polarity supply voltage
- This is the biasing circuit wherein, ICQ and VCEQ are almost independent of beta.
- The level of IBQ will change with beta so as to maintain the values of ICQ and VCEQ almost same, thus maintaining the stability of Q point.

- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Simplified circuit using Thevenin Theorem
- 3rd step: Locate 2 main loops which;
  - BE loop
  - CE loop



VOLTAGE DIVIDER BIAS CIRCUIT

- 2nd step: : Simplified circuit using **Thevenin Theorem**



Simplified Circuit

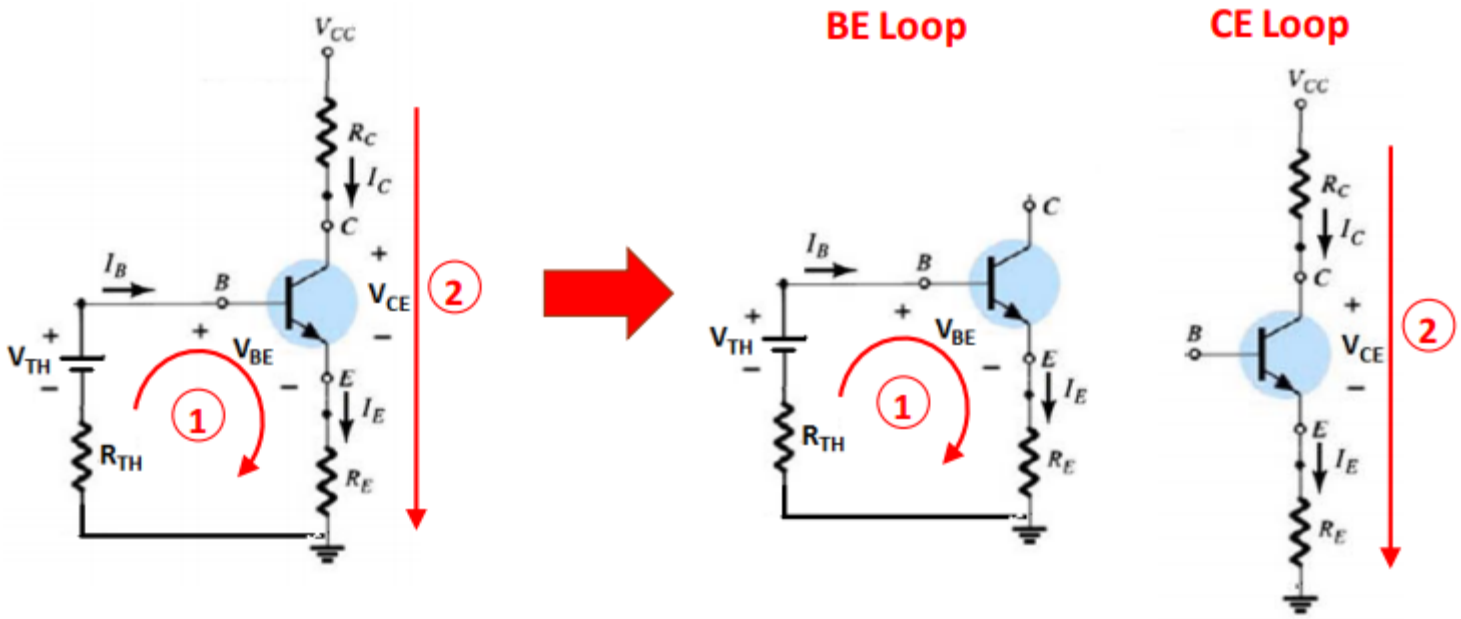
From Thevenin Theorem;

$$R_{TH} = R_1 // R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

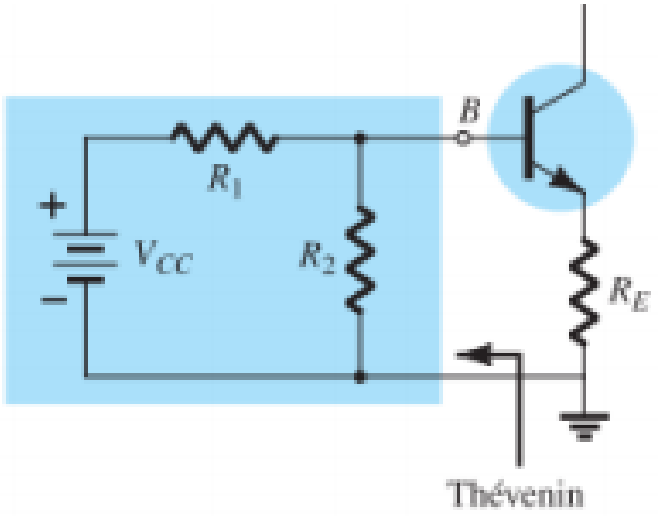
$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

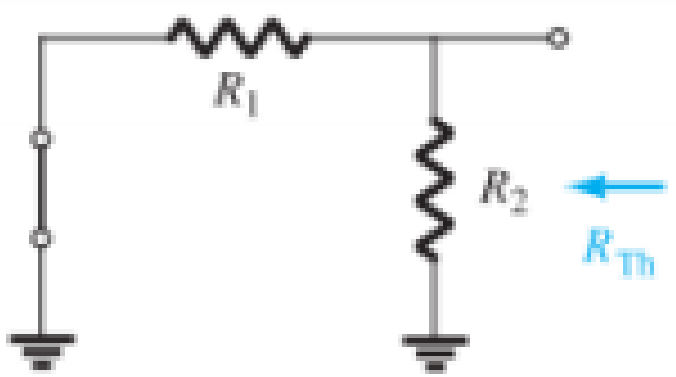
VOLTAGE DIVIDER BIAS CIRCUIT

- 2nd step: Locate 2 main loops.



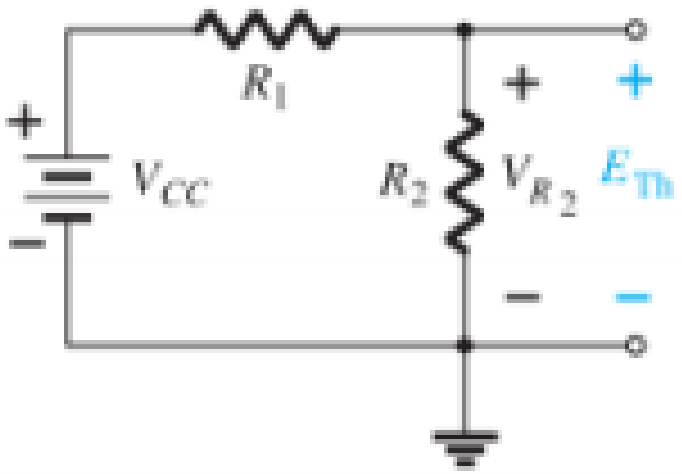
Thevenin Equivalent Resistance





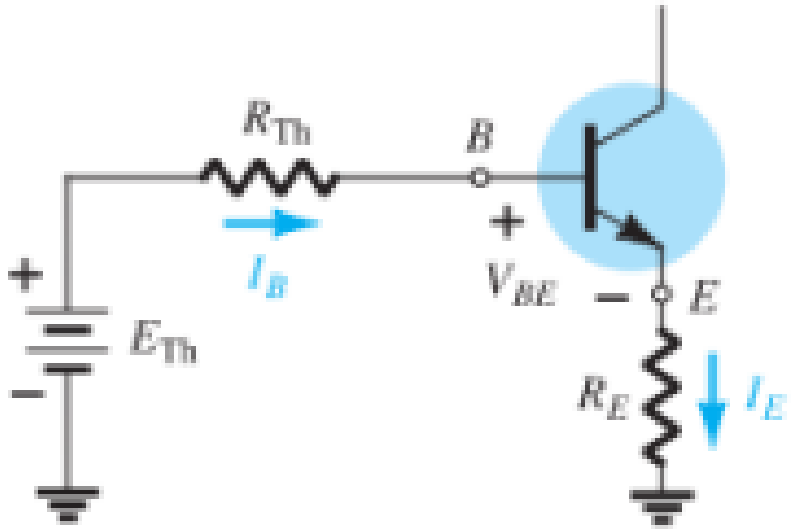
$$R_{Th} = R_1 \| R_2$$

Thevenin Equivalent Voltage



$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Base Emitter Loop



- From KVL;

$$-V_{TH} + I_B R_{TH} + V_{BE} + I_E R_E = 0$$

Recall; $I_E = (\beta + 1) I_B$

Substitute for I_E

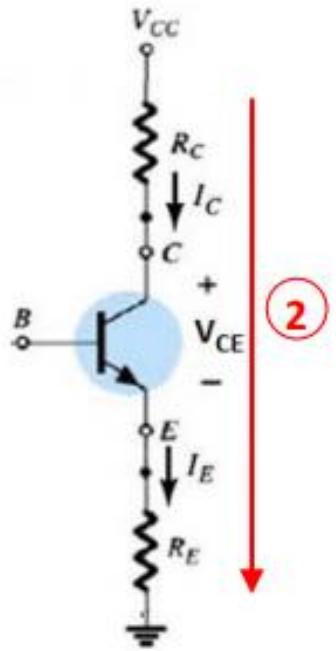
$$-V_{TH} + I_B R_{TH} + V_{BE} + (\beta + 1) I_B R_E = 0$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

VOLTAGE DIVIDER BIAS CIRCUIT

- CE Loop Analysis



- From KVL;

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

- Assume;

$$I_E \approx I_C$$

- Therefore;

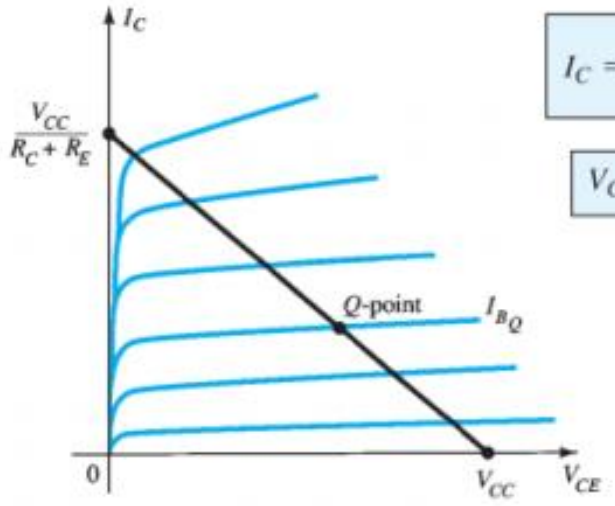
$$\therefore V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Transistor Analysis

- Transistor Saturation

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E}$$

- Load Line Analysis

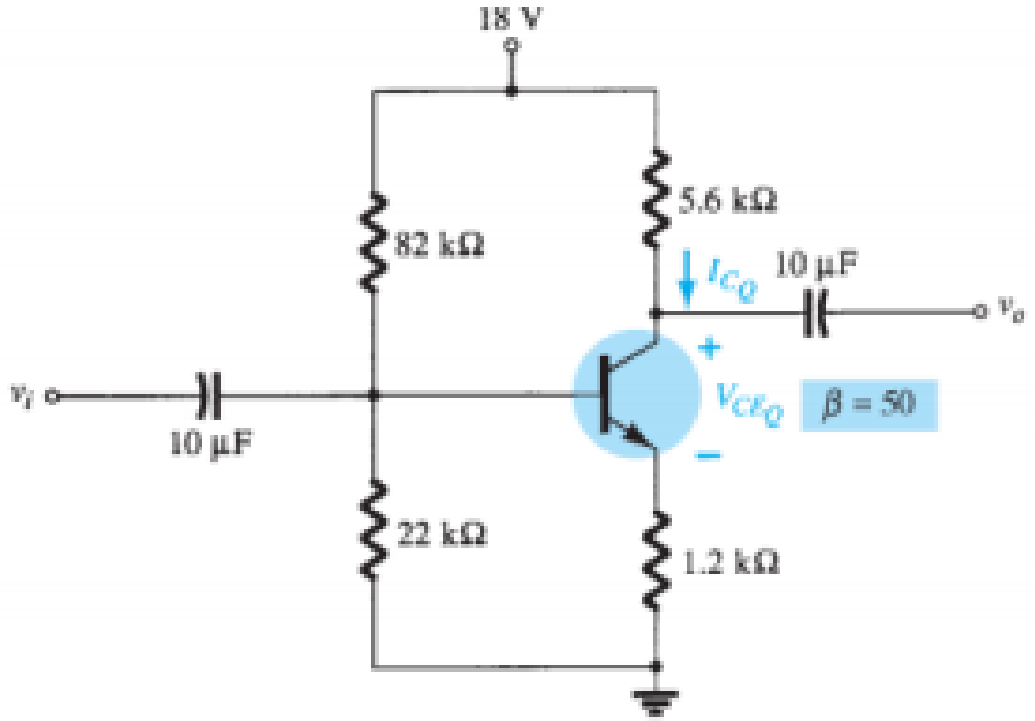


$$I_C = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE}=0\text{ V}}$$

$$V_{CE} = V_{CC}|_{I_C=0\text{ mA}}$$

Example

- Determine the ICQ and VCEQ for the voltage divider network shown below



Solution

$$R_{Th} = R_1 \| R_2 = 82\,k\Omega \| 22\,k\Omega = 17.35\,k\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22\,k\Omega(18\,V)}{82\,k\Omega + 22\,k\Omega} = 3.81\,V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{3.81\,V - 0.7\,V}{17.35\,k\Omega + (51)(1.2\,k\Omega)} = \frac{3.11\,V}{78.55\,k\Omega} = 39.6\,\mu A$$

$$I_{C_Q} = \beta I_B = (50)(39.6\,\mu A) = \mathbf{1.98\,mA}$$

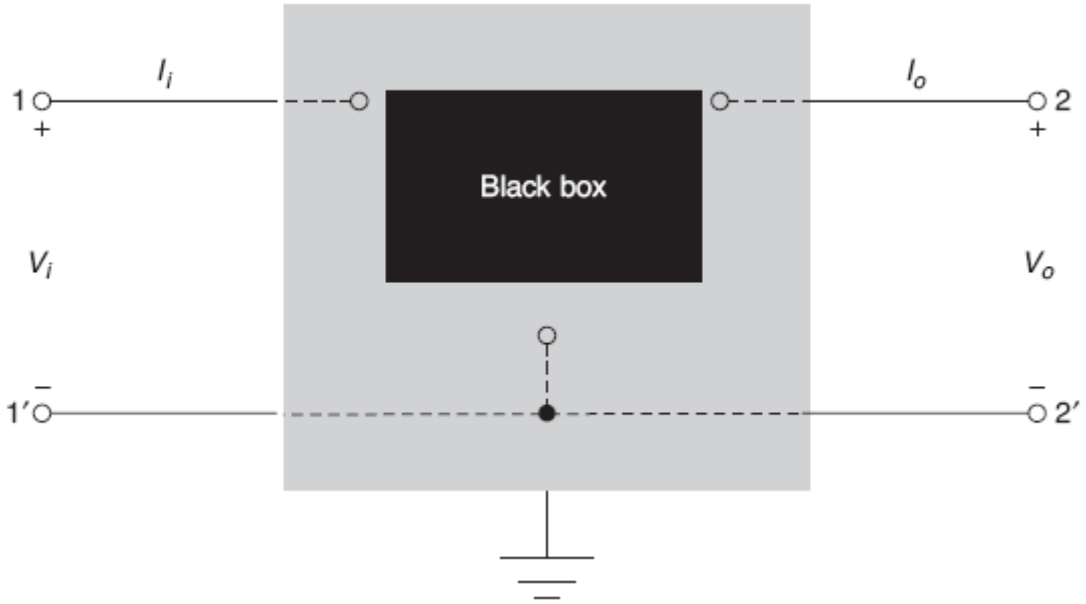
$$\begin{aligned} V_{CE_Q} &= V_{CC} - I_C(R_C + R_E) \\ &= 18\,V - (1.98\,mA)(5.6\,k\Omega + 1.2\,k\Omega) \\ &= \mathbf{4.54\,V} \end{aligned}$$

SMALL-SIGNAL LOW-FREQUENCY OPERATION OF TRANSISTORS

Hybrid Parameters and Two-Port Network

- For the hybrid equivalent model to be described, the parameters are defined at an operating point that may or may not give an actual picture of the operating condition of the amplifier. The quantities h_{ie} , h_{re} , h_{fe} *and* h_{oe} *are called the hybrid parameters and are the components of a small-signal equivalent circuit.* The description of the hybrid equivalent model begins with the general two-port system.

Two-port system representation (Black model realisation)



$$V_i = h_{11}I_i + h_{12}V_o$$

$$I_o = h_{21}I_i + h_{22}V_o$$

(i) $h_{11} \rightarrow$ input impedance $\rightarrow h_i$

(ii) $h_{12} \rightarrow$ reverse transfer voltage ratio $\rightarrow h_r$

(iii) $h_{21} \rightarrow$ forward transfer current gain $\rightarrow h_f$

(iv) $h_{22} \rightarrow$ output admittance $\rightarrow h_o$

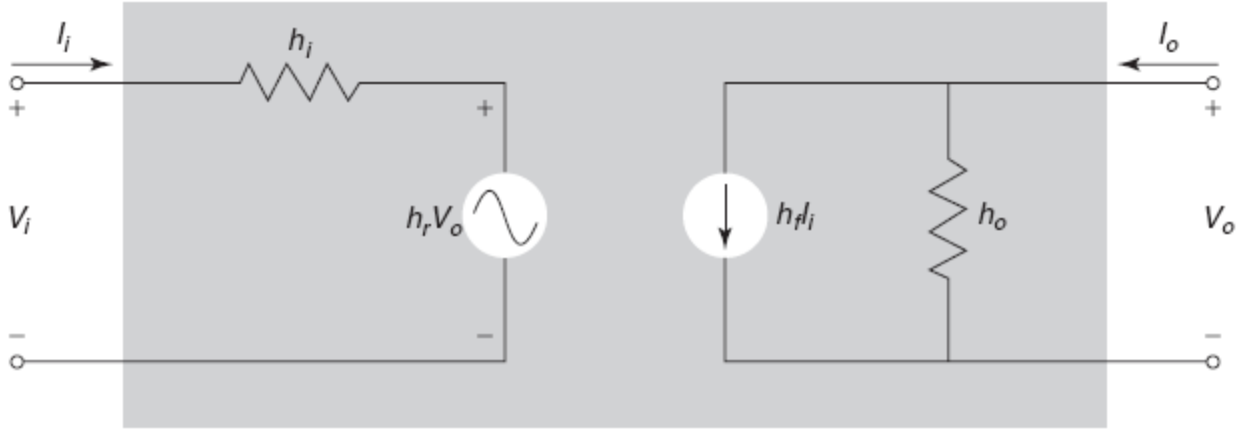
EQUIVALENT CIRCUITS THROUGH HYBRID PARAMETERS AS A TWO-PORT NETWORK

For the transistor, even though it has three basic configurations, they are all four-terminal configurations, and thus, the resulting equivalent circuit will have the same format. The *h-parameter will* however change with each configuration. To distinguish which parameter has been used or which is available, a second subscript has been added to the *h-parameter notation.*

(i) For the common-base configuration: the lower case letter b

(ii) For the common-emitter configuration: the lower case letter e

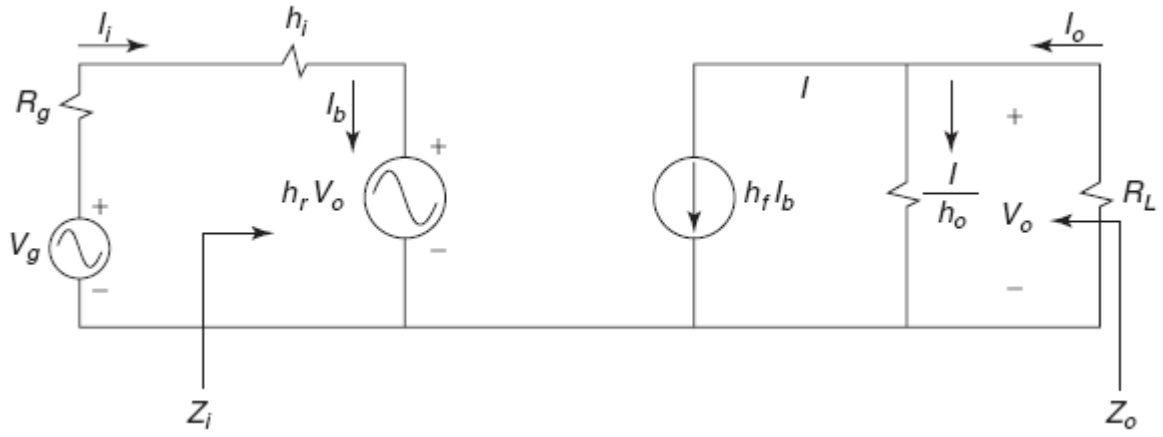
(iii) For the common-collector configuration: the lower case letter c



Complete hybrid equivalent model

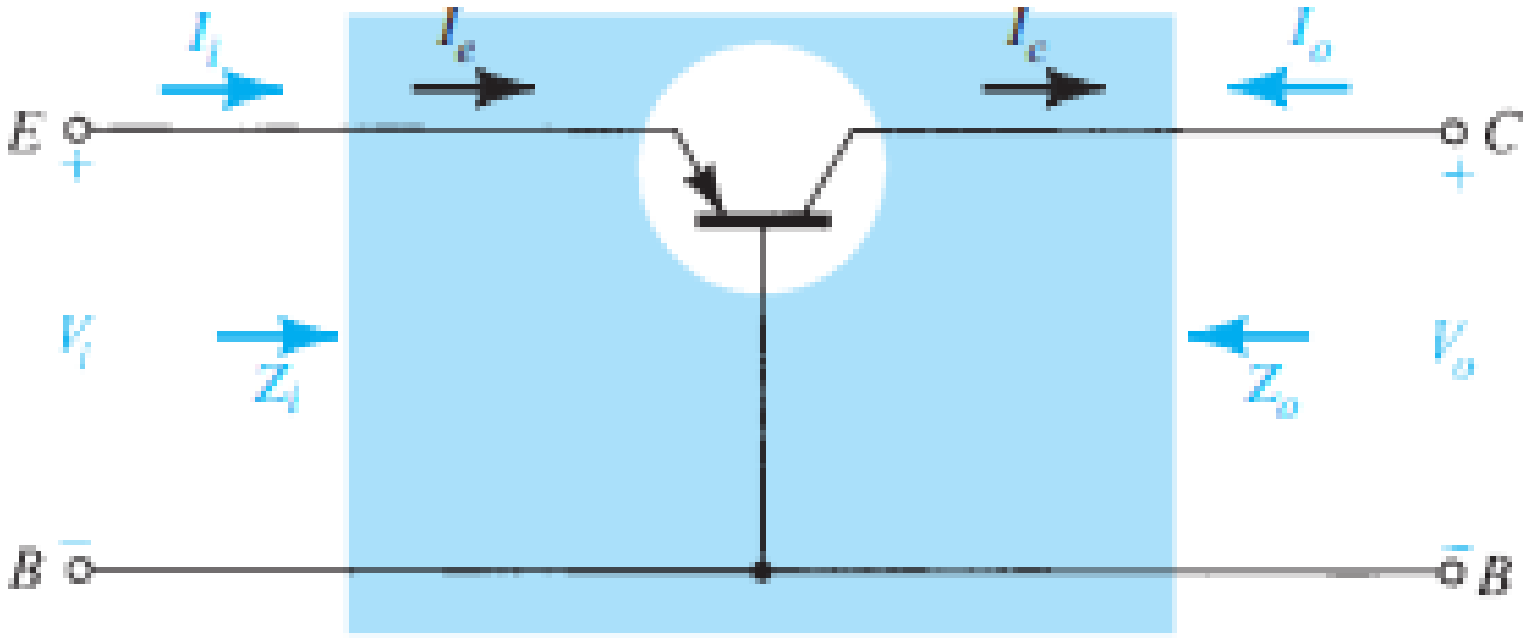
EXPRESSIONS OF CURRENT GAIN, INPUT RESISTANCE, VOLTAGE GAIN AND OUTPUT RESISTANCE

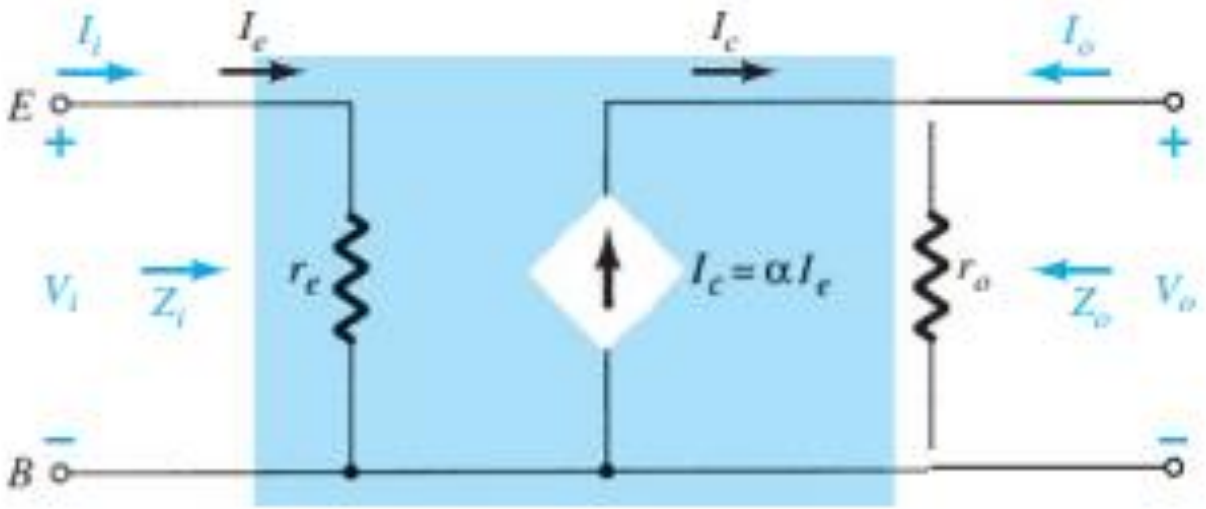
The *h-parameter equivalent circuit of a transistor amplifier having a voltage source* V_g , with its input resistance R_g *connected to the input terminals and a load resistance* R_L *connected to the output* terminals.



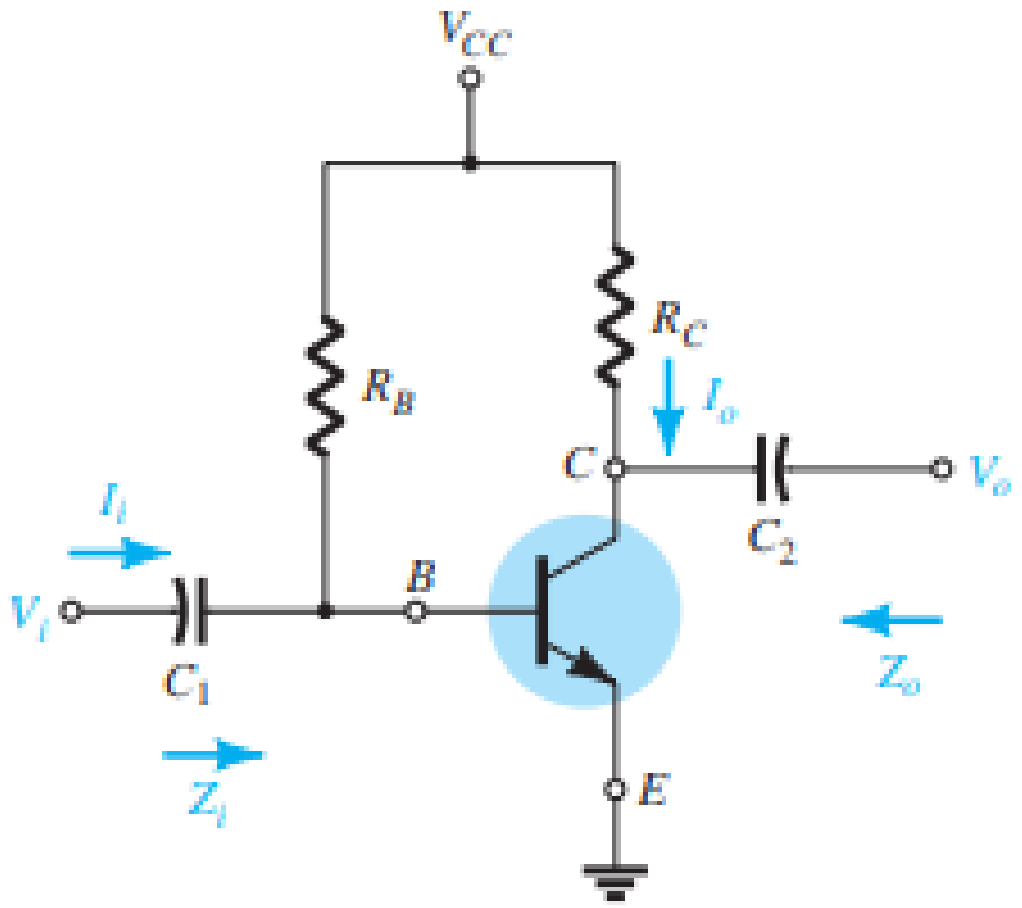
h-Parameter equivalent circuit of a transistor

Common Base Configuration



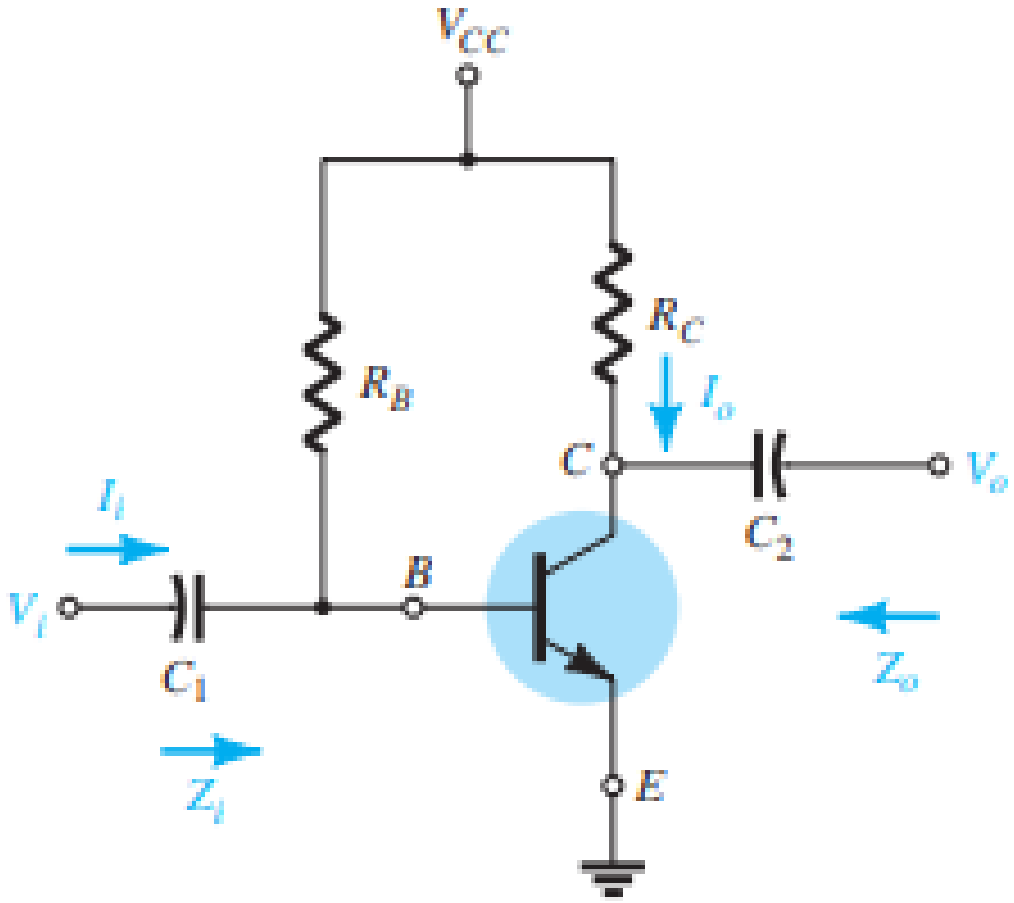

I_i
I_e
I_c
I_o
E
+
V_i
Z_i
r_e
$I_c = \alpha I_e$
r_o
Z_o
V_o
+
B
−
−

Fixed Bias Network

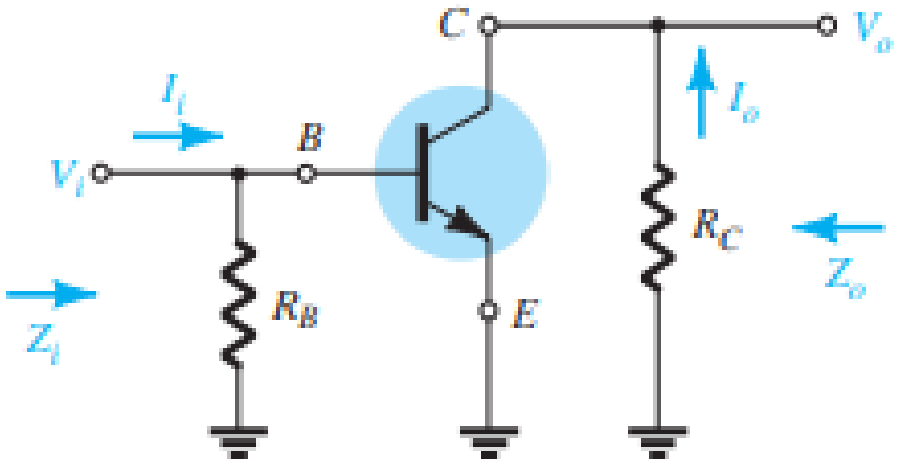


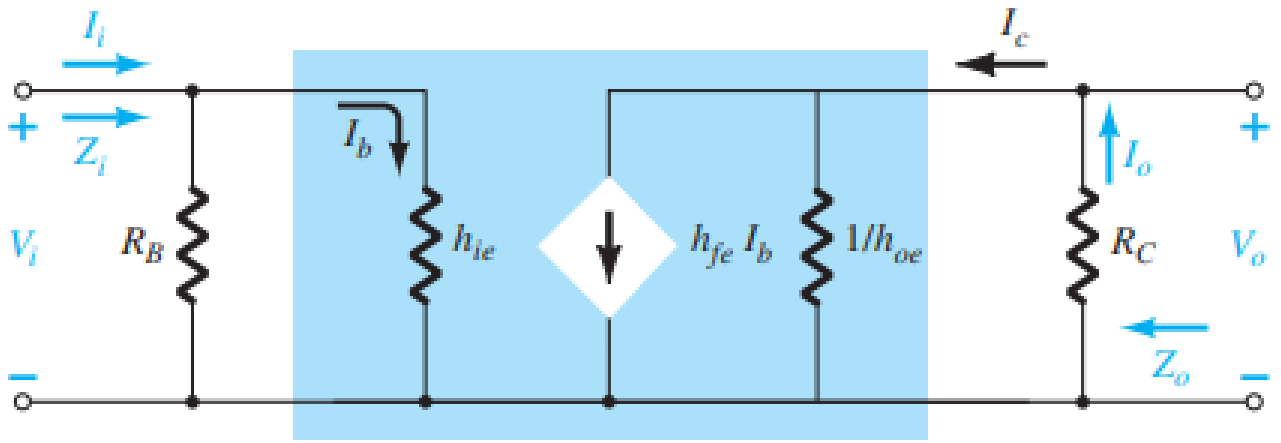
Steps

- 1. Connect the DC source to ground
- 2. Replace all the capacitance with short circuit
- 3. Re draw the network
- 4. write the AC equivalent circuit
- 5. Determine input impedance, output impedance, voltage gain and current gain


V_{CC}
R_B
R_C
I_o
C
V_o
C_2
I_i
B
V_i
C_1
Z_o
Z_i
E

Contd..




I_i
I_c
+
Z_i
I_b
I_o
+
V_i
R_B
h_{ie}
$h_{fe}\, I_b$
$1/h_{oe}$
R_C
V_o
Z_o
−
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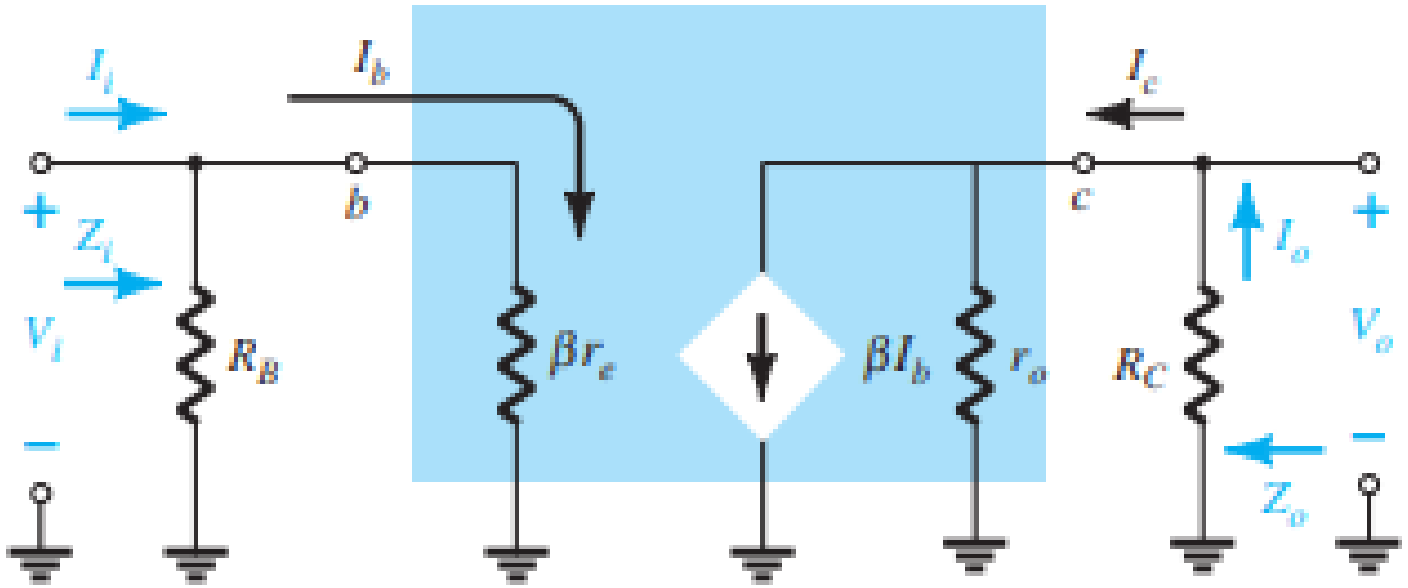


$$Z_i = R_B \| h_{ie}$$

$$Z_o = R_C \| 1/h_{oe}$$

Using $R' = 1/h_{oe} \| R_C$, we obtain

$$V_o = -I_o R' = -I_C R'$$
$$= -h_{fe} I_b R'$$

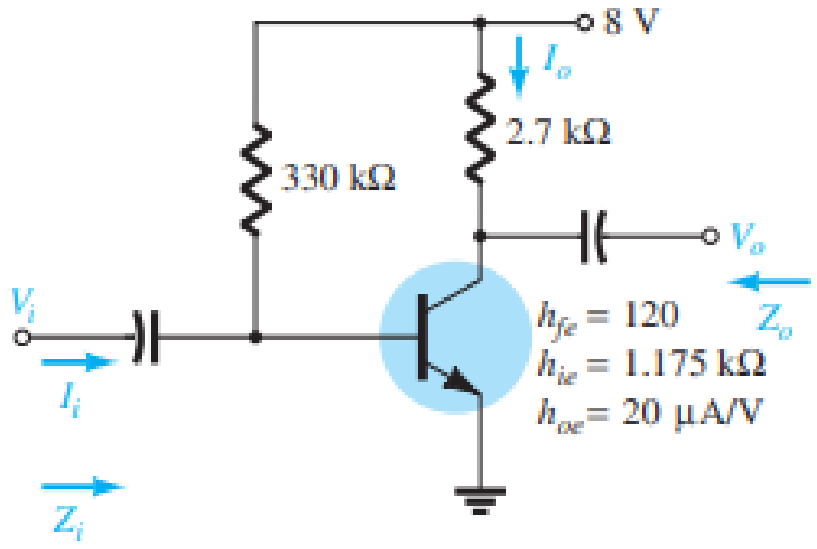
$$I_b = \frac{V_i}{h_{ie}}$$

$$A_v = \frac{V_o}{V_i} = -\frac{h_{ie}(R_C \| 1/h_{oe})}{h_{ie}}$$

A_I Assuming that $R_B \gg h_{ie}$ and $1/h_{oe} \geq 10R_C$, we find $I_b \cong I_i$ and $I_o = I_c = h_{fe}I_b = h_{fe}I_i$, and so

$$A_i = \frac{I_o}{I_i} \cong h_{fe}$$

- For the network shown in figure determine
- Zi, Zo, Av, Ai



$$Z_i = R_B \| h_{ie} = 330\,\text{k}\Omega \| 1.175\,\text{k}\Omega$$

$$\cong h_{ie} = \mathbf{1.171\,k\Omega}$$

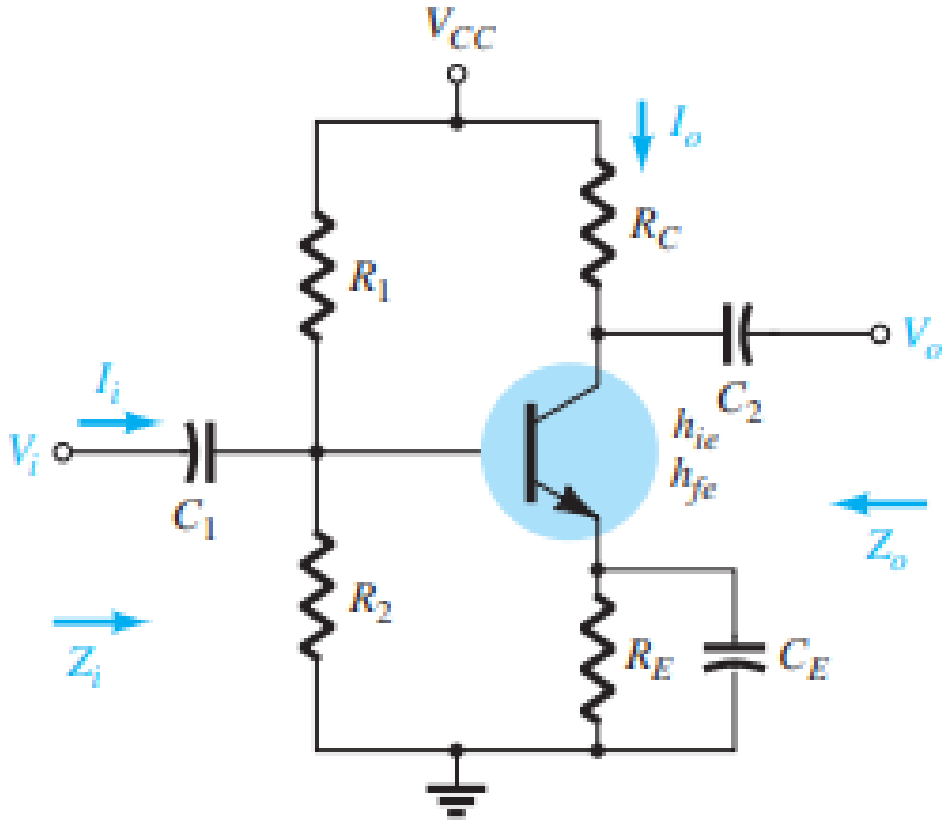
$$r_o = \frac{1}{h_{oe}} = \frac{1}{20\,\mu\text{A/V}} = 50\,\text{k}\Omega$$

$$A_v = -\frac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}} = -\frac{(120)(2.7\,\text{k}\Omega \| 50\,\text{k}\Omega)}{1.171\,\text{k}\Omega} = \mathbf{-262.34}$$

$$A_i \cong h_{fe} = \mathbf{120}$$

$$Z_o = \frac{1}{h_{oe}} \| R_C = 50\,\text{k}\Omega \| 2.7\,\text{k}\Omega = \mathbf{2.56\,k\Omega} \cong R_C$$

Voltage Divider Bias Network



$$Z_i = R_1 \| R_2 \| h_{ie}$$

$$Z_o \cong R_C$$

$$A_v = -\frac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}}$$

$$A_i = \frac{h_{fe}(R_1 \| R_2)}{R_1 \| R_2 + h_{ie}}$$

$$Z_i = R_B \| \beta r_e \quad \text{ohms}$$

$$Z_o = R_C \| r_o \quad \text{ohms}$$

$$Z_i \cong \beta r_e \qquad R_B \geq 10\beta r_e \quad \text{ohms}$$

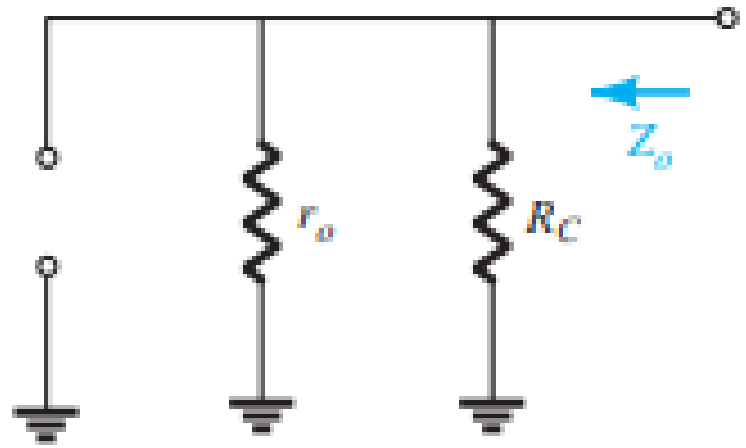
$$Z_o \cong R_C \qquad r_o \geq 10R_C$$

Contd..

$$V_o = -\beta I_b (R_C \| r_o)$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta \left(\frac{V_i}{\beta r_e} \right) (R_C \| r_o)$$



Contd..

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e}$$

$$A_v = -\frac{R_C}{r_e}$$

$r_o \geq 10R_C$