

Dr. Ambedkar Institute of Technology, Bengaluru-560056 Outcome Based Education (OBE) and Choice Based Credit System B.E. Name of the Programme: Electrical and Electronics Engineering Scheme of Teaching and Examination effective from the Academic Year 2026-27 (Batch 2025)
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III Semester	
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Sl · No	Course and Course Code		Course Title	Teaching Department (TD)and Question Paper Sett ing Board (PSB)		Teaching and Learning Scheme					Examination				Credits
						Class room Instruction (CI)hours per semester		Laboratory Instruction (LI)hours Per semester	Term work & s elf-learning in hours	Tea Learning hours per semester	Duration in h ours	CIE Marks	SEE Marks	Total Marks	
						L	T	P	TW+SL						
1	ASC	1BMAT301xx	Mathematics course	TD/PSB: Mathematics		42	28	0	50	120	3	50	50	100	4
2	IPCC	1BSESU302	Digital System Design using Verilog	TD:EEE PSB: ECE		42	0	28	50	120	3	50	50	100	4
3	PCC	1BSEST303	Network Analysis	TD:EEE PSB: EEE		42	28	0	50	120	3	50	50	100	4
4	PCC	1BSEST304	Analog Electronics and Linear Integrated Circuits	TD:EEE PSB: ETE		42	0	0	48	90	3	50	50	100	3
5	PCC	1BEET305	Transformers and Generators	TD:EEE PSB: EEE		42	0	0	48	90	3	50	50	100	3
6	PCCL	1BSESL306	Analog Electronics and Linear Integrated Circuits Lab	TD:EEE		0	0	28	2	30	2	50	50	100	1
7	AEC	1BEEL307x	Ability Enhancement Course Laboratory (Transformers and Generators lab)	TD:EEE		0	0	28	2	30	2	50	50	100	1
8	SDC	1BPRJ308	Community Project (Project-Based Learning)/Societal Project	TD:EEE		0	0	0	30	30	2	50	50	100	1
9	MC	1BCDN309	Placement	Placement Cell		2	0	0	0	--	--	50	--	50	PP/NP
10	NCMC	1BNSN310	National Service Scheme (NSS)	Concerned campus Staff.(CIE: Viva – Voce and demonstrations)	NSS coordinator	0	0	0	28	28	--	100	---	100	PP
		1BPEN310	Physical Education (PE) (Sports and Athletics)		Physical Education Director										
		1BYON310	Yoga		Yoga Teacher										
		1BMUN310	Music		Music Teacher										
Total (In case of regular students)										658	--	550	400	950	21
11	NCMC	1BMATDIP311	Mathematics course for Lateral Entry Students	Mathematics		14	0	0	14	28	---	100	---	100	PP
Total (In case of lateral-entry students not exempted from studying 1BMATDIP311)										686		650	400	1050	21
Ability Enhancement Course (Laboratory)															
1BEEL307A		Transformers and Generators lab		1BEEL307B		Electric Circuit Lab									

Course Title	DIGITAL SYSTEM DESIGN USING VERILOG						
Course Code	1BSESU302						
Course Category	IPCC (Integrated Professional Core Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	3	0	1	0	4	42+0+28+50=120	4
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	Analyze and simplify combinational logic circuits using Boolean algebra, Karnaugh maps, Quine-McCluskey minimization, and Don't Care conditions, and explain the basic Verilog design flow, data types, modules, and ports.
CLO2	Design and analyze combinational logic circuits using MSI components such as adders, subtractors, comparators, decoders, encoders, and multiplexers, and describe them using Verilog data-flow modeling.
CLO3	Analyze and design sequential circuits using latches, master-slave JK flip-flops, characteristic equations, and registers, and implement procedural assignments using Verilog behavioral modeling.
CLO4	Analyze and design binary ripple counters, synchronous binary counters, and shift-register-based counters, and develop their Verilog behavioral descriptions using conditional statements, multiway branching, and loops.
CLO5	Design and implement synchronous mod-n counters using T, JK, D, and SR flip-flops, and model sequential circuits using Verilog structural description with gate-level constructs.

SYLLABUS	No. of Hours	BTLs
UNIT 1	9	L1-L4
PRINCIPLES OF COMBINATIONAL LOGIC: Definition of combinational logic, Generation of switching equations from truth tables, Karnaugh maps- up to 4 variables, Quine-McCuskey Minimization Technique. Quine-McCuskey using Don't Care Terms. INTRODUCTION TO VERILOG: Typical Design Flow, Data types, Modules, Ports.		
SELF-STUDY COMPONENTS: Boolean Algebra, De Morgan's theorem, Truth table, Canonical forms (SOP and POS). Basics about different Hardware Description Languages.		
UNIT 2	9	L1-L4
LOGIC DESIGN WITH MSI COMPONENTS AND PROGRAMMABLE LOGIC DEVICES: Binary Adders and Subtractors, Ripple Carry Adder, BCD Adder, Comparators, Decoders, Encoders, Multiplexers. VERILOG DATA FLOW DESCRIPTION: Continuous assignments, Delays, Expressions, Operators, and operands, operator types, Examples.		
SELF-STUDY COMPONENTS: Practice designing logic functions using Decoders, Encoders, and Multiplexers. Basics about Data flow modelling		

UNIT 3	9	L1-L4
FLIP-FLOPS: The basic Bistable Element, Latches, JK, SR T and D Flip-Flops, The Master-Slave Flip-flops (Pulse-Triggered flip-flops): JK Flip Flop, Characteristic equations. VERILOG BEHAVIORAL DESCRIPTION: Introduction, Procedural Assignments.		
SELF-STUDY COMPONENTS: Design of 4-bit Synchronous Counters using T, JK, D, SR Flip-Flops. Basics of Behavioral Modelling.		
UNIT 4	9	L1-L4
FLIP-FLOPS AND ITS APPLICATIONS: Registers-SISO,SIPO,PISO,PIPO, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers- Ring and Johnson Counter VERILOG BEHAVIORAL DESCRIPTION: Conditional statements, Multiway branching, Loops, Examples.		
SELF-STUDY COMPONENTS: Learn to write Verilog code for Sequential circuits using Behavioral Modelling.		
UNIT 5	9	L1-L4
DESIGN OF SYNCHRONOUS COUNTER: Design of Synchronous Mod-N Counter using clocked T, JK, D and SR flip-flops. VERILOG STRUCTURAL DESCRIPTION: Gate types, Examples. (Gate level description only)		
SELF-STUDY COMPONENTS: Learn to write Verilog code for Sequential circuits using Behavioral & Structural Modelling.		
PRACTICAL COMPONENTS OF IPCC Using suitable simulation software, demonstrate the operation of the following circuits		
Experiments		
1. To simplify the given Boolean expressions and realize using Verilog program. 2. To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description. 3. To realize 4-bit ALU using Verilog program. 4.To realize the following Code converters using Verilog Behavioral description a) Gray to binary b) Binary to Gray 5.To realize using Verilog Behavioral description: 4:1 mux, 8:3 encoder, Priority encoder 6.To realize using Verilog Behavioral description: 1:4 Demux, 3:8 decoder, 2-bit Comparator 7.To realize using Verilog Behavioral description: Flip-flops: a) JK b) SR 8.To realize using Verilog Behavioral description: Flip-flops: a) T b) D		
Demonstration Experiments		
9. Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps). 10. Verilog programs to interface a Relay or ADC to the FPGA/CPLD and demonstrate its working. 11. Verilog programs to interface DAC to the FPGA/CPLD for Waveform generation. 12.Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.		

TEXT BOOKS:	
1	Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2006.
2	Digital Principles and Design by Donald D Givone, McGraw Hill, 2017.
3	Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar, 2 nd Edition 2003, Prentice Hall.

REFERENCE BOOKS:	
1	Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning, 2013.
2	Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2010.
3	Fundamentals of HDL, by Cyril P R, Pearson/Sanguine, 2010.

E-LEARNING RESOURCES:	
1	Hardware Modeling using Verilog https://nptel.ac.in/courses/106105165
2	Digital Design with Verilog https://nptel.ac.in/courses/106103358

Assessment Details both (CIE and SEE)				
The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass. CIE: The CIE has two components – CIE - theory component and CIE – laboratory component. Students have to score a minimum of 40% Marks in the total of CIE - theory and CIE – laboratory components put together, provided students have to score a minimum of 40% marks in CIE laboratory component alone to qualify to take SEE. Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks. **Self-Study The self-study component shall not be included in the SEE. For the CIE, a 5-mark question from the self-study component may be included as either Question 2(b) or Question 2(c).				
CONTINUOUS INTERNAL EVALUATION (CIE)			Max. Marks	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Theory	Weightage of CIE1 and CIE2 Tests or CIE3		30	12
Laboratory components	Rubrics for experiment are added, then taken average	10	20	08
	Lab CIE	10		
TOTAL			50	20

QUESTION PAPER PATTERN (SEE)										
Q. No.	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										

2. Student shall answer five full questions selecting one full question from each unit.

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Analyze and simplify combinational logic circuits using Boolean algebra, Karnaugh maps, and Quine-McCluskey minimization techniques, and understand the fundamentals of Verilog HDL.
CO2	Design and analyze combinational logic circuits using MSI components such as adders, subtractors, comparators, decoders, encoders, and multiplexers, using Verilog data-flow modeling.
CO3	Analyze and design sequential circuits using latches, flip-flops, and registers, and implement sequential logic using Verilog behavioral modeling.
CO4	Design and analyze ripple counters, synchronous counters, and shift-register-based counters using appropriate sequential design techniques and Verilog behavioral constructs.
CO5	Design and implement synchronous mod-n counters using different types of flip-flops and describe sequential circuits using Verilog structural modeling at the gate level.

Mapping of CO's, PO's with PSO's														
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0														
CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2		1							2	2	
CO2	3	3	3	1	3							2	3	
CO3	3	3	3	1	3							2	3	
CO4	3	3	3	2	3				1		1	2	3	
CO5	3	3	3	2	3				1		2	2	3	

Mapping of CO's with Knowledge and Attitude Profile (WK)										
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0										
CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9	
CO1		3	3	2		1				
CO2		2	3	3	3	2				
CO3		2	3	3	3	2				
CO4		3	3	3	2	3				
CO5		2	3	3	3	3				

Mapping of CO's with Sustainable Development Goals (SDG)																	
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0																	
CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1				2													
CO2				2					1								
CO3				2					1								
CO4				2					1								
CO5				2					1								

Course Title	NETWORK ANALYSIS						
Course Code	1BSEST303						
Course Category	PCC (Professional Core Course)						
Teaching - Learning Scheme & Credits	L	T	P	S	Total	Total Teaching Hours	Credits
	3	2	0	0	5	42+28+0+50=120	4
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	Understand and apply fundamental circuit laws and theorems, such as Ohm's Law, Kirchhoff's Laws, and network theorems, in the analysis of both DC and AC circuits
CLO2	Analyze and solve electrical networks systematically using mesh and nodal analysis techniques.
CLO3	Examine the transient behavior of RL, RC and RLC circuits under DC excitation and determine initial and final conditions
CLO4	Apply Laplace Transform methods for the analysis of electrical circuits and the solution of circuit-related differential equations
CLO5	Evaluate and interpret two-port network parameters (Z, Y, h, and T) and understand the relationships among them in various electrical systems.

SYLLABUS	No. of Hours	BTLs
UNIT 1	(9L + 5T)	L1-L4
BASIC NETWORK ANALYSIS Active and passive elements, Ideal and practical voltage and current sources, Independent and dependent (controlled) sources, Source transformation and source shifting techniques, Network reduction methods: Star-Delta (Y- Δ) and Delta-Star (Δ -Y) transformation. Loop (Mesh) and Node analysis for DC and AC circuits with independent and dependent sources, Super-mesh and Super-node concepts and applications.		
SELF-STUDY COMPONENTS: - Applications of active and passive circuit elements in electrical systems. - Practical implementation of dependent (controlled) sources. - Software-based analysis of DC and AC networks using MATLAB/Simulink, LTspice, or PSpice. - Applications of Star-Delta transformation in power distribution networks. - Comparative study of Mesh Analysis and Node Analysis techniques. - Real-world applications of Super-mesh and Super-node methods in electrical circuit analysis.		
UNIT 2	(8L + 5T)	L1-L4
NETWORK THEOREMS: Superposition Theorem, Reciprocity Theorem, Thevenin's Theorem, Norton's Theorem, Maximum Power Transfer Theorem, Millman's Theorem. Analysis of linear DC and AC electrical networks using network theorems with independent and dependent sources.		
SELF-STUDY COMPONENTS: - Applications of Superposition, Thevenin's and Norton's Theorems in practical electrical circuits. - Millman's Theorem and its applications in multi-source electrical networks.		

• Comparison of different network theorems and their suitability for circuit analysis. • Application of Maximum Power Transfer Theorem in electrical and electronic systems. • Analysis of DC and AC networks using simulation tools such as MATLAB/Simulink, LTspice or PSpice. • Real-time applications of network theorems in power systems and electrical engineering circuits.		
UNIT 3	(9L+9T)	L1-L4
TRANSIENT BEHAVIOUR AND INITIAL CONDITIONS: Concept of initial conditions in electrical networks, Initial conditions of resistor, inductor and capacitor, Continuity conditions of inductor current and capacitor voltage, procedure for evaluating initial conditions, Behaviour of circuit elements under DC switching conditions and their representation, Evaluation of initial and final values in R-L, R-C and R-L-C circuits, transient response of series R-L, R-C and R-L-C circuits for DC excitation with initial conditions, classical solutions for first and second order differential equations for series R-L, R-C and R-L-C electrical networks.		
SELF-STUDY COMPONENTS: • Applications of transient response in electrical and electronic systems. • Use of MATLAB/Simulink, LTspice or PSpice for transient analysis of electrical circuits. • Comparison of first-order and second-order circuit responses. • Effect of circuit parameters (R, L and C) on transient response. • Practical applications of charging and discharging circuits. • Analysis of natural and forced responses of electrical networks.		
UNIT 4	(9L+5T)	L1-L5
LAPLACE TRANSFORMATION AND ITS APPLICATIONS TO ELECTRIC CIRCUITS: Introduction, properties of Laplace transform, Laplace transform of a derivative, integral, common forcing functions, initial value and final value theorems, time displacement theorem, Laplace Transform of a network and time domain solution for R-L, R-C, and R-L-C networks for DC excitations, and pulse input.		
Waveform Synthesis: Introduction, Basic types of special signals, Laplace transformation of special signal waveforms, Problems.		
SELF-STUDY COMPONENTS: • Analyse the transient response of an RL circuit using both classical and Laplace methods and compare the results. • Simulate an RC charging circuit under step and pulse excitation using MATLAB or LTspice. • Develop a MATLAB program to compute Laplace and inverse Laplace transforms of common functions. • Generate and analyse unit step, ramp, impulse, and pulse waveforms using MATLAB. • Compare analytical and simulation results for first-order and second-order circuits. • Prepare a summary chart of important Laplace transform pairs and theorems.		
UNIT 5	(7L+4T)	L1-L4
TWO PORT NETWORK: Introduction to two-port networks, Characterization in terms of impedance, admittance, hybrid, and transmission parameters, parameter conversions, Interconnection of two-port networks – Symmetry and Reciprocity.		
SELF-STUDY COMPONENTS: • Study the concept, classification, and applications of two-port networks.		

- Simulate a two-port network using MATLAB, LTspice, or Multisim and compare the results with analytical calculations.

TEXT BOOKS:

- | | |
|---|---|
| 1 | Hayt, Kemmerly and Durbin, “Engineering Circuit Analysis”, 10th Edition, TMH Publication, 2024. |
| 2 | M. E. Van Valkenburg, “Network Analysis”, 3rd Edition, PHI publisher, 2009. |
| 3 | Charles K Alexander Matthew N O Sadiku, “Fundamentals of Electric Circuits”, Mc Graw Hill, 5th Edition, 2022. |

REFERENCE BOOKS:

- | | |
|---|---|
| 1 | Roy Choudhury, “Networks and systems”, 2nd Edition, New Age International Publications, 2016. |
| 2 | Robert L and Boylestad “Introductory Circuit Analysis”, 4TH edition, Pearson publisher, 2010. |
| 3 | M Nahvi and J A Edminister, “Electric Circuits”, 2nd Edition, Schaum’s Series, 2002. |

e-LEARNING RESOURCES:

- | | |
|---|---|
| 1 | NPTEL (National Programme on Technology Enhanced Learning) <ul style="list-style-type: none"> ○ Website: https://nptel.ac.in ○ Courses: <ul style="list-style-type: none"> – <i>Basic Electrical Circuits</i> by Prof. Nagendra Krishnapura (IIT Madras) – <i>Network Analysis</i> by Prof. M. B. Patil (IIT Bombay) |
| 2 | MIT Open CourseWare <ul style="list-style-type: none"> ○ Website: https://ocw.mit.edu ○ Course: <i>Circuits and Electronics</i> (6.002) |
| 3 | All About Circuits <ul style="list-style-type: none"> • Website: https://www.allaboutcircuits.com • Features: In-depth tutorials, forum discussions, circuit simulation tools, calculators. |

Assessment Details both (CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass.

CIE: The CIE has three components – CIE - theory component, assignment and group activity. Students have to score a minimum of 40% Marks in the total of CIE - theory, assignment and group activity components put together to take SEE.

SEE: Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks.

****Self-Study** The self-study component shall not be included in the SEE. For the CIE, a **5-mark question** from the self-study component may be included as either **Question 2(b)** or **Question 2(c)**.

CONTINUOUS INTERNAL EVALUATION (CIE)		Max. Marks	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Theory	Weightage of CIE-1 and CIE-2 Tests or CIE-3	50	20
TOTAL		50	20

QUESTION PAPER PATTERN (SEE)										
Q. No.	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Apply Kirchhoff's laws to perform loop and nodal analysis for resistive and reactive networks.
CO2	Apply the basic electrical laws and theorems to simplify and analyse the complex electric circuits
CO3	Analyse and evaluate the initial and final conditions of RL, RC and RLC circuits and determine the transient response of electrical circuits.
CO4	Apply Laplace Transform techniques to solve first and second-order electrical circuits in the s-domain and analyze the electrical waveforms using standard test signals
CO5	Determine the parameters of two-port networks (Z, Y, h, and T) and analyse their behaviour in interconnected networks.

Mapping of CO's, PO's with PSO's														
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0														
CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	1	2							3	2	1
CO2	3	3	2	2	2							3	2	1
CO3	3	3	2	2	2							3	3	1
CO4	3	2	2	2	2							3	3	2
CO5	3	3	2	2	2		1					3	3	2

Mapping of CO's with Knowledge and Attitude Profile (WK)										
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0										
CO/SDG's	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9	
CO1	3	3	2	1						1
CO2	3	3	3	2	1					1
CO3	3	3	3	2	2	1				1
CO4	3	3	2	2	2	1	1			1
CO5	3	3	3	3	2	1	1	1		2

Mapping of CO's with Sustainable Development Goals (SDG)																	
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0																	
CO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1				3			1		2								
CO2				3			2		3		1						
CO3				3			3		3		1	1	1				
CO4				3			2		3		2	1	1				
CO5				3			3		3		2	2	2				

Course Title	ANALOG ELECTRONICS AND LINEAR INTEGRATED CIRCUITS						
Course Code	1BSEST304						
Course Category	PCC (Professional Core Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	3	0	0	0	3	42+0+0+48=90	3
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	Examine the AC behavior and frequency response of BJT amplifiers and hybrid equivalent model, including the qualitative study frequency effects such as Miller effect.
CLO2	Analyze Power amplifier circuits in different modes of operation.
CLO3	Understand types of MOSFET biasing and demonstrate the use of MOSFET amplifiers.
CLO4	Construct various electronic circuits using OPAMPs and different types of active filters.
CLO5	Explain the working principle, block diagram, and pin configuration of IC 565 PLL, and analyze its applications.

SYLLABUS	No. of Hours	BTLs
UNIT 1	09	L1-L4
BJT AC Analysis: Voltage Divider Configuration, hybrid Equivalent model. BJT Frequency Response: Low frequency analysis, low frequency response of BJT amplifier, Miller effect capacitance, High frequency response of BJT amplifiers- study of capacitors affecting frequency response. (Qualitative analysis).		
SELF-STUDY COMPONENTS: BJT AC Analysis – Voltage Divider Configuration BJT (basic transistor amplifier model) and its comparison with the hybrid model. Effect of load impedance and source resistance on gain. Cascaded BJT amplifier configurations (brief overview).		
UNIT 2	09	L1-L4
Feedback Amplifier: Feedback concepts, feedback amplifier types-- Voltage series, Voltage-shunt, Current Series, and Current Shunt Feedback. Oscillator: Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator. Power Amplifiers: Introduction and amplifier types, Transformer – Coupled class A Amplifier, Transformer – coupled Push – Pull circuits, Complementary –Symmetry Circuits, Amplifier distortion, Class C Amplifier.		
SELF-STUDY COMPONENTS: Effect of feedback on input/output impedance (qualitative). Comparison of Class A, B, AB, C amplifiers with efficiency calculations. Heat sinks and thermal considerations in power amplifiers.		
UNIT 3	09	L1-L4
MOSFET Biasing in MOS Amplifier Circuits: Fixing VGS, Fixing VG, Drain to Gate Feedback Resistor. Small Signal Operation and Modelling: The DC Bias Point, Signal Current in Drain, Voltage Gain, Small Signal Equivalent Circuit Models, Transconductance, The T Equivalent Circuit Model. MOSFET Amplifier Configuration: Basic Configurations, Characterizing Amplifiers, CS Amplifier with And Without Source Resistance, The Common Gate Amplifier, Source Follower.		

SELF-STUDY COMPONENTS: JFET biasing techniques (fixed bias, self-bias, voltage-divider bias). FET small-signal model and parameters (gm, rd). Applications of MOSFET as a switch in digital circuits.		
UNIT 4	09	L1-L4
Operational amplifier: Introduction, block diagram and parameters definition. Op- amp applications: Difference amplifier, instrumentation amplifier. Sample and Hold circuit, Active filters-LP, HP, BP, BR.		
SELF-STUDY COMPONENTS: Ideal vs practical op-amp characteristics (CMRR, slew rate, offset voltage). Summing and integrator/differentiator circuits. Design considerations for instrumentation amplifiers in sensor applications.		
UNIT 5	09	L1-L4
Op-amp comparator: Zero crossing detectors and Schmitt trigger-inverting mode. Converter: A/D – Successive approximation, flash ADC, D/A - Weighted R-2R ladder DAC. IC 565 – Phase Locked Loop (PLL): Introduction to PLL, Block diagram, Pin diagram and description, Operating Principle, Operation of Principle, Applications.		
SELF-STUDY COMPONENTS: Comparator circuit and applications. Dual-slope ADC working principle (brief). IC 565 PLL pin configuration and practical applications such as Free running Oscillator and FM applications.		

TEXT BOOKS:	
1	Robert L. Boylestad and Louis Nashelsky, “Electronic Devices and Circuit Theory”, 11th Edition, Pearson Education, 2015.
2	D. Roy Choudhury, Shail B Jain,” Linear Integrated Circuits”, 4th Edition, New Age International limited, 2019.
3	Adel S. Sedra & Kenneth C. Smith, “Micro Electronic Circuits”, 7th Edition, Oxford University Press, 2017.

REFERENCE BOOKS:	
1	Muhammad Rashid, “Microelectronics Circuits Analysis and Design”, 2nd edition, Cengage Learning, 2014.
2	S. Salivahanan N. Suresh, “Electronic Devices and Circuits”, 3rd edition, Mc Graw Hill publisher, 2013.
3	Millman and Halkias, “Electronic Devices and Circuits”, 4th Edition, Mc Graw Hill, 2015.
4	Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, Pearson, 4th Edition 2015
e-LEARNING RESOURCES:	
1	https://www.tutorialspoint.com/electronic_circuits/electronic_circuits_introduction.htm
2	https://www.electronicshub.org/tutorials/4 .
3	https://nptel.ac.in/courses/108102112
4	http://nptel.vtu.ac.in/econtent/courses/EEE/10EE54/index.php

Assessment Details both (CIE and SEE)			
The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass. CIE: The CIE has three components – CIE - theory component, assignment and group activity. Students have to score a minimum of 40% Marks in the total of CIE - theory, assignment and group activity components put together to take SEE. SEE: Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks. **Self-Study The self-study component shall not be included in the SEE. For the CIE, a 5-mark question from the self-study component may be included as either Question 2(b) or Question 2(c) .			
CONTINUOUS INTERNAL EVALUATION (CIE)		Max. Marks	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Theory	Weightage of CIE1 and CIE2 Tests or CIE3	50	20
TOTAL		50	20

QUESTION PAPER PATTERN (SEE)										
Q. No.	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
UNIT	1	2	3	4	5	6	7	8	9	10
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Describe the working principle, fundamental characteristics of various semiconductor devices such as BJT, FET, MOSFETs, and operational amplifiers in electronic circuits.
CO2	Understand and Analyze various Power Amplifiers and FET biasing Techniques, evaluate performance parameters.
CO3	Analyze and Design FET Amplifier Circuits using Small Signal Models and appropriate Biasing Techniques and Evaluate Parameters.
CO4	Analyze various filter circuits using linear integrated circuits.
CO5	Understand the Structure and Parameters of Op-amp and Analyze its applications in Analog Signal Processing.

Mapping of CO's, PO's with PSO's														
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0														
CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2		2			1			1	1			1
CO2	3	2		2		1		2				2		
CO3			3		2		1				1			
CO4			3	2					1				3	
CO5	3	3	2	2							2	1	3	

Mapping of CO's with Knowledge and Attitude Profile (WK)									
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0									
CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	2	2	3	3	1	1			2
CO2	2	2	3	3	2	1			2
CO3	2	1	3	3	1	1			2
CO4	1	2	2	3	3	2	1	1	1
CO5	1	1	2	3	3	2	1	1	1

Mapping of CO's with Sustainable Development Goals (SDG)																	
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0																	
CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1				3			1		2								
CO2				3			1	1	2								
CO3				3			2		2								
CO4				3			2		3			1					
CO5				3			2	1	3			1					

Course Title	TRANSFORMERS AND GENERATORS						
Course Code	1BEET305						
Course Category	PCC (Professional Core Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	3	0	0	0	3	42+0+0+48=90	3
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	To understand the working of transformers, their analysis and testing.
CLO2	To analyze three phase transformers in different configurations and operate in parallel.
CLO3	To study the working and applications of special transformers.
CLO4	To understand and analyse the working of synchronous generators and its voltage regulation.
CLO5	To analyse salient pole synchronous generator and operation of synchronous generators in parallel and on infinite busbars.

SYLLABUS	No. of Hours	BTLs
UNIT 1	9	L1-L4
Single phase Transformers: Necessity of transformers, principle of operation, Constructional details of core and windings, EMF equation, equivalent circuit, Operation of practical transformer under no-load and on load with phasor diagrams. Losses and Efficiency and condition for maximum efficiency. Open circuit and short circuit tests, calculation of equivalent circuit parameters. Polarity test, Sumpner's test. Predetermination of efficiency, voltage regulation and its significance. Parallel operation of single-phase transformers. Numerical Problems.		
<u>SELF-STUDY COMPONENTS:</u> Reasons for rating of transformers in kVA, Variation of losses with load, methods of reducing losses in transformers.		
UNIT 2	9	L1-L4
Three-phase Transformers: Introduction, Three phase transformers in single units or in banks of three, Transformer connection for three phase operation– star/star, delta/delta, star/delta, and delta/open delta, Parallel Operation of Transformers: Necessity of Parallel operation, conditions for parallel operation, Load sharing in case of similar and dissimilar transformers., Numerical Problems.		
<u>SELF-STUDY COMPONENTS:</u> Comparative features of poly phase connections with reference to vector group, Labelling of three-phase transformer terminals.		
UNIT 3	9	L1-L4
Three-Phase Transformers (continued): Voltage regulation by Tap changing on load and on no-load. Scott connected transformer. Autotransformers: Introduction, copper economy, equivalent circuits, numerical problems. Instrument transformers- Current Transformers (CT) and Potential Transformers (PT): Construction, Operation, and Applications. Welding transformers: construction and operation.		
<u>SELF-STUDY COMPONENTS:</u> Introduction, Working & applications of pulse transformer.		
UNIT 4	9	L1-L4

Synchronous Generators: Constructional features of salient and cylindrical types, excitation systems – static and brushless, working, Armature windings, winding factors, EMF equation; Armature reaction, Synchronous reactance, Equivalent circuit; Synchronous Generators Analysis: Open circuit and short circuit characteristics, short circuit ratio, Alternator on load; Voltage regulation, Voltage regulation by EMF, MMF, and ZPF methods. Numerical Problems.		
SELF-STUDY COMPONENTS: Excitation control for constant terminal voltage when operating on its own load and on infinite bus.		
UNIT 5	9	L1-L4
Synchronous Generators (Salient Pole): Effects of saliency, two-reaction theory, Direct and quadrature axis reactances, slip test, electromagnetic power developed in the salient generators. Power angle characteristic (salient and non-salient pole), power angle diagram, reluctance power, Parallel operation of generators and load sharing; Synchronizing power, Hunting and damper windings. Numerical Problems.		
SELF-STUDY COMPONENTS: Capability curve for large turbo generators. Methods of synchronization.		

TEXT BOOKS:	
1	Electric Machines, D. P. Kothari, et al, 4th Edition, 2011
2	Electric Machines, Ashfaq Hussain, Dhanpat Rai & Co, 2nd Edition, 2013.

REFERENCE BOOKS:	
1	Electric Machinery, A E Fitzgerald, Charles Kingsley, Stephan Umans, McGraw-Hill.
2	Electric Machinery, P.S. Bimbhra, Khanna Publishers.
3	Theory & Performance of Electrical Machine, J.B. Gupta, S.K. Kataria & Sons.
E-LEARNING RESOURCES:	
1	Videos and Lecture Notes: https://nptel.ac.in/courses/Electrical Machines

Assessment Details both (CIE and SEE)			
The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass. CIE: The CIE has three components – CIE - theory component, assignment and group activity. Students have to score a minimum of 40% Marks in the total of CIE - theory, assignment and group activity components put together to take SEE. SEE: Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks. **Self-Study The self-study component shall not be included in the SEE. For the CIE, a 5-mark question from the self-study component may be included as either Question 2(b) or Question 2(c) .			
CONTINUOUS INTERNAL EVALUATION (CIE)		Max. Marks	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Theory	Weightage of CIE1 and CIE2 Tests or CIE3	50	20
TOTAL		50	20

QUESTION PAPER PATTERN (SEE)

Q. No.	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
UNIT	1		2		3		4		5	
1. Two full questions (each of 20 Marks) are to be set from each unit.										
2. Student shall answer five full questions selecting one full question from each unit.										

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Explain the construction, operation and performance of single-phase transformers.
CO2	Analyse the operation, and performance of parallel operation of three-phase transformers.
CO3	Evaluate the construction, operation and performance and applications of special transformers.
CO4	Analyse the construction, operation and performance of synchronous generators.
CO5	Evaluate the steady-state performance of salient-pole and cylindrical-rotor synchronous.

Mapping of CO's, PO's with PSO's														
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0														
CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3					1					1	3		1
CO2	3	2				1					1	3		1
CO3	3	2				1					1	3		1
CO4	3					1					1	3		1
CO5	3	2				1					1	3		1

Mapping of CO's with Knowledge and Attitude Profile (WK)										
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0										
CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9	
CO1	3		3	3				1	1	
CO2	3		3	3				1	1	
CO3	3		3	3				1	1	
CO4	3		3	3				1	1	
CO5	3		3	3				1	1	

Mapping of CO's with Sustainable Development Goals (SDG)																	
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0																	
CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1	1	2	1				3					3					
CO2	1	2	1				3					3					
CO3	1	2	1				3					3					
CO4	1	2	1				3					3					
CO5	1	2	1				3					3					

Course Title	ANALOG ELECTRONICS AND LINEAR INTEGRATED CIRCUITS LAB LABORATORY						
Course Code	1BSESL306						
Course Category	PCCL (Professional Core Course Laboratory)						
Teaching - Learning Scheme & Credit	L	T	P	TW+SL	Total	Total Teaching Hours	Credit
	0	0	1	0	1	0+0+28+02 = 30	01
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	To provide practical exposure to design, setting up, and analyze various analog electronic and Op-Amp circuits.
CLO2	To design, set up, and analyze RC-coupled and feedback BJT amplifiers, and determine their gain, bandwidth, frequency response, and input/output impedance.
CLO3	To design and analyze power amplifier circuits (Class A and Class B) and characterize JFET amplifiers through their input/output characteristics.
CLO4	To measure and evaluate the performance of Op-Amp based circuits such as the difference amplifier and instrumentation amplifier.
CLO5	To design, test, and plot the frequency response of active filters and Examine the working of IC 565 PLL, and analyze its lock range and capture range for applications in FM.

Syllabus	
PART: A - CONVENTIONAL EXPERIMENTS	
1	BJT Amplifiers: Design and Verification of RC-Coupled amplifier, Determine gain, frequency response, input and output impedance.
2	Feedback Amplifiers: Design and Set-up the BJT Common Emitter Voltage Amplifier with Feedback and Determine the Gain, Bandwidth.
3	Power Amplifiers: Design and analysis of power amplifier circuits (Class A, Class B).
4	Characteristics and design of JFET amplifier: Plotting the input/output characteristics of JFET and Design of amplifier.
5	Measurement of Op-Amp parameters: Difference Amplifier and Instrumentation amplifier.
6	Comparators: i) Zero crossing detectors ii) Schmitt trigger circuit using Op-Amps.
7	Converters: Analog to Digital (ADC) i) Successive approximation ii) Flash ADC
8	Converters: Digital to Analog (DAC) Weighted R-2R ladder DAC
9	Active filters: Design and Test the Second Order Active Filters and Plot the Frequency Response: i) Low Pass Filter, ii) High Pass Filter
10	Active filters: i) Band Pass, ii) Band Reject.

11	IC 565: Frequency synthesis using IC 565.
12	IC 565: Applications of IC 565.
PART: B - TYPICAL OPEN-ENDED EXPERIMENTS	
Open-ended experiments are a type of laboratory activity where the outcome is not predetermined and students are given the freedom to explore, design, and conduct the experiment based on the problem statements as per the concepts defined by the course coordinator. It encourages creativity, critical thinking, and inquiry-based learning. Course Project: Students must do a mandatory course project (group size not more than 4 students) using to realize a functional analog circuit on PCB. A maximum of 5 marks shall be awarded for this project (to be evaluated along with the final internal test). Report to be submitted.	
1	Audio amplifier.
2	Electronic Pest Repellent Circuit.
3	Electronic Siren, Audiometer.

Teaching & Learning Process (Innovative Delivery Methods):

1	Active Learning Techniques
2	Problem-Based Learning (PBL)
3	Team-Based Learning (TBL)
4	Hands-On Experiments and Simulations

TEXT BOOKS:

1	Boylestad R. L. and L. Nashelsky, Electronic Devices and Circuit Theory, 10/e, Pearson Education India, 2009
2	Choudhury R., Linear Integrated Circuits, New Age International Publishers. 2008.

REFERENCE BOOKS:

1	Millman J. and C. C. Halkias, Integrated Electronics: Analog and Digital Circuits and Systems, Tata McGraw-Hill, 2010.
2	Gayakward R. A., Op-Amps and Linear Integrated Circuits, PHI Learning Pvt. Ltd., 2012.

E-LEARNING RESOURCES:

1	Analog Electronic Circuits Virtual Lab, IIT Kharagpur – Studies on BJT CE Amplifier — https://be-iitkgp.vlabs.ac.in/exp/ce-amplifier/simulation.html
2	Electronic Devices and Circuits Virtual Lab, IIT Kharagpur — http://vlabs.iitkgp.ac.in/ssd/index.html
3	Analog Electronic Circuits" by Prof. Shanthi Pavan, IIT Madras — https://onlinecourses.nptel.ac.in/noc26_ee65/preview
4	Multisim / PSpice – for BJT, FET, and Op-Amp circuit design and analysis
5	Proteus Design Suite – for circuit design, PCB layout, and simulation

Assessment Details both (CIE and SEE)			
The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass. CIE: The CIE has two components – CIE - theory component and CIE – laboratory component. Students have to score a minimum of 40% Marks in the total of CIE - theory and CIE – laboratory components put together, provided students have to score a minimum of 40% marks in CIE laboratory component alone to qualify to take SEE. Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks. **Self-Study The self-study component shall not be included in the SEE. For the CIE, a 5-mark question from the self-study component may be included as either Question 2(b) or Question 2(c).			
CONTINUOUS INTERNAL EVALUATION (CIE)		Max. Marks	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Laboratory components	Rubrics for each experiment are added, then taken average	30	20
	Lab CIE	20	
TOTAL		50	20

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Design and test simple Analog electronic circuits as per the specifications using discrete electronic components
CO2	Design and analyze Power Amplifiers.
CO3	Understand the FET circuits.
CO4	Measure the performance parameters of Op-Amp based difference and instrumentation amplifiers. Design and test the Op-amp applications.
CO5	Implement Timer circuits using IC Timer NE555

Mapping of CO's, PO's with PSO's														
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0														
CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	1	3				2	2		2		1
CO2	3	2	3	2	2				1	1		2		
CO3	2	2	3	2	2				1	1		1	2	
CO4	2	2	2	3	2				1	1		1	3	
CO5	2	2	3	2	3		1		2	2		1	1	2

Mapping of CO's with Knowledge and Attitude Profile (WK)										
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0										
CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9	
CO1	1	1	2	2	2	3		1	1	
CO2	1	1	2	3	3	3		1	1	
CO3	1	1	2	3	3	3		1	1	

Dr. Ambedkar Institute of Technology, Bengaluru - 560056
 School of Electricals, Electronics Sciences & Engineering
Program: Electrical & Electronics Engineering

Semester: III

Scheme: 2025

CO4	1	1	2	3	2	3		1	1
CO5	1	1	2	3	3	3		2	1

Mapping of CO's with Sustainable Development Goals (SDG)																	
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0																	
CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1				3					2								
CO2				3			1		2								
CO3				3			2		3								
CO4				3					2								
CO5				3			1		2								

Course Title	TRANSFORMERS AND GENERATORS LABORATORY						
Course Code	1BEEL307A						
Course Category	AEC (Ability Enhancement Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	0	0	1	0	1	0+0+28+02 = 30	1
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	To learn the conduction of tests on single-phase and three-phase transformers and determine equivalent circuit parameters and performance.
CLO2	To understand and analyse the performance of transformers under different operating conditions.
CLO3	To conduct experimental investigations on synchronous generators and to determine their performance.
CLO4	To study the voltage regulation of synchronous generators using different standard methods, to compare the results obtained.
CLO5	To understand and analyse the steady-state operating characteristics of synchronous generators.

Syllabus	
1	(1)Open-circuit and short-circuit tests on a single-phase step-up/step-down transformer and pre-determination of: (i) Efficiency and regulation, and (ii) Parameters of the equivalent circuit.
2	Polarity Test and Star–Delta Connection of Three Single-Phase Transformers with Efficiency and Regulation under Balanced Load.
3	Determination of Combined and Individual Transformer Efficiencies using Sumpner’s Test.
4	Parallel operation of two dissimilar single-phase transformers of different kVA ratings and determination of load sharing.
5	Comparison of performance of three single-phase transformers in delta–delta and V–V (open-delta) connections under load.
6	Scott connection for conversion of 3 phase supply to 2 phase supply and plot of secondary side voltages with respect to load variation
7	Direct load test on a three-phase synchronous generator to determine efficiency and regulation.
8	Determination of voltage regulation of an alternator by the EMF, MMF and POTIER TRIANGLE methods.
9	Performance of a synchronous generator connected to an infinite bus under constant load and variable excitation.
10	Determination of power-angle characteristics of a synchronous generator and determination of maximum power developed.
11	Slip test and determination of X_d and X_q .

Teaching & Learning Process (Innovative Delivery Methods):	
1	Active Learning Techniques
2	Problem-Based Learning (PBL)
3	Team-Based Learning (TBL)
4	Hands-On Experiments and Simulations

TEXT BOOKS:	
1	Course Manual

REFERENCE BOOKS:	
1	Electric Machines, D. P. Kothari, et al, 4th Edition, 2011.
2	Electric Machines, Ashfaq Hussain, Dhanpat Rai & Co, 2nd Edition, 2013.
3	Electric Machinery, P.S. Bimbhra, Khanna Publishers.
4	Theory & Performance of Electrical Machine, J.B. Gupta, S.K. Kataria & Sons.

E-LEARNING RESOURCES:	
1	Videos and Lecture Notes: http://www.nptel.ac.in
2	Self-learning through NPTEL, SWAYAM, and other MOOCs.

Assessment Details both (CIE and SEE)			
The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass. CIE: The CIE has two components – CIE - theory component and CIE – laboratory component. Students have to score a minimum of 40% Marks in the total of CIE - theory and CIE – laboratory components put together, provided students have to score a minimum of 40% marks in CIE laboratory component alone to qualify to take SEE. Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks. **Self-Study The self-study component shall not be included in the SEE. For the CIE, a 5-mark question from the self-study component may be included as either Question 2(b) or Question 2(c).			
CONTINUOUS INTERNAL EVALUATION (CIE)		Max. Marks	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Laboratory components	Rubrics for each experiment are added, then taken average	30	20
	Lab CIE	20	
TOTAL		50	20

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Conduct tests on single-phase and three-phase transformers and determine

	equivalent circuit parameters and performance.
CO2	Analyse the performance of transformers under different operating conditions.
CO3	Perform experimental investigations on synchronous generators and to determine their performance.
CO4	Evaluate the voltage regulation of synchronous generators using different standard methods, to compare the results obtained.
CO5	Determine the steady-state operating characteristics of synchronous generators.

Mapping of CO's, PO's with PSO's														
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0														
CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3		2	3		1	2	3	3		1	3	2	1
CO2	3		2	3		1	2	3	3		1	3	2	1
CO3	3		2	3		1	2	3	3		1	3	2	1
CO4	3		2	3		1	2	3	3		1	3	2	1
CO5	3		2	3		1	2	3	3		1	3	2	1

Mapping of CO's with Knowledge and Attitude Profile (WK)										
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0										
CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9	
CO1	2		3	3	2	2	1		2	
CO2	2		3	3	2	2	1		2	
CO3	2		3	3	2	2	1		2	
CO4	2		3	3	2	2	1		2	
CO5	2		3	3	2	2	1		2	

Mapping of CO's with Sustainable Development Goals (SDG)																	
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0																	
CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1				1	3												
CO2				1	3												
CO3				1	3												
CO4				1	3												
CO5				1	3												

Course Title	ELECTRIC CIRCUIT LAB						
Course Code	1BEEL307B						
Course Category	AEC (Ability Enhancement Course)						
Teaching - Learning Scheme & Credit	L	T	P	S	Total	Total Teaching Hours	Credit
	0	0	1	0	1	0+0+28+02=30	1
CIE Marks: 50	SEE Marks: 50		Total Max. Marks: 100			Duration of SEE: 03 Hrs	

Course Learning Objectives:	
CLO1	Understand the fundamental concepts of electrical circuit analysis using simulation tools..
CLO2	Develop the ability to analyze electrical circuits containing independent and dependent sources using mesh and nodal analysis techniques
CLO3	Verify fundamental network theorems such as Thevenin's, Norton's, Superposition, Reciprocity, and Maximum Power Transfer through simulation.
CLO4	Analyze the frequency response and resonance characteristics of series and parallel RLC circuits using simulation software
CLO5	Enhance practical skills in circuit modeling, simulation, result interpretation, and technical documentation.

Syllabus	
PART: A - CONVENTIONAL EXPERIMENTS	
1	To simulate and analyze electrical circuits containing independent and dependent sources using Mesh analysis and Nodal Analysis.
2	Simulation and verification Thevenin's theorem for the circuit independent and dependent sources.
3	Simulation and verification Norton's theorem for the circuit independent and dependent sources.
4	Simulation and verification superposition theorem for the circuit independent and dependent sources.
5	Simulation and verification Maximum Power transfer theorem for the circuit independent and dependent sources.
6	Determination of Resonance frequency and Bandwidth for Series RLC circuits.
7	Determination of Resonance frequency and Bandwidth for Parallel RLC circuits.
PART: B - TYPICAL OPEN-ENDED EXPERIMENTS	
Open-ended experiments are a type of laboratory activity where the outcome is not predetermined, and students are given the freedom to explore, design, and conduct the experiment based on the problem statements as per the concepts defined by the course coordinator. It encourages creativity, critical thinking, and inquiry-based learning.	
1	Simulation and verification Reciprocity theorem for the circuit independent and dependent sources.
2	Determination of Z and Y parameters for the given two port circuits.

Teaching & Learning Process (Innovative Delivery Methods):	
1	Active Learning Techniques
2	Problem-Based Learning (PBL)
3	Team-Based Learning (TBL)
4	Hands-On Experiments and Simulations

TEXT BOOKS:	
1	Hayt, Kemmerly and Durbin, “Engineering Circuit Analysis”, 10th Edition, TMH Publication, 2015.
2	Roy Choudhury, “Networks and systems”, 2nd Edition, New Age International Publications, 2016.
3.	M. E. Van Valkenburg, “Network Analysis”, 3rd Edition, PHI publisher, 2009.

REFERENCE BOOKS:	
1	A K Chakraborty, S P Ghosh, “Network Analysis and Synthesis”, 1st Edition, TMH publisher, 2009.
2	Robert L and Boylestad “Introductory Circuit Analysis”, 4TH edition, Pearson publisher, 2010.
3	M Nahvi and J A Edminister, “Electric Circuits”, 2nd Edition, Schaum’s Series , 2002.
e-LEARNING RESOURCES:	
1	https://www.khanacademy.org/science/electrical-engineering/ee-circuit-analysis-topic .
2	https://www.circuitlab.com/

Assessment Details both (CIE and SEE)			
The weightage of Continuous Internal Evaluation (CIE) and Semester End Exam (SEE) is 50% each. The students have to obtain a minimum of 40% marks individually both in CIE and SEE to pass. CIE: The CIE has two components – CIE - theory component and CIE – laboratory component. Students have to score a minimum of 40% Marks in the total of CIE - theory and CIE – laboratory components put together, provided students have to score a minimum of 40% marks in CIE laboratory component alone to qualify to take SEE. Theory Semester End Exam (SEE) is conducted for 100 marks (3 Hours duration) and reduced to 50 Marks. **Self-Study The self-study component shall not be included in the SEE. For the CIE, a 5-mark question from the self-study component may be included as either Question 2(b) or Question 2(c).			
CONTINUOUS INTERNAL EVALUATION (CIE)		Max. Marks	Minimum Marks to be scored in CIE, to qualify to take SEE (40% individually)
Laboratory components	Rubrics for each experiment are added, then taken average	30	20
	Lab CIE	20	
TOTAL		50	20

Course Outcomes: After the completion of the course, the student will be able to:	
CO1	Simulate and analyze electrical circuits containing independent and dependent sources using mesh and nodal analysis techniques.
CO2	Verify the Thevenin's, Norton's, and Superposition theorems for linear electrical circuits using simulation software.
CO3	Validate the Reciprocity and Maximum Power Transfer theorems through circuit simulation and interpret the obtained results.
CO4	Determine the resonance frequency and bandwidth of series and parallel RLC circuits through simulation and analyze their frequency response characteristics.
CO5	Determine the parameters of two port networks (Z, and Y) and analyse their behavior in interconnected networks

Mapping of CO's, PO's with PSO's														
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0														
CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3		3	2					1	2	3	3	
CO2	3	3		3	2					1	2	3	3	
CO3	3	3		3	2					1	2	3	3	
CO4	3	3		3	2					1	2	3	3	
CO5	3	3		3	2					1	2	3	3	

Mapping of CO's with Knowledge and Attitude Profile (WK)										
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0										
CO	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9	
CO1		3	3	3	2	3		2		
CO2		3	3	3	2	3		2		
CO3		3	3	3	2	3		2		
CO4		3	3	3	2	3		2		
CO5		3	3	3	2	3		2		

Mapping of CO's with Sustainable Development Goals (SDG)																	
Strength of correlation: Strongly related-3, Moderately related-2, Weakly related-1, Not related-0																	
CO/SDG	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CO1				3			1		3			2					
CO2				3			1		3			2					
CO3				3			1		3			2					
CO4				3			1		3			2					
CO5				3			1		3			2					