Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY

(An Autonomous Institute affiliated to VTU, Accredited by NAAC with 'A' grade)

BDA Outer Ring Road, Mallathalli,Bengaluru-56

Board Of Studies 2025-26

Aided By Govt. of Karnataka

Approved
PG Scheme and Syllabus
For
Academic Year 2025-26

Submitted by

Department of Electronics and Communication Engineering

M.tech in VLSI Design and Embedded Systems

To

DEAN (Academic)

Dr. Ambedkar Institute of Technology

Bengaluru-5600056

Scheme of Teaching and Examinations **2024** for **M. Tech. Program**

(As per the latest VTU scheme)

Effective from the Academic year 2025-26

I/II Semester Scheme and Syllabus for Forth-coming 2025 Batch students

III/IV Semester Scheme and Syllabus for the current 2024 Batch students

BOS Chairman | Dean(Academics) | Principal

Dr. Ambedkar Institute of Technology
Scheme of Teaching and Examinations – 2024
M. Tech VLSI Design and Embedded Systems
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
(Applicable to **2025** Batch)

I SEMESTER (Core Courses related to main Engineering Stream)

Sl. No	Course	Course Code	Course Title	Teaching Hours per Week			Examination				Credits
				Theory	Practical/Seminar	Tutorial/ Skill Development Activities	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	P	T/SDA					
1	PCC	MEC101	Digital VLSI design	03	00	00	03	50	50	100	3
2	IPCC	MEC102	Digital System Design Using Verilog	03	02	00	03	50	50	100	4
3	PCC	MEC103	Advanced Embedded System	02	00	02	03	50	50	100	3
4	PCC	MEC104x	Professional Elective I	02	00	02	03	50	50	100	3
5	PCC	MEC105x	Professional Elective II	02	00	02	03	50	50	100	3
6	PCCL	MECL106	VLSI Design and Embedded Systems Lab-I	01	02	00	03	50	50	100	2
7	NCMC	MRMI107	Research Methodology and IPR	Online Courses (online.vtu.ac.in)							PP/NP
8	NCMC	MCDN108	Career Development Skills-I	02	-	-	02	-	-	-	PP/NP
			TOTAL	**15**	**04**	**06**	**18**	**300**	**300**	**600**	**18**

Note: **BSC**-Basic Science Courses, **PCC**: Professional core. **PCC (PB):** Project Based Learning Course, **IPCC**-Integrated Professional Core Courses, **NCMC** - None Credit Mandatory Course, AUD/AEC –Audit Course / Ability Enhancement Course(A pass in AUD/AEC is mandatory for the award of the degree), **PCCL**-Professional Core Course lab, **L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities**(Hours are for Interaction between faculty and students).

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.
Project Based Learning Course (PCC(PB): is a professional core Course, only Students have to complete a project out of learning from the course and SEE will be viva voce on project work.
MRMI16-Research Methodology and IPR- None Credit Mandatory Course (NCMC) if students have **not studied** this course in their undergraduate program then he /she has to take this course at http://online.vtu.ac.in and to qualify for this course is compulsory before completion of the minimum duration of the program (Two years), however, this course will not be considered for vertical progression.
PCCL: Professional Core Course Laboratory: Practical courses whose CIE will be evaluated by the class teacher and SEE will be evaluated by the two examiners.
Skill development activities: Under Skill development activities in a concerning course, the students should

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyse and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.
Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

04 credits courses	50 hours of the Teaching-Learning process
04 credits course (IPCC)	40 hours of Teaching Learning process and 10-12 laboratory sessions
03 credits course	40 hours of Teaching Learning process
02 credits course	25 hours of Teaching Learning process
01 credit course	10-12 ours of Teaching Learning process

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Professional Elective 1		Professional Elective 2	
Course Code under MEC104x	**Course title**	**Course Code under MEC105x**	**Course title**
MEC104A	Advanced Machine Learning And Deep Learning	MEC105A	Design of VLSI systems
MEC104B	Multimedia And Applications	MEC105B	Pattern Recognition & Machine Learning
MEC104C	System Verilog Programming	MEC105C	ASIC
MEC104D	Synthesis and Optimisation of Digital Circuits	MEC105D	Digital Circuits & Logic Design

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M. Tech VLSI Design and Embedded Systems
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II SEMESTER (Core Courses related to main Engineering Stream)

Sl. No	Course	Course Code	Course Title	Teaching Hours per Week			Examination				Credits
				Theory	Practical/Seminar	Tutorial/ Skill Development Activities	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	P	T/SDA					
1	PCC	MEC201	Analog IC Design	03	00	00	03	50	50	100	3
2	IPCC	MEC202	Embedded OS	03	02	00	03	50	50	100	4
3	PCC	MEC203	VLSI Design Verification and Testing	03	00	00	03	50	50	100	3
4	PCC	MEC204	Low Power VLSI Design	02	00	02	03	50	50	100	3
5	PCC	MEC205x	Professional Elective III	03	-	-	03	50	50	100	3
6	PCC	MEC206x	Professional Elective IV	03	-	-	03	50	50	100	3
7	PCCL	MECL207	VLSI Design and Embedded Systems Lab-II	01	02	00	03	50	50	100	2
8	AEC/SEC	MEC208x	Ability/Skill Enhancement Course(Offline/Online)	01			01	50	50	100	1
9	NCMC	MCDN209	Career Development Skills-II	02	-	-	02	-	-	-	PP/NP
			TOTAL	**15**	**04**	**06**	**18**	**300**	**300**	**800**	**22**

Note: **BSC**-Basic Science Courses, **PCC**: Professional core. **PCC (PB):** Project Based Learning Course, **IPCC**-Integrated Professional Core Courses, **NCMC** - None Credit Mandatory Course, AUD/AEC –Audit Course / Ability Enhancement Course(A pass in AUD/AEC is mandatory for the award of the degree), **PCCL**-Professional Core Course lab, **L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities**(Hours are for Interaction between faculty and students).

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.
Project Based Learning Course (PCC(PB): is a professional core Course, only Students have to complete a project out of learning from the course and SEE will be viva voce on project work.
Ability Enhancement Courses (AEC): These courses are designed to help students enhance their skills in communication, language, and personality development. They also promote a deeper understanding of subjects like social sciences and ethics, culture and human behaviour, human rights, and the law.
Skill Enhancement Course (SEC): Skill Enhancement Course means a course designed to provide value-based or skill-based knowledge and should contain both theory and lab/hands-on/training/fieldwork. The main purpose of these courses is to provide students with life skills in the hands-on mode to increase their employability.
If AEC/SEC courses are ONLINE (MOOCs) courses suggested by the concerned board of studies. These courses will be made available on www. online.vtu.ac.in, however online courses are not considered for vertical progression, but qualifying in online courses is mandatory for the award of the degree.
Skill development activities: Under Skill development activities in a concerning course, the students should

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyse and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.
Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

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Professional Elective 3		Professional Elective 4	
Course Code under MEC205x	**Course title**	**Course Code under MEC206x**	**Course title**
MEC205A	Digital IC design	MEC206A	Algorithms for VLSI Physical Design
MEC205B	CMOS RF Circuit Design	MEC206B	ARM Programming and Optimization
MEC205C	Multicore Architectures	MEC206C	High Speed VLSI Design
MEC205D	Static Timing Analysis	MEC206D	VLSI - DSP Architectures
Ability/Skill Enhancement Course(Offline/Online)- Refer online.vtu.ac.in courses			
MEC208A	Skill Enhancement with data structure algorithm	MEC208B	Computer Programming Skill with C
MEC208C	Object oriented programming using C++	MEC208D	Python essentials and libraries for Data Science

*The online courses list (online.vtu.ac.in courses) may vary from time to time depending on the availability of courses at the time of registration and upon the recommendations from the BoS.

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For the students who are willing to take an Industry Internship for one-semester duration and independent project work next semester

III SEMESTER (B)

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week			Examination				Credits
				Theory	Practical/ Mini–Project/ Internship	Tutorial/ Skill Development Activities	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	P	SDA					
1	PEC/MDC	MEC301	(Online Courses) 12 weeks duration							100	3
2	PEC/MDC	MEC302	(Online Courses) 12 weeks duration							100	3
3	PEC/MDC	MEC303	(Online Courses) 12 weeks duration							100	3
4	INT	MECI304	Industry-Internship	One-semester duration				100	100	200	11
TOTAL				**06**	**00**	**00**		100	100	**500**	**20**

Note:
Mxxx301/401 to 303/403: MOOC courses of **12 weeks** duration are the courses suggested by the Board of Studies of the University and will be displayed on www.online.vtu.ac.in. The online courses selected should not be the same as those studied in the first and second semesters of the program. The student will **not be eligible** to get their degree if they unintentionally **select online courses that match previously finished** courses. These courses are not considered for the vertical progression; however, qualifying for these courses and earning the credits is a must for the award of the degree. It is permitted to **complete** these online MOOC courses either in **3rd semester or in 4th semester**.

Industry Internship: The main objective of the industry internship is to ensure that the intern is exposed to a real-world environment and gains practical experience. Often, it may be a practical exposure to the theory that has been learned during the academic period. The industry internship helps students understand of analytical concepts and tools, hone their skills in real-life situations, and build confidence in applying the skills learned. The students who take up a one-semester Internship in the Industry have to appear SEE at the institute at the end of the semester as per the examination calendar.
Project Work: Students in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of the Project. Subsequently, the students shall collect the material required for the selected project, prepare a synopsis, and narrate the methodology to carry out the project work. Each student, under the guidance of a Faculty, is required to
- Present the seminar on the selected project orally and/or through Power Point slides.
- Answer the queries and be involved in debate/discussion.
- Submit two copies of the typed report with a list of references.
- The participants shall take part in discussions to foster a friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Those, who have **not pursued /completed** the internship, shall be declared as **fail** in the internship course and have to complete the same during subsequent University examinations after satisfying the internship requirements. Internship SEE (University examination) shall be as per the University norms.
CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.

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IV SEMESTER (B)

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work	Duration in hours	CIE Marks	SEE Marks Viva voce	Total Marks	
				L	P					
1	PROJ	MEC401	Project	04	08	03	100	100	200	20
			TOTAL	**04**	**08**	**03**	**100**	**100**	**200**	**20**

CIE marks for the project report (20 marks), seminar (20 marks) and question and answer (10 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Principal. The committee shall consist of internal guide and a faculty from the department with the senior most acting as the Chairperson.

Semester End Examination SEE marks for the project report (30 marks), seminar (10 marks) and question and answer session (10 marks) shall be awarded (based on the quality of the report and presentation skill, participation in the question and answer session) by the examiners appointed by the University.

Project Work: The project work shall be carried out individually. However, in case a disciplinary or interdisciplinary project requires more participants, then a group consisting of not more than three shall be permitted.

Students in consultation with the guide/co-guide (if any) in disciplinary project or guides/co-guides (if any) of all departments in case of multidisciplinary projects, shall pursue a literature survey and complete the preliminary requirements of the selected Project work. Each student shall prepare a relevant introductory project document, and present a seminar.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, all Guide/s and co-guide/s (if any) and a senior faculty of the concerned departments. The CIE marks awarded for project work shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.

SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check, shall be as per the University norms.

I Semester Syllabus
(2025 BATCH)

As per latest VTU

Subject Title: **Digital VLSI design**		
Subject Code: **MEC101**	No. of Credits: **03 = 3:0:0 (L:T:P)**	No. of lecture hours per week: **03**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **40**

Course Learning Objectives: This course will enable the students to:

1. Understand the MOSFET structures (fabrication processes) and operations.
2. Ability to explain VLSI Design Methodologies.
3. Learn Static and Dynamic operation principles, analysis and design of inverter circuit.
4. Concepts and techniques involved in the digital circuits design.
5. Outline the comprehensive coverage of Methodologies and Design practice that are used to reduce the Power Dissipation of large scale digital circuits.
6. Analyze the IC design process.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**MOS Transistor**: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects. **Modelling of MOS Transistor using SPICE:** Basic Concepts, The LEVEL 1 Model Equations, The LEVEL 2 Model Equations ,The LEVEL 3 Model Equations, Capacitance Models, Comparison of the SPICE MOSFET Models, Typical SPICE Model Parameters (from appendix) **[TEXT 1]**	**8**	L1,L2, L3
2	**MOS Inverters-Static Characteristics**: Introduction, Resistive-Load Inverter, Inverters with n Type MOSFET Load. **MOS Inverters-Static Characteristics**: CMOS Inverter. **MOS Inverters**: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitic, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters. **[TEXT 1]**	**8**	L1,L2, L3
3	**COMBINATIONAL MOS LOGIC CIRCUITS:** Introduction MOS Logic Circuits with Depletion nMOS Loads, CMOS Logic Circuits, Complex Logic Circuits, CMOS Transmission Gates (Pass Gates). **[TEXT 1]**	**8**	L1,L2, L3
4	**SEQUENTIAL MOS LOGIC CIRCUITS**: Introduction, Contents Behaviour of Bistable Elements, The SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, CMOS D-Latch and Edge-Triggered Flip-Flop Schmitt Trigger Circuit(Ref Appendix of the chapter). **[TEXT 1]** **Bi-CMOS Logic Circuits**: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behaviour of BJTs. Basic BiCMOS Circuits: Static Behaviour, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications. **[TEXT 1]**	**8**	L1,L2, L3
5	**DYNAMIC LOGIC CIRCUITS**: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits. **[TEXT 1]**	**8**	L1,L2, L3, L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Model the MOS transistor (PSPICE model) using the theoretical equations

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CO2	Design the CMOS inverter using the specifications
CO3	Design and simulate the combinational logic circuits using the different techniques
CO4	Construct and analyse the transistor level flip flops and latches using the CMOS and BICMOS technology.
CO5	Analyse and model the high performance dynamic CMOS circuits
Course outcome and program outcome mapping	
CO1	PO1,PO2,PO8,PO9,PO10
CO2	PO1, PO2, PO3, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Sung Mo Kang &Yusuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, McGraw-Hill (Third Edition), 2005.

REFERENCE BOOKS/WEBLINKS:

1. Sung Mo Kang &Yusuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, McGraw-Hill (Fourth Edition), 2014.
2. Neil Weste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective”, 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
3. Wayne, Wolf, “Modern VLSI design: System on Silicon” Pearson Education”, Second Edition, 2008.
4. Douglas A Pucknell & Kamran Eshragian , “Basic VLSI Design” PHI 3rd Edition (original Edition – 1994).
5. www.ntpel.com

Subject Title: **DIGITAL SYSTEM DESIGN USING VERILOG**		
Subject Code**: MEC102**	No. of Credits**: 04 = 3:0:2 (L:T:P)**	No. of lecture hours per week**: 04**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives

1 Understand digital system design methodologies.

2 Understand usage of Verilog in digital system design.

3 Understand various digital circuits, memory circuits and state logic for control circuits.

5 Understand FPGA design and floating point arithmetic.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction to Verilog:** Computer-Aided Design, Hardware Description Languages, Verilog Description of Combinational Circuits, Verilog Modules, Verilog Assignments, Procedural Assignments, Modeling Flip-Flops Using Always Block, Always Blocks Using Event Control Statements, Delays in Verilog, Compilation, Simulation, and Synthesis of Verilog Code. **[TEXT 1]**	8	L1,L2,L3
2	**Verilog Data Types and Operators**, Simple Synthesis Examples, Verilog Models for Multiplexers, Modeling Registers and Counters Using Verilog Always Statements, Behavioral and Structural Verilog, Constants, Arrays, Loops in Verilog, Testing a Verilog Model. **Floating-Point Arithmetic**: Representation of Floating-Point Numbers, Floating-Point Multiplication, Floating-Point Addition, Other Floating-Point Operations. **[TEXT 1]**	8	L1,L2 ,L3
3	**Additional Verilog topics**: Verilog Functions, Verilog Tasks, Multivalued Logic and Signal Resolution, Built-in Primitives, User-Defined Primitives, SRAM Model, Rise and Fall Delays of Gates, Named Association, Generate Statements, System Functions, Compiler Directives, File I/O Functions, Timing Checks. **[TEXT 1]**	8	L1,L2, L3,L4
4	**Design Examples**: BCD to 7-Segment Display Decoder, A BCD Adder, 32-Bit Adders, Traffic Light Controller, State Graphs for Control Circuits, Scoreboard and Controller, Synchronization and Debouncing, A Shift-and-Add Multiplier, Array Multiplier, A Signed Integer/Fraction Multiplier, Binary Dividers. **[TEXT 1]**	8	L1,L2, L3,L4
5	**Designing with Field Programmable Gate Arrays**: Implementing Functions in FPGAs, Implementing Functions Using Shannon's Decomposition, Carry Chains in FPGAs, Cascade Chains in FPGAs. **[TEXT 1]**	8	L2,L3, L4.

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

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COURSE OUTCOMES:	
After studying this course, students will be able to:	
CO1	Develop a Verilog code for digital circuits/systems
CO2	Develop floating point based arithmetic building blocks for ALU sub-systems.
CO3	Apply advanced Verilog features to develop digital systems.
CO4	Realize the various ALU sub-system blocks using behavioural methodology.
CO5	Implement digital circuits using Field Programmable Gate Arrays.

Course outcome and program outcome mapping	
CO1	PO1, PO2
CO2	PO2, PO3, PO4
CO3	PO3, PO4, PO5, PO6
CO4	PO4, PO5, PO6, PO7
CO5	PO5, PO6

TEXT BOOKS:

1. Byeong Kil Lee, Charles H Roth, and Lizy Kurian John, "*Digital Systems Design Using Verilog*", First Edition, Boston, MA : Cengage Learning, 2016.

REFERENCE BOOKS/WEBLINKS:

1. J. Bhaskar, "A Verilog HDL Primer", Third Edition, BS publications, Reprint 2023.
2. Samir Palnitkar, "A Guide to Digital Design and Synthesis", Sun Soft press, Reprint 2003.
3. Peter Ashenden ,"Digital Design: An Embedded Systems Approach Using Verilog", Morgan Kaufmann publishers, Elsvier, Reprint 2010.
4. www.ntpel.com

Session No	**Practical Session**	No of Hours	Blooms Taxonomy Level
1	Develop Verilog code for the multiplication of two unsigned binary numbers and signed binary numbers using the state machine. Verify the program with the help of a test bench.	**2**	L3, L4.
2	Develop Verilog code for the given sequence generation using the Mealy and More state machine. Verify the program with the help of a test bench.	**2**	L3, L4.
3	Develop a Verilog code for the division of two binary numbers. Verify the program with the help of a test bench.	**2**	L3,L4
4	Develop Verilog code for the multiplication of two floating point numbers. Verify the program with the help of a test bench.	**2**	L3,L4
5	Develop Verilog code for the SRAM model. Verify the program with the help of a test bench.	**2**	L3, L4.

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is

40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of IPCC

1. Two Tests each of 20 Marks
2. Two assignments each of 10 Marks / One Skill Development Activity of 20 Marks
3. Total Marks of two tests and two assignments / One Skill Development Activity added will be CIE for 60 Marks, marks scored will be proportionally scaled down to 30 Marks.

CIE for the practical component of IPCC

1. On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The 15 Marks are for conducting the experiment and preparation of the laboratory record, the other 05 Marks shall be for the test conducted at the end of the semester.
2. The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments 'write-ups are added and scaled down to15 marks.
3. The laboratory test at the end /after completion of all the experiments shall be conducted for 50 Marks and scaled down to 05 Marks. Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory Component of IPCC for 20marks.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers
for the course (duration 03hours)

1. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50marks.
2. The question paper will have ten questions. Each question is set for 20marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
4. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

1. The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20marks.
2. SEE will be conducted for 100marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of50% of maximum marks of the course(CIE+SEE)

<table>
<tr><td colspan="5">Subject Title: Advanced Embedded Systems</td></tr>
<tr><td>Subject Code: MEC103</td><td colspan="2">No. of Credits: 03 = 2:2:0 (L:T:P)</td><td colspan="2">No. of lecture hours per week: 02</td></tr>
<tr><td>Exam Duration: 3 Hours</td><td colspan="2">CIE + (Assignment + Seminar) + SEE = 40+10+50 =100</td><td colspan="2">Total No. of lecture hours: 40</td></tr>
<tr><td colspan="5">Course Learning Objectives: This course will enable the students to:
1. Understand the need of embedded systems.
2. Get exposure to the basic hardware components and their selection methods based on the characteristics and quality attributes of an embedded system.
3. Acquire the knowledge of the ARM based embedded systems, architectural features of ARM Cortex-M processors.
4. Describe the fundamental issues of embedded system design and development.
5. Get exposure to Multi-core architectures of embedded systems.</td></tr>
<tr><td>UNIT No.</td><td colspan="2">Syllabus Content</td><td>No. of hours</td><td>*BTL</td></tr>
<tr><td>1</td><td colspan="2">Embedded System: Embedded vs General computing system, application and purpose of Embedded System, Core of an Embedded System, Memory, Sensors, Actuators, LED, Optocoupler, keyboard, Communication Interface, Embedded firmware, Other system components, PCB and Passive components, Characteristics and Quality Attributes of Embedded Systems.(TEXT 1)</td><td>8</td><td>L1,L2, L3,L4</td></tr>
<tr><td>2</td><td colspan="2">ARM Embedded Systems: The RISC Design Philosophy, The ARM Design Philosophy, Embedded System Hardware, Embedded System Software.
ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts, and the Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.
(TEXT2)</td><td>8</td><td>L1,L2, L3,L4</td></tr>
<tr><td>3</td><td colspan="2">ARM Cortex-M3/M4 Processors: ARM Cortex-M processors, Architecture, Instruction Set, ARM Cortex-M3/M4 Processors based MCU (LPC1768 microcontroller). (TEXT 3)</td><td>8</td><td>L1,L2, L3,L4</td></tr>
<tr><td>4</td><td colspan="2">Embedded System Design and Development: Hardware Software Co-Design, embedded firmware design approaches, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Challenges in embedded computing system design, The embedded system design process-Requirements, Specification, Architecture design, Designing hardware and software components, System integration, Design flows. (TEXT 1 & 4)</td><td>8</td><td>L1,L2, L3,L4</td></tr>
<tr><td>5</td><td colspan="2">Multi-Core Architectures for Embedded Systems: Introduction, Architectural Considerations, Interconnection Networks, Software Optimizations, Case Studies: HiBRID-SoC for Multimedia Signal Processing, VIPER Multiprocessor SoC, Defect-Tolerant and Reconfigurable MPSoC, Homogeneous Multiprocessor for Embedded Printer Application, General Purpose Multiprocessor DSP, Multiprocessor DSP for Mobile Applications, Multi-Core DSP Platforms. (TEXT 5)</td><td>8</td><td>L1,L2, L3,L4</td></tr>
<tr><td colspan="5">*BTL: Blooms Taxonomy Level, L:T:P = Lecture: Tutorial : Practical
Note:
• Each Unit will have internal choice for SEE.
• The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.</td></tr>
</table>

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COURSE OUTCOMES:	
	After studying this course, students will be able to:
CO1	Identify the basic building blocks, characteristics and quality attributes of embedded systems.
CO2	Understand the fundamental issues of ARM processor and ARM based embedded systems.
CO3	Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
CO4	Design simple Embedded systems
CO5	Use Multi-core architectures in embedded system design and debugging.

Course outcome and program outcome mapping	
CO1	PO2, PO3, PO4, PO5, PO12
CO2	PO2, PO3, PO4, PO5, PO6, PO12
CO3	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO4	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO5	PO1, PO2, PO3, PO4, PO5, PO6, PO8, PO12

TEXT BOOKS:

1. **Introduction to Embedded Systems,** Shibu K V, Tata McGraw Hill Education, 2009.
2. Sloss Andrew N, Symes Dominic, Wright Chris, "**ARM System Developer's Guide: Designing and Optimizing**", Morgan Kaufman Publication, 2004.
3. Joseph Yiu, **"The Definitive Guide to the ARM Cortex-M3 and Cotrx-M4 Processors"**, Newnes, (Elsevier), 2014.
4. Marilyn Wolf, "**Computers as Components- Principles of Embedded Computing System Design",** Morgan Kaufman Publications, 2017.
5. Georgios Kornaros, **"Multi-Core Embedded Systems",** CRC Press, 2010.

REFERENCE BOOKS/WEBLINKS:

1. "Multicore Programming", Increased Performance through Software Multi–threading by Shameem Akhter and Jason Roberts, Intel Press, 2006.
2. James K Peckol, "Embedded Systems – A Contemporary Design Tool", John Wiley, 2008.
3. Embedded Systems- Architecture, Programming and Design, Raj Kamal, Tata McGraw-Hill, 2008.
4. www.ntpel.com

Subject Title: **ADVANCED MACHINE LEARNING AND DEEP LEARNING**		
Subject Code**: MEC104A**	No. of Credits**: 03 = 2:2:0 (L:T:P)**	No. of lecture hours per week**: 02**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

Course Learning objectives:

1. To understand the fundamental concepts of machine learning and its applications
2. To master the concepts of classification and clustering techniques.
3. To develop a deep understanding of convolutional neural networks (CNNs) and their architecture.
4. To apply deep learning techniques to large-scale datasets and real-world problems.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction and Regression:** Introduction, Types of Learning, Simple Linear Regression: Hypothesis, Cost Function, Learning Rate, Gradient Descent for Linear Regression, Multivariate Linear regression, Polynomial Linear Regression.	8	L1,L2, L3
2	**Classification and Clustering:** Naïve Bayes Classification, Decision tree Classification. **Clustering:** K-means Clustering, Association Rules. **Neural Networks:** Logistic Regression, Hypothesis, Cost Function, Gradient Descent Learning, Multiclass Classification, Back propagation of Error.	8	L1,L2, L3
3	**Convolutional Neural Networks:** The operation, Pooling, Convolution and Pooling as an infinitely strong prior, Variants of the basic functions, efficient algorithms, Random or Unsupervised Features, Neuroscientific Basis for Convolutional Networks.	8	L1,L2, L3
4	**Recurrent Neural Networks:** RNN, Bidirectional RNN, Encoder-Decoder Sequence to sequence architecture, Deep Recurrent Networks, Recursive Neural Networks, The Long Short Term Memory and other Gated RNNs, Optimization for Long Term Dependencies.	8	L1,L2, L3
5	**Applications:** Large-Scale Deep Learning, Computer Vision, Speech Recognition, Natural Language Processing, Other Applications.	8	L1,L2, L3, L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Demonstrate a comprehensive understanding of machine learning and deep learning fundamentals and their applications.
CO2	Apply various machine learning algorithms and deep learning architectures to solve complex problems.
CO3	Develop and implement machine learning models using appropriate programming languages and tools.

Course outcome and program outcome mapping

CO1	PO1,PO2,PO8,PO9,PO10

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CO2	PO1, PO2, PO3, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10

TEXT BOOKS:

1. Deep Learning - Goodfellow, Bengio and Courville
2. Fundamentals of Deep Learning – Nikhil Budama
3. Neural Networks and Deep Learning – CharuAggarwal
4. Hands-on Deep Learning Algorithms with Python – SudharsanRavichandran

REFERENCE BOOKS/WEBLINKS:

1.

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Subject Title: **MULTIMEDIA AND APPLICATIONS**		
Subject Code**: MEC104B**	No. of Credits**: 03 = 2:2:0 (L:T:P)**	No. of lecture hours per week**: 02**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Understand Digital System Verification Using Object Oriented Methods
2. Learn the System Verilog Language for Digital System Verification.
3. Create/Build Test Benches for the Design/Methodology.
4. Use Constrained Random Tests for Verification
5. Understand Concepts of Functional Coverage

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	Introduction: Multimedia information representation, Multimedia networks, Multimedia applications, Application and networking terminology, Network QoS and application QoS, Digitization principles, Text, images, audio and video.	**8**	L1,L2, L3
2	Text and image compression: Compression principles, Text compression- Run length, Huffman, LZW, Document Image compression using T2 and T3 coding, image compression- GIF, TIFF and JPEG.	**8**	L1,L2, L3
3	Audio and Video Compression: Audio compression – principles, DPCM, ADPCM, Adaptive and Linear Predictive coding, Code-Excited LPC, Perceptual coding, MPEG and Dolby coders video compression, Video compression principles.	**8**	L1,L2, L3
4	Video Compression Standards: H.261, H.263, MPEG, MPEG 1, MPEG 2, MPEG-4 and Reversible VLCs, MPEG-7 standardization process of multimedia content description, MPEG 21 multimedia framework.	**8**	L1,L2, L3
5	Multimedia Networks: Basics of Multimedia Networks, Communications and Applications: Quality of Multimedia Data Transmission, Multimedia over IP, Multimedia over ATM Networks, Transport of MPEG-4, Media on Demand (MoD).	**8**	L1,L2, L3, L4

***BTL**: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Apply the SystemVerilog concepts to verify the design.
CO2	Apply constrained random tests benches using SystemVerilog.
CO3	Appreciate Functional Coverage.

Course outcome and program outcome mapping

CO1	PO1,PO2,PO8,PO9,PO10
CO2	PO1, PO2, PO3, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10

TEXT BOOKS:

1. Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010.

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2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design- A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006.
REFERENCE BOOKS/WEBLINKS: 1.

Subject Title: **SYSTEM VERILOG PROGRAMMING**		
Subject Code**: MEC104C**	No. of Credits**: 03 = 2:2:0 (L:T:P)**	No. of lecture hours per week**: 02**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

This course will enable the students to:

1. Understand digital system verification using object oriented methods
2. Learn the System Verilog language for digital system verification.
3. Create/build test benches for the basic design/methodology.
4. Use constrained random tests for verification
5. Understand concepts of functional coverage

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Verification Guidelines**: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components. **Data Types**: Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with type def, creating user defined structures, type conversion, Enumerated types, constants and strings, Expression width.	**8**	L1,L2, L3
2	**Procedural Statements and Routines**: Procedural statements, Tasks, Functions and void functions, Task and function overview, Routine arguments, returning from a routine, Local data storage, time values. **Converting the test bench and design**: Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.	**8**	L1,L2, L3
3	**Randomization**: Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Iterative and array constraints, Random control. and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL.	**8**	L1,L2, L3
4	**Threads and Interprocess Communication**: Working with threads, Disabling threads, Interprocess communication, Events, semaphores, Mailboxes, Building a test bench with threads and Interprocess Communication.	**8**	L1,L2, L3
5	**Functional Coverage**: Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.	**8**	L1,L2, L3

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

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COURSE OUTCOMES: After studying this course, students will be able to:	
CO1	Write test benches for moderately complex digital circuits.
CO2	Use System Verilog language features to implement digital systems.
CO3	Apply constrained random tests benches using System Verilog.
CO4	Understand building of test bench for threads and interprocess Communication.
CO5	Appreciate functional coverage and coverage strategies.
Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Chris Spear, 'System Verilog for Verification – A guide to learning the Test bench language features', Springer Publications, 2nd Edition, 2010.

REFERENCE BOOKS/WEBLINKS:

1. Stuart Sutherland, Simon Davidmann, Peter Flake, ―System Verilog for Design A guide to using system verilog for Hardware design and modelling, Springer Publications, 2nd Edition, 2006.

Subject Title: **Synthesis and Optimization of Digital Circuits (SODC)**		
Subject Code: **MEC104D**	No. of Credits: **03 = 3:1:0 (L:T:P)**	No. of lecture hours per week: **03**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **40**

Course Learning Objectives:

1 Explain the need for synthesis and optimization for digital circuits

2 Describe the basic optimization techniques used in circuits design

3 Explain the advanced tools and techniques in digital systems design. These include Hardware Modelling and Compilation Techniques

4 Illustrate the concept of scheduling and resource binding for optimization.

5. Describe the logic-Level synthesis and optimization techniques for combinational and Sequential circuits.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction:** Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization. **Graphs:** Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications. **[Text1]**	**8**	L1,L2, L3
2	**Hardware Modelling:** Hardware Modelling Languages, distinctive features, structural hardware language, Behavioural hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques. [**Text1]**	**8**	L1,L2, L3, L4
3	**Two Level Combinational Logic Optimization**: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations. **Multiple Level Combinational Optimizations**: Models and transformations for combinational networks, algebraic model: Substitution, Extraction and Algebraic Kernels, Decomposition. [**Text1]**	**8**	L1,L2, L3, L4
4	**Schedule Algorithms:** A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits. **Cell Library Binding:** Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Anti-fuse based F.P.G.As), rule based library binding. [**Text1]**	**8**	L1,L2, L3, L4
5	**Sequential Circuit Optimization**: Sequential circuit optimization using state based models: State minimization, state Encoding, Other Optimization Methods and Recent Developments.[Text1]	**8**	L1,L2, L3, L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Model the MOSFET using small signal and large signal analysis
CO2	Design and analyze the CMOS analog circuits.
CO3	Calculate the frequency response of the analog circuits

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CO4	Model/synthesis/analyze the OPAMP, OSCILLATORS and PLL circuits
CO5	Understand and design the bandgap reference circuits, switched capacitor filters and chip I/O pad circuits
Course outcome and program outcome mapping	
CO1	PO2,PO5,PO12
CO2	PO2,PO3,P05
CO3	PO4,PO5
CO4	PO5,PO6
CO5	PO6,PO7

Text Book:

1. Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", Tata McGraw-Hill, 2003.

REFERENCE BOOKS/WEBLINKS:

1. Edwars M.D., Automatic Logic synthesis Techniques for Digital Systems, Macmillan New Electronic Series, 1992.
2. Sneh Saurabh, "Introduction to VLSI Design Flow", Cambridge University press, 2023.

Subject Title: **Design of VLSI systems**		
Subject Code: **MEC105A**	No. of Credits: **03 = 3:2:0 (L:T:P)**	No. of lecture hours per week: **03**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **40**

Course Learning Objectives: This course will enable the students to:

1. Give in-depth knowledge about VLSI design methodologies
2. Understand the coding concept of the VLSI design of ASIC design
3. Analyse the performance of VLSI arithmetic blocks using CAD tools
4. Design arithmetic blocks using the CMOS for ALU
5. Evaluate the circuit design/fabrication cost.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**VLSI System Design Methodology:** Structure Design, Strategy, Hierarchy, Regularity, Modularity, and Locality. System on Chip Design options: Programmable logic and structures, Programmable interconnect, programmable gate arrays, Sea of gate and gate array design, standard cell design, full custom mask design. **Chip Design Methods:** Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System	**8**	L1,L2, L3
2	**Design Capture Tools:** HDL Design, Schematic Design, Layout Design, Floor planning and Chip Composition. Design Verification Tools: Simulation Timing Verifiers, Net List Comparison Layout Extraction, Design Rule Verification. **Data Path Sub System Design:** Introduction, Addition, Subtraction, Comparators, Counters, Boolean logical operations, coding, shifters, Multiplication, Parallel Prefix computations	**8**	L1,L2, L3
3	**Array Subsystem Design:** SRAM, Special purpose RAMs, DRAM, Read only memory, Content Addressable memory, Programmable logic arrays. **Control Unit Design:** Finite State Machine (FSM) Design, Control Logic Implementation: PLA control implementation, ROM control implementation.	**8**	L1,L2, L3
4	**Special Purpose Subsystems:** Packaging, power distribution, I/O, Clock, Transconductance amplifier, follower integrated circuits. **Design Economics:** Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Person power, example	**8**	L1,L2, L3,L4
5	**VLSI System Testing & Verification:** Introduction, A walk through the Test Process, Reliability, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan **VLSI Applications: Case Study: RISC microcontroller, ATM Switch, etc.**	**8**	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Gain in-depth knowledge in VLSI design methodologies.

CO2	Develop the architectures for VLSI system design.
CO3	Design arithmetic blocks using the CMOS for ALU.
CO4	Evaluate the circuit design/fabrication cost.
CO5	Model the VLSI system using the State-Machine.
Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3
CO2	PO1,PO2,PO3,PO4
CO3	PO3,PO4,PO5,PO6
CO4	PO2,PO3,PO4,PO5
CO5	PO3,PO5,PO7

TEXT BOOKS:

1. Neil H.E. Weste, David Harris, “CMOS VLSI Design: A Circuits and System Perspectives” Addison Wesley - Pearson Education, 3rd Edition, 2004.

REFERENCE BOOKS/WEBLINKS:

1. Wayne, Wolf, “Modern VLSI Design: System on Silicon” Prentice Hall PTR/Pearson Education, Second Edition, 1998.
2. Douglas A Pucknell & Kamran Eshragian , “Basic VLSI Design” PHI 3rd Edition (original Edition – 1994).

Subject Title**: Pattern Recognition & Machine Learning**		
Subject Code**: MEC105B**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. To understand the model selection and different types of variables.
2. To study Supervised Learning Linear Regression Models.
3. To learn the various types of Supervised Learning Kernels.
4. To get familiar with Unsupervised Learning.
5. To learn the Probabilistic Graphical Models.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**Introduction:** Probability Theory, Model Selection, The Curse of Dimensionality, Decision Theory, Information **Theory Distributions:** Binary and Multinomial Variables, The Gaussian Distribution, The Exponential Family, Nonparametric Methods.	**8**	L1,L2, L3,L4
2	**Supervised Learning Linear Regression Models:** Linear Basis Function Models, The Bias-Variance Decomposition, Bayesian Linear Regression, Bayesian Model Comparison Classification & Linear Discriminant Analysis: Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Mode	**8**	L1,L2, L3,L4
3	**Supervised Learning Kernels:** Dual Representations, Constructing Kernels, Radial Basis Function Network, Gaussian Processes Support Vector Machines: Maximum Margin Classifiers, Relevance Vector Machines Neural Networks: Feed-forward Network, Network Training, Error Back propagation	**8**	L1,L2, L3,L4
4	**Unsupervised Learning:** Mixture Models: K-means Clustering, Mixtures of Gaussians, Maximum likelihood, EM for Gaussian mixtures, Alternative View of EM**.** **Dimensionality Reduction:** Principal Component Analysis, Factor/Component Analysis, Probabilistic PCA, Kernel PCA, Nonlinear Latent Variable Models	**8**	L1,L2, L3,L4
5	**Probabilistic Graphical Models:** Bayesian Networks, Conditional Independence, Markov Random Fields, Inference in Graphical Models, Markov Model, Hidden Markov Models	**8**	L1,L2, L3,L4

***BTL**: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Identify areas where Pattern Recognition and Machine Learning can offer a solution.
CO2	Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.
CO3	Describe and model data.
CO4	Solve problems in Regression and Classification.
CO5	Discuss main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems.

Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. "**Pattern Recognition and Machine Learning**", Christopher Bishop Springer 2006.

REFERENCE BOOKS/WEBLINKS:

1. Konstantinos Koutroumbas, Sergios Theodoridis, "**Pattern recognition**", Fourth Edition, Academic Press, 2009.
2. Tom M. Mitchell "**Machine Learning: An Artificial Intelligence Approach**", First Edition, Mc Graw Hill, Reprint 2017.

Subject Title: **ASIC DESIGN**		
Subject Code: **MEC105C**	No. of Credits: **03 = 2:2:0 (L:T:P)**	No. of lecture hours per week: **02**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **40**

Course Learning Objectives: This course will enable the students to:

1. Explain ASIC methodologies and programmable logic cells to implement a function on IC.
2. Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.
3. Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs.
4. Design CAD algorithms and explain how these concepts interact in ASIC design

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction To ASICs**, Full Custom, Semi-Custom and Programmable ASICS, ASIC Design Flow, ASIC Cell Libraries. **CMOS Logic:** Datapath Logic Cells: Datapath Elements, Adders: Carry Skip, Carry Bypass, Carry Save, Carry Select, Conditional Sum, Multiplier (Booth Encoding), Data Path Operators, I/O Cells.**[TEXT1]**	**8**	L1,L2, L3
2	**ASIC Library Design:** Logical Effort: Predicting Delay, Logical Area and Logical Efficiency, Logical Paths, Multi Stage Cells, Optimum Delay and Number Of Stages. **Programmable ASIC Logic Cells:** MUX as Boolean Function Generators, Actel ACT: ACT 1, ACT 2 And ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX.**[TEXT1]**	**8**	L1,L2, L3
3	**Programmable ASIC I/O Cells:** Xilinx and Altera I/O Block. **Low-Level Design Entry:** Schematic Entry: Hierarchical Design, Netlist Screener. **ASIC Construction:** Physical Design, CAD Tools. **Partitioning:** Goals and Objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead Algorithms. **[TEXT1]**	**8**	L1,L2, L3
4	**Floor Planning and Placement:** Goals and Objectives, Floor Planning Tools, Channel Definition, I/O And Power Planning and Clock Planning. **Placement:** Goals and Objectives, Min-Cut Placement Algorithm, Iterative Placement Improvement, Physical Design Flow. **[TEXT1]**	**8**	L1,L2, L3
5	**Routing:** Global Routing: Goals and Objectives, Global Routing Methods, Back-Annotation. Detailed Routing: Goals and Objectives, Measurement of Channel Density, Left-Edge and Area-Routing Algorithms. Special Routing, Circuit Extraction and DRC. **[TEXT1]**	**8**	L1,L2, L3

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort and FPGA architectures.
CO2	Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow.
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay.
CO4	Understand and identify different Programmable ASIC Logic Cells.
CO5	Create floor plan including partition and routing with the use of CAD algorithms.
Course outcome and program outcome mapping	
CO1	PO1,PO2
CO2	PO2, PO3,PO4,PO5
CO3	PO2,PO3,PO4,PO5
CO4	PO2,PO3, PO4,PO5
CO5	PO3,PO4, PO5,PO6

TEXT BOOKS:

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits" Addison Wesley Professional; 2005.

REFERENCE BOOKS/WEBLINKS:

1. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd edition, Addison Wesley/ Pearson education, 2011.
2. VikramArkalgudChandrasetty,"VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011, ISBN: 978-1-4614-1119-2.
3. RakeshChadha, Bhasker J., "An ASIC Low Power Primer", Springer, ISBN: 978-1-4614-4270-7.

Subject Title: **Digital Circuits & Logic Design**		
Subject Code: **MEC105D**	No. of Credits: **03 = 2:2:0 (L:T:P)**	No. of lecture hours per week: **02**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **40**

Course Learning Objectives: This course will enable the students to:

1. • Understand the concepts of sequential machines
2. • Design Sequential Machines/Circuits
3. • Analyze the faults in the design of circuits
4. • Apply fault detection experiments to sequential circuits

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Threshold Logic**: Introductory Concepts, Synthesis of Threshold Networks **Capabilities, Minimization, and Transformation of Sequential Machines:** The Finite- State Model, Further Definitions, Capabilities.	8	L1,L2, L3
2	**Fault detection by path sensitizing**: Detection of multiple faults, Failure-Tolerant Design, Quadded Logic, Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits.	8	L1,L2, L3
3	**Fault-location experiments**: Boolean Differences, Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.	8	L1,L2, L3
4	**Structure of Sequential Machines**: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, decompositions, Synthesis of Multiple Machines.	8	L1,L2, L3
5	**State Identifications and Fault-Detection Experiments**: Homing Experiments, Distinguishing Experiments, Machine Identification, Fault Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection.	8	L1,L2, L3, L4

*BTL: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Able to understand the concepts of sequential machines
CO2	Able to understand the Sequential Machines/Circuits
CO3	Able to understand the structure of sequential machines
CO4	Able to analyse the faults in the design of circuits.
CO5	Able to analyse fault detection experiments to sequential circuits.

Course outcome and program outcome mapping

CO1	PO1,PO2,PO8,PO9,PO10
CO2	PO1, PO2, PO3, PO8,PO9,PO10

CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Switching and Finite Automata Theory', Zvi Kohavi, TMH, ISBN: 978_0_07_099387_7, 2nd Edition, 2008.

REFERENCE BOOKS/WEBLINKS:

1. 'Digital Circuits and logic Design', Charles Roth Jr., Cengage Learning, 7thedition, 2014.
2. 'Fault Tolerant and Fault Testable Hardware Design', Parag K Lala, Prentice Hall Inc. 1985.
3. 'Introductory Theory of Computer', E. V. Krishnamurthy, Macmillan Press Ltd, 1983
4. 'Theory of computer science – Automata, Languages and Computation', Mishra & Chandrasekaran, 2ndEdition, PHI, 2004.
5. https://nptel.ac.in/

Subject Title: **VLSI Design and Embedded Systems Lab-I**		
Subject Code**: MECL106**	No. of Credits**: 02 = 1:0:2 (L:T:P)**	No. of lecture hours per week**: 02**
Exam Duration**: 3 Hours**	CIE + SEE **= 50+50=100**	Total No. of lecture hours**: 36**

Course Learning Objectives: This course will enable the students to:

1. Design and implementation of basic digital blocks using VERILOG and FPGA Kits.
2. To learn the programming skills in data flow, structural, and behavioral
3. Design of states machines
4. Analyze LPC 1768 MCU
5. Develop assembly and Embedded C programming of ARM Cortex-M3 Processor and Develop 32-bit microcontroller based Embedded system applications

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
	PART A		
	VLSI FRONT END DESIGN PROGRAMS:		
1	Write a Verilog code for the following 8 bit adder circuits and implement using chip-scope techniques. 1. Carry Ripple Adder 2. Carry Look Ahead adder 3. Carry Skip Adder 4. BCD Adder & Subtractor	**3**	L3,L4
2	Write a Verilog code for the following 8 bit multiplier circuits and implement using chip-scope techniques. 1. Array Multiplication (Signed and Unsigned) 2. Booth Multiplication (Radix-4)	**3**	L3,L4
3	Write a Verilog code for the following 8/4 circuits and implement using chip-scope techniques. 1. Magnitude Comparator 2. LFSR 3. Parity Generator 4. Universal Shift Register	**3**	L3,L4
4	Write Verilog Code for 3-bit Arbitary Counter to generate 0,1,2,3,6,5,7 and repeats.	**3**	L3, L4
5	Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.	**3**	L3, L4
6	Design a FIFO and LIFO buffers in Verilog and Verify its Operation.	**3**	L3,L4
7	Design a coin operated public Telephone unit using Mealy FSM model with specified operations.	**3**	L3,L4
	PART-B		
	ARM Cortex M3 Programs:		
1	Write an Assembly language program to link multiple object files and link them together.	**3**	L3,L4
2	Write Embedded C program to read on-chip ADC value and display it on terminal of LPC 1768.	**3**	L3,L4
3	Write Embedded C program to interface LED and Relay to LPC 1768 MCU.	**3**	L1,L2,

			L3,L4
4	Write Embedded C Program to interface RTC to LPC1768.	**3**	L1,L2, L3,L4
5	Write Embedded C program to design a Stopwatch using interrupts.	**3**	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- The internal assessment will be based on Record, Conduction, Question and Answer session.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Design digital circuits for specific applications.
CO2	Verify the digital circuits using chip scope techniques.
CO3	Develop a Verilog code based on states machines.
CO4	Analyze the architecture of ARM Cortex-M3.
CO5	Create different assembly and Embedded C programs.
CO6	Design and testing programs for different embedded applications using LPC1768.

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4
CO4	PO2,PO6
CO5	PO2, PO3, PO4, PO5, PO12
CO6	PO2, PO3, PO4, PO5,PO12

TEXT BOOKS:

1. J. Bhaskar, “A Verilog HDL Primer”, Third Edition, BS publications, Reprint 2023.
2. Samir Palanithkar, “Verilog HDL”, Second Edition, 2012.
3. Joseph Yiu, “The Definitive Guide to the ARM CORTEX-M3”, Second Edition, Newnes, 2008.

REFERENCE BOOKS/WEBLINKS:

1. Byeong Kil Lee, Charles H Roth, and Lizy Kurian John, “*Digital Systems Design Using Verilog*”, First Edition, Boston, MA: Cengage Learning, 2016.

Course Title: RESEARCH METHODOLOGY AND IPR	
Course Code: **MRMI107**	ONLINE
Credits: PP/NP	
MRMI16-Research Methodology and IPR- None Credit Mandatory Course (NCMC) if students have not studied this course in their undergraduate program then he /she has to take this course at http://online.vtu.ac.in and to qualify for this course is compulsory before completion of the minimum duration of the program (Two years), however, this course will not be considered for vertical progression.	

BOS Chairman Dean(Academics) Principal

<table>
<tr><td rowspan="3"></td><td colspan="3">SUBJECT TITLE: CAREER DEVELOPMENT SKILLS – I (AY: 2024-25)</td></tr>
<tr><td>Subject Code:MCDN108</td><td>NonCredit Mandatory Course (NCMC)</td><td>No of lecture hours per week: 02</td></tr>
<tr><td colspan="2">Evaluation Method: CIE + Assignment +Group Activity (Max: 50 Marks)</td><td>Total No. of lecture hours: 26</td></tr>
</table>

Course objectives:

1. The lessons under this course are designed to enable the students to plan their career on correct measures and motivate them to set their goals on prior basis.
2. This course aims to develop the personality skills of the students and teach them to lead a corporate discipline nurture. It also helps them to get groomed with professional ethics.
3. This course complies with the overcoming ability of students dealt in stress and it also teaches the punctuality and time managing.
4. This course will help students make inferences and predictions about spoken, writing & listening discourse.
5. To prepare for Verbal Ability, stick to the rule of – concepts first and practice later. Study English grammar to understand the concepts. Then practice several sample questions of different kinds to gain confidence, speed and accuracy.

<table>
<tr><th rowspan="2">Unit No.</th><th rowspan="2">Syllabus content</th><th>No. of hours</th></tr>
<tr><th>Theory</th></tr>
<tr><td>1</td><td>Number System: Number system, Power cycle, Remainder cycle, Factors, Multiples, HCF and LCM, Trailing Zeroes
Profit and Loss: Concept and Problem-solving technic in Profit and Loss
Ratio, Proportion and Partnership: Concept and Problem-solving technic in Ratio and Proportion, Partnership
Percentage: Percentages as Fractions and Decimals, Percentage Increase / Decrease</td><td>6 hours</td></tr>
<tr><td>2</td><td>Alligation and Mixture: Basic Concept of Alligation and Mixture, concept of mixture containing more than two Ingredients.
Simple Interest and compound interest: Concept and Problem-solving technic in simple interest and compound interest.
Probability: Probability, Total Probability, Finding Probability without using Combination, Finding Probability using Pascal Triangle
Problems on Average: Concept of Average, Weighted Average.
Permutation and Combination: Fundamental Counting Principle, Permutation and Combination, Computation of Permutation, Circular Permutations, Computation of Combination</td><td>6 hours</td></tr>
<tr><td>3</td><td>Time, Speed & Distance: Basics of time, speed and distance, Relative speed, Problems based on trains, Problems based on boats and streams, Problems based on races.
Time and Work: Work with different efficiencies, Alternate day work, Pipes and cisterns, Work equivalence, Division of wage, Leaving the work concept with example
Logarithm, Progression, Geometry: Concept and Problem-solving technic in Logarithm and Progression. Basics of Geometry of 2 and 3 dimensional with formula, concepts and shortcut method.</td><td>6 hours</td></tr>
<tr><td>4</td><td>Verbal Ability I – Reading Comprehension: Types and Tackling Strategies, understanding meaning of a text, Drawing Connections, Summarizing and Synthesizing, Building Vocabulary, Speed Reading Strategies</td><td>4 hours</td></tr>
<tr><td></td><td>Verbal Ability IV – Verbal Reasoning and Verbal Analogy: Verbal Reasoning, Verbal Classification, Logical sequence of word</td><td></td></tr>
</table>

BOS Chairman Dean(Academics) Principal

5	**Resume writing and Profiling:** What is resume, it’s importance and differences between CV, Resume and Biodata. Latest format of resumes. **Time Management, Leadership skills**: Scheduling, Prioritizing the work and preparing priority matrix. The qualities of leaders and types of leadership skills.	**4 hours**
	Course Outcomes: **CO1:** The students will be able to learn about the overview of their goals and also gets to know diversities in the field of their career planning. **CO2:** The student will develop and improve their personal and professional effectiveness. By the end of this course, students will have deployed themselves about the corporate culture. **CO3:** At the completion of this course, students will develop the self-confidence and emerge as the confident person. **CO4:** After the completion of this course students will understand the stress, time and emotional management. Also, they will learn about the overcoming the fear and uncomfortable situations such as public speaking. **CO5:** After the completion of this course, students will gain knowledge about the assertiveness of Listening, Reading, Writing & Interpersonal segments.	
	REFERENCE BOOKS. 1. Soft skills for Managers by Dr. T. KALYANA CHAKRAVATHI 2. Personal Development and Soft Skills by BARUN K MITRA, Oxford Higher Education 3. The Emotionally Intelligent Workplace by DANIEL GOLEMAN. 4. Communication skills and soft skills an integrated approach by E. SURESH KUMAR, P. SREEHARI, J SAVITHRI. 5. Top Talking in English (international communication skills) by CHARLES T. RAJENDRA 6. Soft skills by RAJ LAKSHMI SURYAVANSHI, Gurucool Publishing	

II Semester Syllabus

(2025 Batch)

Subject Title: **Analog IC Design**		
Subject Code: **MEC201**	No. of Credits: **03 = 3:1:0 (L:T:P)**	No. of lecture hours per week: **03**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **40**

Course Learning Objectives: This course will enable the students to:

1. Understand the MOSFET operations in detail.
2. Understand the small signal circuit concepts of MOSFET.
3. Analysis of analog circuits parameters based on the small signal circuits.
4. Applications OP-Amp in an analog building blocks.
5. Design and develop ADC and DAC using different architectures.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Basic MOS Device Physics:** General considerations, MOS I/V Characteristics, second order effects, MOS device models. **Single stage Amplifier:** CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models. **[Text 1]**	8	L1,L2, L3
2	**Differential Amplifiers:** Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell. **Passive and active Current mirrors:** Basic current mirrors, Cascade mirrors, active current mirrors. **[Text 1]**	8	L1,L2, L3, L4
3	**Frequency response of CS stage:** source follower, Common gate stage, Cascade stage and Difference pair. Noise in CS stage, C- G stage, source follower, cascade stage, differential pair. **[Text 2]**	8	L1,L2, L3, L4
4	**Operational Amplifiers:** One Stage OP-Amp. Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, PSRR. Compensation of 2stage OP-Amp, Other compensation techniques. **[Text 2]** **Oscillators:** Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. **PLL:** Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.	8	L1,L2, L3, L4
5	**Band gap References** and Switched capacitor filters. **[Text1]** **Chip Input and Output (I/O) Circuits:** Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and its Prevention. [**TEXT 1**]	8	L1,L2, L3, L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Model the MOSFET using small signal and large signal analysis
CO2	Design and analyze the CMOS analog circuits.
CO3	Calculate the frequency response of the analog circuits
CO4	Model/synthesis/analyze the OPAMP, OSCILLATORS and PLL circuits
CO5	Understand and design the bandgap reference circuits, switched capacitor filters and chip I/O pad circuits

Course outcome and program outcome mapping

CO1	PO1,PO2,PO8,PO9,PO10
CO2	PO1, PO2, PO3, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Behzad Razavi, **Design of Analog CMOS Integrated Circuits**", TMH, 2007.
2. R. Jacob Baker, "**CMOS Circuit Design, Layout, and Simulation**", Second Edition, Publisher: Wiley-IEEE Press, 1997.
3. Phillip E. Allen, Douglas R. Holberg, **CMOS Analog Circuit Design**, Second Edition, Oxford University Press, 2002.

REFERENCE BOOKS/WEBLINKS:

1. R. Jacob Baker, "**CMOS Circuit Design, Layout, and Simulation**", Third Edition, Publisher: Wiley-IEEE Press, 2010.
2. Philip E. Allen, Douglas R. Holberg, "**CMOS Analog Circuit Design**", Oxford University Press, Third Edition, 2013.
3. nptel.ac.in/courses/117106093/.

Subject Title: **Embedded OS**		
Subject Code**: MEC202**	No. of Credits**: 04 = 3:0:2 (L:T:P)**	No. of lecture hours per week**: 04**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 50**

Course Learning Objectives

1. Introduce the fundamental concepts of the OS and real time embedded systems.
2. Apply concepts relating to embedded operating systems such as scheduling techniques, Dynamic priority policies.
3. Describe concepts related to multi resource services like blocking, Deadlock, live lock & soft real-time services.
4. Understand the embedded OS related concepts.
5. Expose to different available RTOS through their case studies

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Real-Time Systems and Resources:** Brief history of Real Time Systems, A brief history of Embedded Systems. Resource Analysis, Real-Time Service Utility, scheduling classes, Scheduler concepts, OS basics, Types of OS, OS in an embedded device, State transition diagram. (Text 1)	8	L1,L2,L3
2	**Processing with Real Time Scheduling:** Introduction, Pre-emptive Fixed Priority Scheduling Policies with timing diagrams, Problems and issues, Feasibility, Rate Monotonic least upper bound (No derivation), Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies. (Text 1)	8	L1,L2 ,L3
3	**I/O Resources**: Worst case execution time, Execution efficiency, I/O Architecture. **Memory:** Physical hierarchy, Shared Memory, ECC Memory. **Multi-resource Services:** Blocking, Deadlock and livelock, Priority inversion. **Soft real-time services:** Missed deadline, QoS. (Text 1)	8	L1,L 2, L3
4	**Embedded OS Concepts:** Tasks, Process and Threads, Process and thread creations, Simple Programs, Semaphores, Mutex, Mailboxes, Message queues, Pipes, Multithreading, Programs related to semaphores, message queue, Examples of Embedded OS. (Text 2)	8	L1,L 2, L3
5	**Case Studies:** FreeRTOS, RTLinux, VxWorks, Micro C/OS-II, Embedded Linux, Comparison of available RTOS, Selection criteria of RTOS for an application. (Text 1)	8	L2, L3, L4.

*BTL: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Discuss the fundamentals of various real time services, real time service utilities, and real time embedded system.
CO2	Apply priority based static and dynamic real time scheduling techniques for the given real time embedded system specifications.
CO3	Analyze deadlock conditions, shared memory problem, priority inversion, missed deadlines and QoS of real time embedded systems.

	Develop the programs for multithreaded applications using different embedded OS concepts. Choose the appropriate available OS to improve the real time embedded system performance.
CO4	Realize the various ALU sub-system blocks using behavioural methodology.
CO5	Implement digital circuits using Field Programmable Gate Arrays.
Course outcome and program outcome mapping	
CO1	PO1, PO2, PO6, PO12
CO2	PO1, PO2, PO4, PO5, PO12
CO3	PO1, PO2, PO6, PO12
CO4	PO1, PO2, PO5, PO6, PO12 PO1, PO2, PO4, PO5, PO6, PO12
CO5	PO5, PO6

TEXT BOOKS:

1. "**Real-Time Embedded Components and Systems",** Sam Siewert, Cengage Learning India Edition, 2007.
2. "**Embedded/Real-time Systems**", Dr K.V.K.K. Prasad, Dreamtech press, 2017.

REFERENCE BOOKS/WEBLINKS:

1. James W S Liu, "**Real Time System**", Pearson education, 2008.
2. Qing Li, "**Real Time Concepts for Embedded Systems**", Elsevier, 2011.
3. Rajkamal, "Embedded Systems- Architecture, Programming, and Design", TMH, 2007.
4. W. Richard Stevens, Stephan A. Rago, "Advanced UNIX Programming", 2nd Edition, Pearson, 2006.
5. Dr. Craig Hollabaugh, "Embedded Linux: Hardware, Software and Interfacing", 1st Edition, Pearson, 2008.
6. nptel.ac.in/courses

1. http://www.FreeRTOS.org

Session No	Practical Session	No of Hours	Blooms Taxonomy Level
1	Create periodic, aperiodic and sporadic tasks for different attributes, assign priorities, modify priorities, schedule using RM/EDF/LLF/other algorithm in any online scheduler and analyze the results with respect to CPU utilization and turnaround time.	**2**	L3, L4.
2	Develop and execute a program using any thread library to create the number of thread specified by the user, each thread independently generates a random integer as an upper limit and then computes and prints the number of primes less than or equal to that upper limit, along with that upper limit.	**2**	L3, L4.
3	Create multitasking program to demonstrate task synchronization.	**2**	L3,L4
4	Create multitasking program to demonstrate IPC using mailbox.	**2**	L3,L4
5	Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.	**2**	L3, L4.

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of IPCC

1. Two Tests each of 20 Marks
2. Two assignments each of 10 Marks / One Skill Development Activity of 20 Marks
3. Total Marks of two tests and two assignments / One Skill Development Activity added will be CIE for 60 Marks, marks scored will be proportionally scaled down to 30 Marks.

CIE for the practical component of IPCC

1. On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The 15 Marks are for conducting the experiment and preparation of the laboratory record, the other 05 Marks shall be for the test conducted at the end of the semester.
2. The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments 'write-ups are added and scaled down to15 marks.
3. The laboratory test at the end /after completion of all the experiments shall be conducted for 50 Marks and scaled down to 05 Marks. Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory Component of IPCC for 20marks.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03hours)

1. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50marks.
2. The question paper will have ten questions. Each question is set for 20marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
4. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

1. The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20marks.
2. SEE will be conducted for 100marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of50% of maximum marks of the course(CIE+SEE)

Subject Title: **VLSI Design Verification and Testing**		
Subject Code**: MEC203**	No. of Credits**: 03 = 2:2:0 (L:T:P)**	No. of lecture hours per week**: 02**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Learn the basics of testing and verification and the role of testing and verification in VLSI design.
2. Able to identify the types of faults and apply the appropriate fault model to detect them.
3. Study of various fault diagnosing techniques and test generation methods.
4. Study of verification tools and simulators.
5. Able to understand the levels of verification and applying the verifying strategies at various levels of VLSI design.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction to Testing:** Introduction**,** Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing. **Fault Modelling**: Defects errors and faults, Functional versus Structural testing, Levels of fault models, Single stuck-at fault-Fault equivalence, Equivalence of Single Stuck-at Faults, Fault collapsing, Fault dominance and Check point theorem. **Logic and Fault simulation:** Simulation for design verification, simulation for test evaluation, Modelling Circuits for simulation, Algorithms for true value simulation: compiled code simulation, Event driven Simulation, Algorithms for Fault simulation: Serial, Parallel, Deductive, Concurrent fault simulation, Roth's TEST-DETECT algorithm, Differential fault simulation. **[TEXT 2]**	**8**	L1,L2, L3
2	**Test Generation for Combinational logic circuits**: Fault Diagnosis of Digital Systems, Test Generation Techniques for Combinational Logic Circuits, Detection of Multiple Faults in Combinational Logic Circuits. **Test generation for Sequential circuits**: Testing of sequential circuits as Iterative combinational circuits, state table verification, random testing, transition count testing, signature analysis. **[TEXT 1]**	**8**	L1,L2, L3,L4
3	**Design of Testable Sequential Circuits:** What is testability, Controllability and Observability, Design of testable combinational logic Circuits, testable design of sequential circuits, The Scan-Path Technique for Testable Sequential Circuits, Level-Sensitive Scan Design, Random Access Scan Technique, Built-in Test, Design for autonomous self-test, designing testability into logic boards. **[TEXT 1]**	**8**	L1,L2, L3,L4
4	**What is verification**: What is a test bench, The importance of verification, Reconvergence model, what is being verified: Formal verification, Equivalence checking, Model checking, Functional verification, test bench generation, Functional verification approaches: Black-Box verification, White-box verification, Grey-box verification, Testing versus verification: Scan-based testing, design for verification. **Verification Tools:** Linting tools: Limitations of linting tools, linting verilog source code, linting VHDL source code, Code reviews, Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, **[TEXT3]**	**8**	L1,L2, L3
5	**The Verification Plan:** The role of verification plan: specifying the verification plan, defining the first success, Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, Verification strategies: verifying strategies, verifying the response,	**8**	L1,L2, L3

	Random verification, From specifications to features: Component-level features, system-level features, error types to look for, From features to testcases: prioritize, group into testcases, design for verification, from testcases to testbenches: verifying testbenches. **[TEXT3]**		

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Understand the need for testing, testing philosophy; Remember, Apply and Analyse various fault models and different types of simulation techniques.
CO2	Contemplate on various test generation methods applicable to both combinational and sequential logic circuits.
CO3	Understand and Exploit the features of testable design, Scan based techniques, Built-in Test and Autonomous Self-test strategies for today's VLSI design testing.
CO4	Remember and Understand the need for verification, compare it with testing and explain model check, verification approaches and verification tools and simulators.
CO5	Understand and Perform extensive study on verification plan from specification to first time success, random verification and explain about levels of verification and verification strategies.

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4,PO5
CO4	PO7,PO8
CO5	PO3,PO4

TEXT BOOKS:

1. P K Lala**," Fault Tolerant & Fault Testable Hardware Design", B S publications, 2014.**
2. M L Bushnell and V D Agrawal, "**Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits**", First Edition, Kluwar Academic Publishers, New York, 2002.
3. Janick Bergeron, "**Writing Test Benches: Functional Verification of HDL Models**", Second Edition, Kluwar Academic Publishers, 2003.

REFERENCE BOOKS/WEBLINKS:

1. Abramovici M, Breuer M A and Friedman A D, "Digital Systems Testing and Testable Design", Wiley, 1994.
2. P K Lala, "Digital Circuit Testing and Testability", First Edition, Academic Press, 1997.
3. Bhasker J, Chadha and Rakesh, "Static Timing Analysis for Nanometer Designs-A Practical Approach", First Edition, Springer Publications, 2009.
4. Wang, Wu and Wen, "VLSI Test Principles and Architectures", Morgan Kaufmann publishers, 2006.
5. Neil Weste and K. Eshrangian, "Principles of CMOS VLSI Design: A System Perspective," 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
6. https://nptel.ac.in/courses/106103116

Subject Title: **Low Power VLSI Design**		
Subject Code**: MEC204**	No. of Credits**: 04 = 3:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 04**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 52**

Course Learning Objectives: This course will enable the students to:

6. Understand the basic knowledge of power dissipation in CMOS devices and analyse the Technology Impact on Low Power.
7. Study the Probabilistic power analysis and Simulation Power analysis.
8. Discuss the concepts of Low power Clock Distribution.
9. Illustrate the concepts of Low power Architecture & Systems
10. Discuss the various Algorithm & Architectural Level Methodologies.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction:** Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **Simulation power analysis:** SPICE circuit simulation gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. **TEXT-1**	**8**	L1,L2, L3
2	**Probabilistic power analysis**: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **Low Power Design Circuit level**: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. **TEXT-1 and TEXT-2**	**8**	L1,L2, L3
3	**Logic level:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. **TEXT-1 and TEXT-2**	**8**	L1,L2, L3
4	**Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design. **TEXT-1 and TEXT-2**	**8**	L1,L2, L3
5	**Algorithm & Architectural Level Methodologies:** Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis. **TEXT-1 and TEXT-2**	**8**	L1,L2, L3

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Analyze the Algorithm & Architectural Level Methodologies.
CO2	Apply the Different simulation tools for Power analysis.

CO3	Analyze Power & performance management with the concepts of gate level logic simulation and various concepts of Gate reorganization.
CO4	Discuss Power dissipation in clock distribution and the Sources of power dissipation on Digital Integrated circuits.
CO5	Illustrate the data correlation analysis in DSP systems.

Course outcome and program outcome mapping

CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Kaushik Roy, Sharat Prasad, "**Low-Power CMOS VLSI Circuit Design**" Wiley, 2000
2. Gary K. Yeap, "**Practical Low Power Digital VLSI Design**", KAP, 2002
3. Jan M. Rabaey , Massoud Pedram, "**Low Power Design Methodologies**" The Springer International Series in Engineering and Computer Science.

REFERENCE BOOKS/WEBLINKS:

1. A.P. Chandrasekaran and R.W. Broadersen, "**Low power digital CMOS design**", Kluwer Academic, 1995.
2. A Bellamour and M I Elmasri, "**Low power VLSI CMOS circuit design**", Kluwer Academic, 1995.
3. www.ntpel.com.

Subject Title: **Digital IC design**		
Subject Code**: MEC205A**	No. of Credits**: 03 = 3:0:0:0 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Learn circuit-oriented approach towards digital design
2. Illustrate the impact of interconnect wiring on the functionality and performance of a digital gate.
3. Infer different approaches to digital timing and clocking circuits
4. Understand the impact of clock skew on the behaviour of digital synchronous circuits
5. Explain the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Implementation Strategies For Digital ICS**: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future.	**8**	L1,L2, L3
2	**Coping With Interconnect**: Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability-Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques, Reduced-Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip.	**8**	L1,L2, L3,L4
3	**Timing Issues In Digital Circuits**: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design— An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Latch-Based Clocking, SelfTimed Circuit Design, Self-Timed Logic - An Asynchronous Technique, Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self-Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL.	**8**	L1,L2, L3,L4
4	**Designing Memory and Array Structures**: Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Non-volatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References, Drivers/Buffers, Timing and Control.	**8**	L1,L2, L3, L4
5	**Designing Memory and Array Structures:** Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Data retention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4 Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor	**8**	L1,L2, L3, L4

	Memory Trends and Evolutions.		

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.
CO2	Use the approaches to minimize the impact of interconnect parasitic on performance, power dissipation and circuit reliability
CO3	Impose the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.
CO4	Infer the reliability of the memory
CO5	Solve application specific integrated circuit problems

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4,PO5
CO4	PO7,PO8
CO5	PO3,PO4

TEXT BOOKS:

1. Jan M Rabey, Anantha Chandrakasan, BorivojeNikolic,, **Digital Integrated Circuits-A Design Perspective**, PHI, 2nd Edition, 2003.
2. M. Smith, **Application Specific Integrated circuits**, Addison Wesley, 1997.

REFERENCE BOOKS/WEBLINKS:

1. H. Veendrick, **—MOS IC‘s: From Basics to ASICs**, Wiley-VCH, 1992.

Subject Title: **CMOS RF CIRCUIT DESIGN**		
Subject Code**: MEC205B**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Learn basic concepts in RF and microwave design emphasizing the effects of nonlinearity and noise.
2. Able to appreciate communication system, multiple access and wireless standards necessary for RF circuit design.
3. Able to deal with transceiver architecture, various receiver and transmitter designs, their merits and demerits
4. Understand the design of RF building blocks such as Low Noise Amplifiers and Mixers.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction to RF Design and Wireless Technology:** **Basic concepts in RF design (I):** General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range.**[Text 1]**	8	L1,L2, L3,L4
2	**Basic concepts in RF design (II**): Passive impedancetransformation, scattering parameters, analysis of nonlineardynamic systems.**[Text 1]**	8	L1,L2, L3,L4
3	**Communication Concepts:** General concepts, analog modulation, digital modulation, spectral re-growth, Mobile RF communications, Multiple access techniques, Wireless standards.**[Text 1]**	8	L1,L2, L3,L4
4	**Transceiver Architecture (I):** General considerations, Receiver architecture.**[Text 1]**	8	L1,L2, L3,L4
5	**Transceiver Architecture (II):** Transmitter architectures **Low Noise Amplifiers:** LNA topologies: common-source stage withinductive load, common-source stage with resistive feedback. **Mixers:** General considerations, passive down conversion mixers. **[Text 1]**	8	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Analyze the effect of nonlinearity and noise in RF and microwave design.
CO2	Exemplify the approaches taken in actual RF products.
CO3	Minimize the number of off-chip components required to design mixers and Low-Noise Amplifiers.
CO4	Explain various receivers and transmitter topologies with their merits and drawbacks.
CO5	Demonstrate how the system requirements define the parameters of the circuits and how the performance of each circuit impacts that of the overall transceiver.

Course outcome and program outcome mapping

CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. B. Razavi, "**RF Microelectronics**," PHI, Second edition, 2004.

REFERENCE BOOKS/WEBLINKS:

1. R. Jacob Baker, H.W. Li, D.E. Boyce "CMOS Circuit Design, layout and Simulation", PHI 1998.
2. Thomas H. Lee "Design of CMOS RF Integrated Circuits" Cambridge University press 1998.
3. Y.P. Tsividis, "Mixed Analog and Digital Devices and Technology", TMH 1996.
4. www.ntpel.com.

Subject Title: **Multicore Architectures**		
Subject Code**: MEC205C**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Provide the knowledge of Multi– core architecture and system overview of threading.
2. Cover fundamental concepts of Parallel programming and its constructs.
3. Describe in detail the concepts of Threading APIs.
4. Get exposure to different concepts of OpenMP.
5. Provide Solutions to common parallel programming problems.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**Introduction to Multi– core Architecture:** Motivation for Concurrency in software, Parallel Computing Platforms, Parallel Computing in Microprocessors, Differentiating Multi–core Architectures from Hyper–Threading Technology, Multithreading on Single–Core versus Multi–Core Platforms Understanding Performance, Amdahl's Law, Growing Returns: Gustafson's Law. **System Overview of Threading:** Defining Threads, System View of Threads, Threading above the Operating System, Threads inside the OS, Threads inside the Hardware, What Happens When a Thread Is Created, Application Programming Models and Threading, Virtual Environment: VMs and Platforms, Runtime Virtualization, System Virtualization. (Text: Chapters 1 and 2)	**8**	L1,L2, L3
2	**Fundamental Concepts of Parallel Programming:** Designing for Threads, Task Decomposition, Data Decomposition, Data Flow Decomposition, Implications of Different Decompositions, and Challenges You will Face, Parallel Programming Patterns. **A Motivating Problem:** Error Diffusion, Analysis of the Error Diffusion Algorithm. **An Alternate Approach:** Parallel Error Diffusion, Other Alternatives. **Threading and Parallel Programming Constructs:** Synchronization, Critical Sections, Deadlock, Synchronization Primitives, Semaphores, Locks, Condition Variables, Messages, Flow Control–based Concepts, Fence, Barrier, Implementation dependent Threading Features. (Text: Chapters 3 and 4)	**8**	L1,L2, L3
3	**Threading APIs:** Threading APls for Microsoft Windows, Win32/MFC Thread APls, Threading APls for Microsoft Dot–NET Framework, Creating Threads, Managing Threads, Thread Pools, Thread Synchronization, POSIX Threads, Creating Threads, Managing Threads, Thread Synchronization, Signaling, Compilation and Linking. (Text: Chapter 5)	**8**	L1,L2, L3
4	**OpenMP:** A Portable Solution for Threading Challenges in Threading a Loop, Loop–carried Dependence, Data– race Conditions, Managing Shared and Private Data, Loop Scheduling and Portioning, Effective Use of Reductions, Minimizing Threading Overhead, Work–sharing Sections, Performance–oriented Programming, Using Barrier and No wait, Interleaving Single– thread	**8**	L1,L2, L3,L4

	and Multi– thread Execution, Data Copy–in and Copy–out, Protecting Updates of Shared Variables, Intel Task queuing Extension to OpenMP, OpenMP Library Functions, OpenMP Environment Variables, Compilation, Debugging, performance. (Text: Chapter 6)		
5	**Solutions to Common Parallel Programming Problems:** Too Many Threads, Data Races, Deadlocks, and Live Locks, Deadlock, Heavily Contended Locks, Priority Inversion, Solutions for Heavily Contended Locks, Non–blocking Algorithms, ABA Problem, Cache Line Ping– ponging, Memory Reclamation Problem, Recommendations, Thread–safe Functions and Libraries, Memory Issues, Bandwidth, Working in the Cache, Memory Contention, Cache related Issues, False Sharing, Memory Consistency, Current IA– 32 Architecture, Itanium Architecture, High–level Languages, Avoiding Pipeline Stalls on IA–32, Data Organization for High Performance. (Text: Chapter 7)	**8**	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Apply the knowledge of parallel programming to solve the design problems.
CO2	Analyze the dataflow among different cores of the multicore processor.
CO3	Use different Threading APIs for programming multicore architectures.
CO4	Explain the different aspects of OpenMP in parallel programming.
CO5	Solve common parallel programming problems for multicore architectures.

Course outcome and program outcome mapping

CO1	PO2, PO3, PO4, PO5, PO12
CO2	PO2, PO3, PO4, PO5, PO6, PO12
CO3	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO4	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO5	PO1, PO2, PO3, PO4, PO5, PO6, PO8, PO12

TEXT BOOKS:

1. Shameem Akhter and Jason Roberts "Multicore Programming, Increased Performance through Software Multi–threading" Intel Press, 2006.ISBN 0-9764832-4-6.

REFERENCE BOOKS/WEBLINKS:

1. Calvin Lin, Lawrence Snyder, "Principles of Parallel Programming" Pearson Education, 2009. ISBN-13: 978-0321487902.
2. Michael J. Quinn ,"Parallel Programming in C with MPI and OpenMP", Tata McGraw Hill, 2004. ISBN 13: 9780070582019.
3. David E, Culler, Jaswinder Pal Singh with Anoop Gupta "Parallel Computer Architecture A Hardware/ Software Approach", eBook ISBN: 9780080573076 Hardcover ISBN: 9781558603431.

Subject Title**: Static Timing Analysis (STA)**		
Subject Code**: MEC205D**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Understand timing analyses at various process, environment and interconnect corners.
2. Apply the learnt concepts of STA to evaluate the delay of the circuits.
3. Understand and analyze the signal integrity issues for the IC.
4. Generate the timing analysis report using EDA tool.
5. Understand verification and analyze the generated report to identify issues for the violation
6. Learn different techniques to meet timing in an IC design.
7. Set up the timing analysis environment and perform the timing analysis for various cases.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**Introduction**: Nanometer Designs, What is Static Timing Analysis?. Why Static Timing Analysis?, Crosstalk and Noise, Design Flow, CMOS Digital Designs, FPGA Designs, Asynchronous Designs, STA at Different Design Phases, Limitations of Static Timing Analysis, Power Considerations, Reliability Considerations, **STA Concepts**: CMOS Logic Design, Basic MOS Structure, CMOS Logic Gate, Standard Cells, Modeling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions .	**8**	L1,L2, L3
2	**Standard Cell Library**: Pin Capacitance, Timing Modeling, Timing Models - Combinational Cells, Timing Models - Sequential Cells, State-Dependent Models, Interface Timing Model for a Black Box, Advanced Timing Modeling, Power Dissipation Modeling, Other Attributes in Cell Library, Characterization and Operating Conditions.	**8**	L1,L2, L3
3	**Interconnect Parasitics:** RLC for Interconnect, Wireload Models, Representing Coupling Capacitances, Hierarchical Methodology, Reducing Parasitics for Critical Nets. **Delay Calculation**: Overview, Cell Delay using Effective Capacitance, Interconnect Delay, Slew Merging, Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation, Slack Calculation.	**8**	L1,L2, L3
4	**Configuring the STA Environment**: What is the STA Environment? Specifying Clocks, Generated Clocks, Constraining Input Paths, Constraining Output Paths, Timing Path Groups, Modeling of External Attributes, Design Rule Checks, Virtual Clocks, Refining the Timing Analysis, Point-to-Point Specification, Path Segmentation.	**8**	L1,L2, L3,L4
5	**Timing Verification**: Setup Timing Check, Hold Timing Check, Multicycle Paths, Crossing Clock Domains, False Paths, Half- Cycle Paths, Removal Timing Check, Recovery Timing Check, Timing across Clock Domains, **Examples**: Slow to Fast Clock Domains, Fast to Slow Clock Domains, Half-cycle Path - Case 1, Half-cycle Path - Case 2, Fast to Slow Clock Domain, Slow to Fast Clock Domain, Multiple Clocks.	**8**	L1,L2, L3,L4
*BTL: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical			

Note: • Each Unit will have internal choice for SEE. • The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.	
COURSE OUTCOMES: After studying this course, students will be able to:	
CO1	Evaluate the delay of any given digital circuits.
CO2	Prepare the resources to perform the static timing analysis using EDA tool
CO3	Prepare timing constraints for the design based on the specification.
CO4	Generate the timing analysis report using EDA tool for different checks.
CO5	Perform verification and analyze the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing.
Course outcome and program outcome mapping	
CO1	PO1, PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4,PO5
CO4	PO7, PO8,
CO5	PO3, PO4
TEXT BOOKS: 1. J. Bhasker, R Chadha,., “Static Timing Analysis for Nanometer Designs: A Practical Approach”, Springer, 2009.	
REFERENCE BOOKS/WEBLINKS: 1. Sridhar Gangadharan, Sanjay Churiwala, “Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)”, Springer, 2013. 2. Naresh Maheshwari and Sachin Sapatnekar, "Timing Analysis and Optimization of sequential Circuits", Springer Science and Business Media, 1999.	

Subject Title**: Algorithms for VLSI Physical Design**		
Subject Code**: MEC206A**	No. of Credits**: 03 = 3:0:0:0 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Explain the need for synthesis and verification for digital circuits
2. Describe the VLSI Automation algorithms used for physical design
3. Understand the problem of placement and routing and identify algorithms to address these problems.
4. Illustrate the concept of cell routing constrained and unconstrained via minimization.
5. Get the knowledge of compaction problem and basic ways to tackle it.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Logic Synthesis & Verification:** Introduction to combinational logic synthesis, Binary Decision Diagram, **High Level Synthesis**: Hardware models for High-level synthesis, Internal representation of the input algorithm (Data Flow Graph). [TEXT 2]	8	L1,L2, L3
2	**VLSI Automation Algorithms**: **Partitioning:** problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms [TEXT 1]	8	L1,L2, L3
3	**Placement, Floor Planning & Pin Assignment**: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment [TEXT 1]	8	L1,L2, L3
4	**Global Routing**: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches **Detailed Routing**: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms [TEXT 1]	8	L1,L2, L3,L4
5	**Over The Cell Routing & Via Minimization**: two layers over the cell routers, constrained & unconstrained via minimization **Compaction:** problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction [TEXT 1]	8	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Understand and exploit the features of logic synthesis and high level synthesis at introductory level in the VLSI design which happens before the physical design.
CO2	Understand the partitioning process, formulate the problem, classify and exemplify the different partitioning algorithms.
CO3	Understand the placement, floor-planning and pin assignment process, formulate the problem, classify and exemplify the different algorithms.
CO4	Understand the placement floor-planning and pin assignment process, formulate the problem, classify and exemplify the different algorithms.

CO5	Understand the over the cell routing and compaction process, formulate the problem, and exemplify the different algorithms.
Course outcome and program outcome mapping	
CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO4,PO5,PO7
CO4	PO1,PO2,PO3,PO4
CO5	PO4,PO6,PO7,PO12

TEXT BOOKS:

1. Naveed Shervani, "**Algorithms for VLSI physical design Automation**", Kluwer Academic Publisher, Second edition.
2. Sabih H. Gerez, "Algorithms for VLSI Design Automation", JOHN WILEY & SONS, 2000.

REFERENCE BOOKS/WEBLINKS:

1. Christophn Meinel & Thorsten Theobold, "**Algorithm and Data Structures for VLSI Design**", KAP, 2002.
2. Rolf Drechsheler : "**Evolutionary Algorithm for VLSI**", Second edition
3. Trimburger, "**Introduction to CAD for VLSI**", Kluwer Academic publisher, 2002
4. Andrew B. Kahng • Jens Lienig, Igor L. Markov, Jin Hu "**VLSI Physical Design:From Graph Partitioning to Timing Closure**", Springer publications, 2011.

Subject Title**: ARM Programming and Optimization**		
Subject Code**: MEC206B**	No. of Credits**: 03 = 3:0:0:0 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Understanding the programmer's model of ARM processor.
2. Use of available optimization methods for ARM architectures.
3. Realizing real time signal processing applications & primitive OS operations on different ARM architectures.
4. To analyze and demonstrate different applications on ARM development boards.
5. Understand the different memory optimization methods for ARM architectures

UNIT No.	Syllabus Content	No. of hours	*BTL
1	Introduction, Data Path Architecture, Registers, Modes, Exceptions **Programming in C for ARM**: Overview of C Compilers and optimization, basic C data types, C looping structures, register allocation, function calls, pointer aliasing, structure arrangement, bit fields, unaligned Data and endianess, division, floating point, inline functions and inline assembly, portability issues. (Text 1)	**8**	L1,L2, L3
2	**Writing and Optimizing ARM Assembly Code:** Writing assembly code, profiling and cycle counting, instruction scheduling, register allocation, conditional execution, looping constructs, Bit manipulation, efficient switches. Handling unaligned data. (Text 1)	**8**	L1,L2, L3
3	**Digital Signal Processing on ARM**: Representing a digital signal, Introduction to DSP on the ARM, FIR filters: Realization of filters on ARM7 and Cortex M3, IIR Filters: Realization of filters on ARM7 and Cortex M3, CMSIS DSP Library. (Text 1)	**8**	L1,L2, L3
4	**Firmware:** Firmware and Boot loader **Embedded Operating Systems:** Fundamental Components, Simple Operating System. (Text 1)	**8**	L1,L2, L3,L4
5	**Memory Protection Unit:** Over view of the MPU's, MPU registers, setting up the MPU, Memory barrier and memory configuration, Using sub-region disable, Consideration when using MPU, Other usages of MPU. (Text 2)	**8**	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Describe the programmer's model of ARM processor and Apply the optimization methods available for ARM architectures to design embedded software in C to meet given constraints.
CO2	Apply the optimization methods available for ARM architectures to design embedded software in assembly code to meet given constraints.
CO3	Realize real time signal processing applications on different ARM architectures by making use of software libraries.
CO4	Realize primitive OS operations on different ARM architectures by making use of software libraries.
CO5	Analyze the memory protection and optimization methods available for ARM architectures.

Course outcome and program outcome mapping	
CO1	PO2, PO3, PO4, PO5, PO12
CO2	PO2, PO3, PO4, PO5, PO6, PO12
CO3	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO4	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO5	PO1, PO2, PO4, PO5, PO6, PO12

TEXT BOOKS:

1. ARM System Developers Guide, Andrew N Sloss, Dominic Symes, Chris Wright, 2008, Elsevier, Morgan Kaufman publishers, ISBN-13:9788181476463.

2. The definitive Guide to the ARM Cortex- M3 & M4 Processors, Joseph Yiu, 3rd Edition, 2014, Newnes (Elsevier), ISBN: 978-93-5107-175-4.

REFERENCE BOOKS/WEBLINKS:

1. ARM System on Chip Architecture, Steve Furber, 2nd Edition, 2001, Pearson Education Limited, ISBN-13:9780201675191.

2. Technical reference manual for ARM processor cores, including Cortex M series, ARM 11, ARM 9 & ARM 7 processor families.

Subject Title**: High Speed VLSI Design**		
Subject Code**: MEC206C**	No. of Credits**: 03 = 3:0:0:0 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Learn sources of process – driven performance variation in quarter-micron CMOS and apply the rules of thumb.
2. Comprehend non-clocked static circuit families, used to implement combinatorial logic.
3. Interpret the design styles used for clocked and non-clocked systems.
4. Explore the design parameters such as on-chip device length tolerance, supply rail inconsistency and temperature variations.
5. Understand clocking styles, jitters and skews.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Process Variability:** Introduction**,** Front-end -of-line variability considerations, charge loss mechanisms, back-end-of- line variability considerations.**[Text 1]**	**8**	L1,L2, L3
2	**Non-Clocked logic styles**: Introduction, static CMOS structures, DC VS logic, Non-clocked pass-gate families. **Clocked logic styles**: Introduction, single-rail domino logic styles. Dual-rail domino structures, latched domino structures, clocked pass gate logic. **[Text 1]**	**8**	L1,L2, L3
3	**Circuit Design margin and design variability:** Introduction, process induced variation, design induced variations, and application induced variations', Noise. **Latching Strategies:** Introduction, basic latch design, latching single ended logic, latching differential logic, race-free latched for pre-charge logic.**[Text 1]**	**8**	L1,L2, L3
4	**Interface Techniques:** Introduction, signaling standard, chip-chip communication networks, ESD protection, Driver design techniques, receiver design techniques.**[Text 1]**	**8**	L1,L2, L3,L4
5	**Clocking styles:** Introduction, clock jitter and skew, clock generation and clock distribution.**[Text 1]**	**8**	L1,L2, L3,L4

***BTL**: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Accomplish their goal in achieving the tradeoffs in performance, power, area, reliability and cost by the selection of design styles
CO2	Analyze strengths and weakness of clocked and non-clocked logic circuit families in terms of characteristics.
CO3	Interpret the performance considerations to enable high speed communication; by choosing the input and output convention compatible with signal levels required for the design.
CO4	Analyze Interface techniques for signaling standard and communications.
CO5	Design clocking styles clock distributions and jitters.

Course outcome and program outcome mapping	
CO1	PO1,PO2
CO2	PO2, PO3, PO4
CO3	PO3, PO5, PO6
CO4	PO4,PO5,PO6,PO7
CO5	PO5, PO6, PO7

TEXT BOOKS:

1. Kerry Bernstein, “High Speed CMOS Design Styles”, Kluwer, 1999.

REFERENCE BOOKS/WEBLINKS:

1. Howard Johnson & Martin Graham, “High Speed Digital Design” AHandbook of Black Magic, Prentice Hall PTR, 1993.
2. William S. Dally & John W. Poulton, “Digital Systems Engineering”,Cambridge University Press, 1998.
3. Masakazu Shoji, “High Speed Digital Circuits”, Addison Weley Publishing Company, 1996.

Subject Title: **VLSI - DSP Architectures**		
Subject Code: **MEC206D**	No. of Credits: **03 = 3:0:0:0 (L:T:P:S)**	No. of lecture hours per week: **03**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **40**

Course Learning Objectives: This course will enable the students to:

1. To provide sound foundation of digital signal processing (DSP) architectures and designing efficient VLSI architectures for DSP systems
2. Understand the concepts of digital filters
3. Understand the arithmetic architectures suitable for DSP processors
4. Get in-depth knowledge in Pipelining and parallel processing pipelining architecture suitable for low power architectures
5. Get Knowledge on clock distribution suitable for DSP processors architectures
6. Understand the working of Programmable Digital Signal Processors DSP

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	DSP Array processor architectures, fast convolution Cook Toom-algorithm, Winograd algorithm, Iterated convolution, Cyclic convolution, algorithmic strength reduction in filters and transforms, pipelined and parallel recursive and adaptive filters	**8**	L1,L2, L3
2	Scaling and round off noise, digital lattice filter structures, bit level arithmetic architectures, parallel multipliers, interleaved floor plan and bit plane based digital filters, bit serial multipliers, bit serial filter design and implementation.	**8**	L1,L2, L3
3	Pipelining and parallel processing pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power, retiming, unfolding, folding transformation, register minimization techniques, Register minimization in folded architectures.	**8**	L1,L2, L3
4	Synchronous wave and asynchronous pipelines, synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI design, wave pipelining, asynchronous pipelining	**8**	L1,L2, L3,L4
5	Programmable Digital Signal Processors DSP Processors for mobile and wireless communications, Processors for multimedia signal Processing, Multi Processor Systems	**8**	L1,L2, L3,L4

***BTL**: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Design arithmetic architectures, parallel multipliers, Pipelining and parallel processing pipelining of FIR digital filters,
CO2	Able to develop DSP and VLSI architectures for various application using system concepts given.
CO3	Create new approaches using the knowledge and skills developed.
CO4	Ability to develop new products in DSP and VLSI field
CO5	Do the analysis on the digital system developed and give the performance analysis on the product developed.

Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3,PO4,PO5
CO2	PO2,PO3,PO4
CO3	PO3,PO4
CO4	PO5,PO6
CO5	PO6,PO7,PO8

TEXT BOOKS:

1. "VLSI Digital Signal Processing Systems Design and Implementation" Keshab K. Parhi, Wiley VCH Verilog GmbH & Co. K GaA.

REFERENCE BOOKS/WEBLINKS:

1. "Architectures for Digital Signal Processing", Peter Pirsch, IEEE Signal Processing Magazine, Vol.14, No.5, September.
2. "DSP Processor fundamentals Architecture and Features", IEEE Press series on Signal Processing.

Subject Title: **VLSI Design and Embedded Systems Lab-II**		
Subject Code**: MECL207**	No. of Credits**: 02 = 1:0:2 (L:T:P)**	No. of lecture hours per week**: 04**
Exam Duration**: 3 Hours**	CIE + SEE **= 50+50=100**	Total No. of lecture hours**: 36**

Course Learning Objectives: This course will enable the students to:

1. Objective of this lab is to learn the Virtuoso tool as well learn the flow of the Full Custom IC design cycle.
2. Usage of DRC, LVS and Parasitic Extraction on the various designs, like inverter, differential amplifier, operational amplifier, R-2R based DAC and Mixed signal design of SAR based ADC,
3. Timing analysis and power analysis of the circuits using CADENCE
4. Design a testing program for thread and process creation.
5. Design a testing program for specified conditions using multithreaded application.
6. Design a POSIX based message queue for communicating between two tasks.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
	PART A		
1	Design an INVERTER and analyze the following parameters using the cadence VIRTUSO *Schematic Entry* *Building the Inverter Test Design* *Analog Simulation* *Creating Layout View of Inverter* *Parasitic Extraction* *Creating the Configuration View* *Generating Stream Data*	**3**	L1,L2, L3,L4
2	Design an Diff_ Amplifier and analyze the following parameters using the cadence VIRTUSO *Schematic Entry* *Analog Simulation* *Creating a Layout View of Diff_ Amplifier* *Physical Verification*	**3**	L1,L2, L3,L4
3	Design an Common Source Amplifier and analyze the following parameters using the cadence VIRTUSO *Schematic Entry* *Symbol Creation* *Building the Common Source Amplifier Test Design* *Analog Simulation with Spectre* *Creating a layout view of Common Source Amplifier*	**3**	L1,L2, L3,L4
4	Design an Common Drain Amplifier and analyse the following parameters using the cadence VIRTUSO *Schematic Entry Symbol Creation* *Building the Common Drain Amplifier Test Design* *Analog Simulation with Spectre* *Creating a layout view of Common Drain Amplifier*	**3**	L1,L2, L3, L4
5	Design an Operational Amplifier and analyze the following parameters using the cadence VIRTUSO	**3**	L1,L2, L3, L4

	Schematic Entry *Symbol Creation* *Building the Operational Amplifier Test Design* *Analog Simulation with Spectre* *Creating a layout view of Operational Amplifier*		
6	Design an R-2R DAC and analyze the following parameters using the cadence VIRTUSO *Schematic Entry Symbol Creation* *Building the R-2R DAC Test Design* *Analog Simulation with Spectre* *Creating a layout view of R-2R DAC*	**3**	L1,L2, L3,L4
7	Design an SAR BASED ADC and analyse the following parameters using the cadence VIRTUSO *Design Information* *Import the Verilog Module into ADE Using Verilog In.* *Schematic Entry* *Mixed Signal Simulation Using AMS in ADE*	**3**	L1,L2, L3,L4
	PART-B		
1	Creating a Thread and Process using POSIX Thread standard.	**3**	L1,L2, L3,L4
2	Creating two pipes for sending and receiving messages.	**3**	L1,L2, L3,L4
3	Creating 'n' number of child Threads.	**3**	L1,L2, L3,L4
4	Program to pass message through pipes.	**3**	L1,L2, L3,L4
5	Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes.	**3**	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- The internal assessment will be based on Record, Conduction, Question and Answer session.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Design analog circuits
CO2	Draw layouts of analog circuits
CO3	Analyze the analog circuits using CADENCE
CO4	Create test programs for thread and process.
CO5	Develop the Multithreaded application.
CO6	Create a POSIX based message queue for communicating between two tasks.

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4
CO4	PO1,PO4,PO8
CO5	PO4,PO5,PO6,PO8
CO6	PO3,PO4,PO5,PO6,PO8,PO9

TEXT BOOKS:

1. CMOS analog circuits by Allen Philip

2. Shibu K V, “Introduction to Embedded Systems”, First Edition, Tata McGraw Hill Education Private Limited, 2009.

REFERENCE BOOKS/WEBLINKS:

1. https://www.buecher.de › ... › Mikroelektronik › Sonstige
2. https://www.cadence.com
3. https://www.cadence.com › Home › Tools
4. https://www.cadence.com › Home › Training › All Courses.

Subject Title**:** MOOC online courses*		
Subject Code**:**	No. of Credits**: 03**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + SEE **=**	Total No. of lecture hours**: 40**

#	**Course Type**	**Course Title**	**Course Duration**
1	MOOC – Swayam NPTEL	VLSI Design Flow: RTL to GDS	12 weeks
2	MOOC – Swayam NPTEL	Analog Electronics	12 weeks
3	MOOC – Swayam NPTEL	System Design using Verilog	12 weeks
4	MOOC – Swayam NPTEL	Computer Architecture And Organization	12 weeks
5	MOOC – Swayam NPTEL	Fabrication Techniques for MEMs-based sensors: clinical perspective	12 weeks
6	MOOC – Swayam NPTEL	Fundamentals of Artificial intelligence	12 weeks
7	MOOC – Swayam NPTEL	Electronic Systems Design: Hands-on Circuits and PCB Design with CAD Software	12 weeks
8	MOOC – Swayam NPTEL	Industrial Automation and Drives	12 weeks
9	MOOC – Swayam NPTEL	Fundamentals of Nano and Quantum Photonics	12 weeks
10	MOOC – Swayam NPTEL	Introduction To Algorithms and Analysis	12 weeks
11	MOOC – Swayam NPTEL	Introduction to Internet of Things	12 weeks
12	MOOC – Swayam NPTEL	Analog IC design	12 weeks
13	MOOC – Swayam NPTEL	C-based VLSI design	12 weeks
14	MOOC – Swayam NPTEL	Embedded System design	12 weeks
15	MOOC – Swayam NPTEL	Digital VLSI Testing	12 weeks
16			

*MOOC/VTU online courses approved list. Students have to register and complete atleast three of the courses selected from the list. Any new course if suitable can be considered for student registration upon approval of the Board of Studies.