Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY

(An Autonomous Institute affiliated to VTU, Accredited by NAAC with 'A' grade)

BDA Outer Ring Road, Mallathalli,Bengaluru-56

Board Of Studies 2023-24

Approved
Scheme and Syllabus of
V & VI Semester
For
2021 Batch

Submitted by

Department of Electronics and Communication Engineering

To

DEAN (Academic)

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

V Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	PCC	21ECT501	Digital Communication	ECE	3	0	0			3	50	50	100	3
2	IPCC	21ECT502	Microprocessor & Microcontrollers	ECE	3	0	2		3	3	50	50	100	4
3	PCC	21ECT503	Computer Communication Networks	ECE	3	0	0		3	3	50	50	100	3
4	PCC	21ECT504	Microwave Theory & Antennas	ECE	3	0	0		3	3	50	50	100	3
5	PCC	21ECL505	Communication Lab II	ECE	0	0	2		3	3	50	50	100	1
6	AEC	21RMT506	Research Methodology & Intellectual Property Rights	Any Department	2	0	0		2	2	50	50	100	2
7	HSSC	21CVT507	Environmental Studies	Civil/Chemistry	1	0	0			1	50	50	100	1
8	AEC	21ECL508x	Ability Enhancement Course-V	ECE						1/2	50	50	100	1
9	HSSC	21HSN509	Aptitude and Verbal ability skills		1	0	1	0		2	50	--	PP/NP	0
										Total	450	400	800	18

Ability Enhancement Course - V

21ECL5081	Computer Communication Networks Lab	**21ECL5083**	Antenna Design & Testing
21ECL5082	Communication Simulink Toolbox	**21ECL5084**	Microwaves toolbox

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

VI Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	HSSC	21ECT601	Technological Innovation Management and Entrepreneurship								50	50	100	03
2	IPCC	21ECT602	Computer Organization & ARM Microcontrollers	ECE	2	2			4	3	50	50	100	04
3	PCC	21ECT603	VLSI Design & Testing	ECE	3				3	3	50	50	100	03
4	PEC	21ECT604X	Professional Elective -I	ECE	3				3	3	50	50	100	03
5	OEC	21ECT605X	OpenElective-I	ECE	3				3	3	50	50	100	03
6	PCC	21ECL606	VLSI Laboratory	ECE			2		2		50	50	100	01
7	MP	21ECM607	Mini Project	ECE			2		2		50	50	100	02
8	INT	21ECI608	Innovation/Entrepreneurship /Societal Internship								50	50	100	03
9	HSSC	21HSN609	Analytical & Reasoning skills	Placement Cells	2	0	0-		02	--	50	--	PP/NP	00
								Total			500	450	900	22

Research/Industrial Internship - At the End of the sixth / Seventh semester (in two cycles to accommodate all the students of the University) Research/Industrial Internship shall be carried out – Based on industrial/Govt./NGO/MSME/Rural Internship/Innovation/Entrepreneurship. All the students admitted shall have to undergo a mandatory internship of 24 weeks during the vacation of VI/VII semesters. A University Viva-Voce examination shall be conducted during VII/VIII semester and the prescribed credit shall be included in VII/VIII semester. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements. Research internship Students have to take up research internships at Centers of Excellence (CoE) / Study Centers established in the same institute and /or out of the institute at reputed research organizations / Institutes. A research internship is intended to give you the flavour of current research going on on a particular topic/s. The internships serve this purpose. They help students get familiarized with the field, the skill needed the effort amount and kind of effort required for carrying out research in that field.

Industry internships: This is an extended period of work experience undertaken by university/Institute students looking to supplement their degree with professional development. The students are allowed to prepare themselves for the workplace and develop practical skills as well as academic ones. It also helps them learn to overcome

unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with "unexpected contingencies" helps students recognize, appreciate, and adapt to organization realities by tempering knowledge with practical constraints.

Mini-project work: Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini-project can be assigned to an individual student or a group having not more than 4 students. (or Mini Project is a laboratory-oriented course which will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications) CIE procedure for
Mini-project: (i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide. The CIE marks awarded for the Mini-project work, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the college. The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates. SEE for Mini-project: (i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester-end examination (SEE) conducted at the department. (ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester-end examination (SEE) conducted separately at the departments to which the student/s belongs
Open Elective Courses: Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives). Selection of an open elective shall not be allowed if, • The candidate has studied the same course during the previous semesters of the program. • The syllabus content of open electives is similar to that of the Departmental core courses or professional electives. • A similar course, under any category, is prescribed in the higher semesters of the program. • Registration to electives shall be documented under the guidance of the Programme Coordinator/ Advisor/Mentor

Professional Elective Courses-I		**Open Elective Courses-I**	
Subject Code	**Title**	**Subject Code**	**Title**
21ECE6041	Artificial Neural Networks (L:T:P :: 2:2:0)	**21ECE6051**	Communication Engineering (L:T:P :: 3:0:0)
21ECE6042	Cryptography (L:T:P :: 2:2:0)	**21ECE6052**	Microcontrollers (L:T:P :: 3:0:0)
21ECE6043	Python Programming (L:T:P :: 2:0:2)	**21ECE6053**	Basic VLSI Design (L:T:P :: 3:0:0)
21ECE6044	Micro Electro Mechanical Systems (L:T:P :: 3:0:0)	**21ECE6054**	Electronic Circuits with Verilog (L:T:P :: 2:0:2)
		21ECE6055	Sensors & Actuators (L:T:P :: 3:0:0)

Assessment and Evaluation method

V Semester:

- **21ECT502- Microprocessor & Microcontrollers** shall have the 03 hours of theory examination (SEE), however, practical sessions question shall be included in the theory question papers
- **ESC or ETC, of 03 credits Courses** shall have only a theory component (L: T :P:S=3:0:0:0) or if the nature the of course required practical learning then the syllabus shall be designed as an Integrated course (L: T:P:S= 2:0:2:0). All **PLC** courses are Integrated courses.
- **All 01 Credit** courses shall have the SEE of 02 hours duration and the pattern of the question paper shall be MCQ
- **Integrated courses (IPCC)** will have 50 marks CIE and 50 Marks SEE.
- **Non-integrated courses (PCC)** have 50 marks CIE (including 5 marks Assignment and 5 marks Group Activity) and 50 Marks SEE.

VI Semester:

- **21ECT602- Computer Organization & ARM Microcontrollers** shall have the 03 hours of theory examination (SEE), however, practical sessions question shall be included in the theory question papers
- **ESC or ETC, of 03 credits Courses** shall have only a theory component (L: T :P:S=3:0:0:0) or if the nature the of course required practical learning then the syllabus shall be designed as an Integrated course (L: T:P:S= 2:0:2:0). All **PLC** courses are Integrated courses.
- **All 01 Credit-** courses shall have the SEE of 02 hours duration and the pattern of the question paper shall be MCQ
- **Integrated courses (IPCC)** will have 50 marks CIE and 50 Marks SEE.
- **Non-integrated courses (PCC)** have 50 marks CIE (including 5 marks Assignment and 5 marks Group Activity) and 50 Marks SEE.

V Semester

DIGITAL COMMUNICATION			
Course Code:	21ECT501	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:2	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	3	**Exam Hours:**	3

Course objectives:

1. Understand the mathematical representation of signal, symbol, and noise.
2. Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
3. Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
4. Compute performance parameters and mitigate channel induced impediments in corrupted channel conditions.

Module-1

Bandpass Signal to Equivalent Low pass:

Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low pass representation of bandpass systems, Complex representation of band pass signals and systems (Text 1: 2.8, 2.9, 2.10, 2.11, 2.12, 2.13).

Line codes: Unipolar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities (Text 1: Ch 6.10). Overview of HDB3, B3ZS, B6ZS (Ref.1: 7.2)

Teaching Learning Method:	Lectures, Interactive (Q & A discussion), Activity/Assignment based
RBT Level:	L1, L2, L3

Module-2

Signaling over AWGN Channels-

Introduction, Geometric representation of signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver.

(Text 1:7.1, 7.2, 7.3, 7.4)

Teaching Learning Method:	Lectures, Interactive (Q&A discussion), Activity/Assignment based
RBT Level:	L1, L2, L3, L4

Module-3

Digital Modulation Techniques:

Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M ary PSK, M-ary QAM. (Relevant topics in Text 1of 7.6, 7.7).

Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability (Relevant topics in Text 1of 7.8).

Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivation of probability of error equation) (Text 1: 7.11, 7.12. 7.13).

Teaching Learning Method:	Lectures, Interactive (Q&A discussion), Activity/Assignment based
RBT Level:	L1, L2, L3, L4

Module-4

Communication through Band Limited Channels:

Digital Transmission through Band limited channels: Digital PAM Transmission through Band limited Channels, Signal design for Band limited Channels: Design of band limited signals for zero lSI-The Nyquist Criterion (statement only), Design of band limited signals with controlled lSI-Partial Response signals, Probability of error for detection of Digital PAM: Probability of error for detection of Digital PAM with Zero lSI, Symbol-by-Symbol detection of data with controlled lSI (Text 2: 9.1, 9.2, 9.3.1, 9.3.2). Channel Equalization: Linear Equalizers (ZFE, MMSE), (Text 2: 9.4.2).

Teaching Learning Method:	Lectures, Interactive (Q&A discussion), Activity/Assignment based
RBT Level:	L1, L2, L3, L4

Module-5

Principles of Spread Spectrum:

Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95 (Text 2: 11.3.1, 11.3.2, 11.3.3, 11.3.4, 11.3.5, 11.4.2).

Teaching Learning Method:	Lectures, Interactive (Q&A discussion), Activity/Assignment based
RBT Level:	L1,L2,L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Understand the representation of bandpass signals into its' equivalent low pass signals and properties of various line code formats and their usage.

CO2. Analyse and compute the performance parameters of two different receiver architectures when low-pass and band pass symbol sets defined over symbol period are transmitted over noisy and noiseless bandlimited channel.

CO3. Generate and Evaluate different M-ary symbol sets on performance parameters at the receiver side under ideal and corrupted bandlimited channels.

CO4. Demonstrate the digital transmission of bandpass signals through bandlimited channels incorporating signal design processed at the receiver to meet specified performance criteria.

CO5. Understand the principles of spread spectrum communications to identify its application to recent communication systems in use today.

Suggested Learning Resources:

Text Books:

1: Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0—47 1-64735-5.

2: John G Proakis and Masoud Salehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN 978-8—131-70573-5.

3: B.P.Lathi and Zhi Ding, "Modern Digital and Analog communication Systems", Oxford University Press, 4th Edition, 2010, ISBN: 978-0- 198-07380-2.

Reference Books

1: Ian A Glover and Peter M Grant, "Digital Communications", Pearson Education, Third Edition, 2010, ISBN 978-0-273-71830-7.

2: Bernard Sklar and Ray, "Digital Communications - Fundamentals and Applications", Pearson Education, Third Edition, 2014, ISBN: 978-81-317-2092-9.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity 1: Presentation on various topics

Activity 2: Small projects on applications of digital communication
Activity 3: Group discussion on various topics of digital communication

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	1			1	1	2		1		2	2	2	2
CO2	3	3	2	2		2	1	2		2		3	3	3	3
CO3	3	3	2	2		2	2	2		3		3	3	3	3
CO4	3	3	2	2		2	2	2		3		3	3	3	3
CO5	2	1	1	1		2	2	2		3		3	2	2	3

High-3, Medium-2, Low-1

V Semester

MICROPROCESSOR & MICROCONTROLLER			
Course Code:	21ECT502	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	52	**Total Marks:**	100
Credits:	04	**Exam Hours:**	03

Course objectives:

i. To illustrate the architecture of 8051 Micro controller.

ii. To understand the Special Function Registers, addressing modes and memory organization.

iii. To introduce Assembly language programming of 8051 Micro controller.

iv. To understand the RISC V microprocessors and Instruction Set Architecture.

Module-1	**08 hrs**

Introduction to microprocessors and microcontrollers: RISC & CISC CPU Architectures, Harvard & Von- Neumann CPU architecture.

8051 Microcontroller: The 8051 Architecture, Pin diagram of 8051, Memory organization, External Memory interfacing. Classification of Instruction, Addressing modes: Immediate addressing, Register addressing, Direct addressing, Indirect addressing, relative addressing, Absolute addressing, bit direct addressing. **(TEXT 1 and TEXT 2)**

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, l3

Module-2	**07 hrs**

8051 Instructions and Programming: 8051 instructions, Data transfer instructions,Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instructions. 8051 programming: Assembler directives, Assembly language programs and Time delay calculations. Stack operations.

Introduction to Embedded C: C data types, logical operations, programming 8051 using embedded C

(**TEXT 2 and TEXT 3**)

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3

Module-3	**09 hrs**

Timers/counters: 8051 timers/counters, delay program, counter programming 8051 timers to generate delay and counting operation using assembly and C language. Data communication, Basics of Serial Data Communication, 8051 Serial Communication, Programming in assembly and C.

Serial Communication: Data communication, Basics of Serial Data Communication, 8051 Serial Communication, Programming in assembly and C.

8051 interrupts and interfacing: Interrupts and Basics of interrupts, 8051 Interfacing and Applications: Basics of I/O concepts, I/O Port Operation, Interfacing 8051 to DAC,LED/LCD. **(TEXT 3)**

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3

Module-4	**08 hrs**

RISC-V Microprocessors: Introduction, Modular vs. Incremental ISAs, ISA Design 101 **RV32I: RISC-V Base Integer ISA:** Introduction, RV32I Instruction formats, RV32I Registers, RV32I Integer Computation, RV32I Loads and Stores, RV32I Conditional Branch, RV32I Unconditional Jump, RV32I Miscellaneous, Comparing RV32I, ARM-32, MIPS-32, and x86-32 using Insertion Sort. **RISC-V Assembly Language:** Introduction, Calling convention, Assembly, Linker, Static vs. Dynamic Linking, Loader.	
Teaching Learning Method:	Chalk and Talk, Power point presentations, Programming assignments
RBT Level:	L1, L2, L3

Module-5	**08 hrs**
RV32M: Multiply and Divide- Introduction **RV32F and RV32D: Single- and Double-Precision Floating Point**- Introduction, Floating-Point Registers, Floating-Point Loads, Stores, and Arithmetic, Floating-Point Converts and Moves, Miscellaneous Floating-Point Instructions, Comparing RV32FD, ARM-32, MIPS-32, and x86-32 using DAXPY. **RV32C: Compressed Instructions-** Introduction, **RV32A: Atomic Instructions-** Introduction, **RV32V: Vector**- Introduction	
Teaching Learning Method:	Chalk and Talk, Power point presentations, Programming assignments
RBT Level:	L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Conduct the following experiments by writing Assembly Language Program (ALP) using ARM Cortex M3 Registers using an evaluation board/simulator and the required software tool

Sl. No.	**Experiments**	**12 hrs**
1	**Data transfer programs-** **i]** WALP to transfer data between internal and external memories **ii]** WALP to exchange data between internal and external memories	
2	**Arithmetic operation programs-** **i]** WALP to add 10 bytes of data **ii]** WALP to add multi bytes of data **iii]** WALP to find the square and cube of an 8 bit binary number	

3	**Logical operation programs-**
	i] Let X, Y, Z refer to the contents of the memory location 30h,31h,and 32h respectively, write an ALP to perform the following logical operations;
	If X=00 perform the operation Y OR Z.
	If X=01 perform the operation Y AND Z.
	If X=02 perform the operation Y XOR Z.
	ii] WALP to compare the bytes of data present at the memory location 21h and 22h and represent the result of comparison through the bits whose addresses are 00h and 01h.
	If (21h)<(22h)then clear the bit at 01h and also set the bit at 00h.
	If (21h)>(22h)then set the bit at 01h and also clear the bit at 00h.
	If (21h)=(22h)then set the bit at 01h and also set the bit at 00h.
	iii] WALP to stimulate the Boolean expression **Eg:** Y=A+BC.	

4	i] **Parity Program-** WALP to count the number of 1's in a byte which is be accepted from the port 0 and displays the result on the port1. **ii] Palindrome Program-** WALP to check whether the gives byte is a valid bit palindrome,accep byte from the port0 and display aah if valid else 00H in port1.
5	**Timer program-** WALP to generate the output value AAH and 55H alternatively at the Port 0 for every 2 sec.
6	**Counter program-** WALP to count the number of inputs to the counter_0 by configuring the timer as a counter in mode_1 and display the count in ports.
7	**Design and implementation of RISC V Processor Subsystem using Verilog:** a) Floating Point Addition & Subtraction. b) Floating Point Multiplication. c) Operand Logic.
Demonstration Experiments (For CIE only not for SEE) Conduct the following experiments on an 8051 MC using evaluation version of Embedded 'C' & Keil µvision-3 tool/compiler.	
08	**Demonstrate the serial communication-**WALP to transfer the characters serially.
09	**Demonstrate the interfacing of DAC programs-**WALP to generate the wave forms i] Square wave ii] Triangle wave **iii]** Ramp wave (Both positive and negative)
10	**Demonstrate the interfacing of LED programs-** WALP to display the count (UP/DOWN/LED BLINKING)

Course outcomes:

At the end of the course the student will be able to:

CO1: understand the features and architecture of 8051 Microcontroller.

CO2: program 8051 microcontroller using assembly language and embedded C.

CO3: configure timers/counters of 8051 and understand serial communication and interrupts of 8051.

CO4: understand need of RISC V microprocessors and basics of RV32I.

CO5: understand basics of RV32M, RV32F, RV32D, RV32C, RV32A, RV32V.

Suggested Learning Resources:

Text Books:

1. **Yu-cheng Liu, Glenn A.Gibson,** "Microcomputer Systems: The 8086/8088 Family Architecture, Programming, and Design"

2. **Kenneth J. Ayala,** "The 8051 Microcontroller Architecture, Programming & Applications", 2e Penram International, 1996 / Thomson Learning 2005.

3. **Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay,** "The 8051 Microcontroller and Embedded Systems – using assembly and C", PHI, 2006 / Pearson, 2006.

4. **The RISC-V Reader: An Open Architecture** Atlas Beta Edition, 0.0.1, David Patterson and Andrew Waterman, October 4, 2017

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Programming Assignments / Mini Projects can be given to improve programming skills

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3					2	2	2				2	1	3	1
CO2	3	3	3			2		2	1			2	1	3	1
CO3	3	3	3		3	2		2	1			2	1	3	1
CO4	3	2	3		3	2		2	1			2	1	3	1
CO5	3	2	2		2	2		2	1				1	3	1

High-3, Medium-2, Low-1

V Semester

COMPUTER COMMUNICATION NETWORKS			
Course Code:	21ECT503	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:1	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	3	**Exam Hours:**	03

Course objectives:
This course will enable students to:
1. Provide Insight into the basics of networking, OSI reference and TCP/IP model.
2. Study of access links, protocols, error detection and correction techniques in the data link layer.
3. Understanding of routing algorithms, addressing techniques of the network layer.
4. Understand Protocol techniques of the transport layer.
5. Identify Services, Protocols, directory service and Security of the application layer

Module-1	**08 hrs**
Introduction: Data communication, Networks, Network types. **Network Models:** TCP/IP Protocol Suite, The OSI Model, Connecting devices. (1.1, 1.2, 1.3.1-1.3.4, 2.2, 2.3, 17.1.1-17.1.3 of Text)	
Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of OSI and TCP-IP protocol suites, Example of ARP and RARP.
RBT Level:	L1, L2, L3
Module-2	**08 hrs**
Data-Link Layer: Introduction, Link Layer addressing. **Error Detection and Correction:** Introduction, Cyclic Redundancy Check, Checksum. **Media Access Control:** Random Access, Controlled Access, Channelization, Virtual LAN. **Wired LANs**: Ethernet Protocol, Standard Ethernet. (9.1, 9.2.1, 9.2.2, 10.1, 10.3.1, 10.4.1, 10.4.2, 12.1, 12.2, 12.3, 13.1,13.2.1, 13.2.2,17.1, 17.2 of Text)	
Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animations showing Framing, CSMA, Connecting devices, Problems on ALOHA, CSMA, Framing and Standard Ethernet.
RBT Level:	L1, L2, L3
Module-3	**08 hrs**
Network Layer: Network Layer services, Packet Switching, IPV4 Addresses, IPv6 addressing and Protocol. **Network Layer Protocols:** Internet Protocol (IP). **Unicast Routing:** Routing Algorithms. (18.1, 18.2, 18.4, 19.1, 20.1, 20.2 ,22.1 ,22.2 of Text)	
Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of DHCP, routing protocols, Numericals on Addressing,
RBT Level:	L1, L2, L3
Module-4	**08 hrs**
Transport Layer: Introduction, Transport Layer Protocols. **Transport-Layer Protocols in the Internet:** Port numbers, User Datagram Protocol, Transmission Control Protocol. 23.1, 23.2, 24.1.2 - 24.3.5 of Text)	
Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation/Implementation of Flow control protocols and TCP using

RBT Level:	simulators. L1, L2, L3
Module-5	**08 hrs**
Application Layer: Introduction, **Standard Client – Server Protocols**: World Wide Web and HTTP, Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS, Network Security. (25.1, 26.1.2, 26.2, 26.3, 26.6 ,31.1 of Text)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation/Implementation of HTTP, FTP, DNS using network simulators. L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Define the network components, layers, addressing, topology, and connectivity and network types for data transmission.

CO2. Distinguish the basic network configurations and standards associated with each network.

CO3. Describe the layering architecture of computer networks and distinguish between the OSI reference model and TCP/IP protocol suite.

CO4. Identify the protocols and functions associated with the transport layer services.

CO5.Construct a network model and determine the routing of packets using different routing algorithms and identify the concepts of Network security.

Suggested Learning Resources:

Text Books:

1: Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

Reference Books

1: James J Kurose, Keith W Ross, "Computer Networks", Pearson Education.

2: Wayne Tomasi, "Introduction to Data Communication and Networking", Pearson India, 1st edition.

3: Andrew Tannenbaum, "Computer Networks", Prentice Hall.

4: William Stallings, "Data and Computer Communications", Prentice Hall

Web Links:

https://nptel.ac.in/courses/106105183.

TCP/IP Tutorial and Technical Overview, (IBM Redbook) - Download From http://www.redbooks.ibm.com/abstracts/gg243376.html

TCP/IP Guide, Charles M Kozierok, Available Online - http://www.tcpipguide.com/ Request for Comments (RFC) - IETF - http://www.ietf.org/rfc.html

https://cosmolearning.org/courses/computer-networks-524/video-lectures/

https://www.eecis.udel.edu/~bohacek/videoLectures/ComputerNetworking/ComputerNetworking_v2.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity 1: Implementation of simple networks and various networking protocols and algorithms using simulators like NCTUns / CISCO packet tracer and measurement of various parameters using WireShark

Activity 2: Implementation of simple networks and various networking protocols and algorithms in

C/C++/Python

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	-	**3**	**3**	**3**	-	-	-	-	**3**	**3**	-	-	-	-	-
CO2	-	**3**	**3**	**3**	**3**	-	-	-	**3**	**3**	-	-	**1**	-	-
CO3	-	**3**	**3**	**3**	**3**	-	-	-	**3**	**3**	-	**3**	-	**1**	-
CO4	-	**3**	**3**	**3**	**3**	-	-	-	**3**	**3**	-	**3**	**2**	-	-
CO5	-	**3**	**3**	**3**	**3**	-	-	-	**3**	**3**	-	**3**	**2**	**2**	-

High-3, Medium-2, Low-1

V Semester

MICROWAVE THEORY AND ANTENNA			
Course Code:	21ECT504	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03 Hrs

Course objectives:

1. Understanding the basics of microwave and waveguides.
2. Understanding the concepts of microwave networks, microwave passive devices and semiconductor devices.
3. Understanding microwave tubes, microwave design principles and antenna basics.
4. Understanding the importance of point sources, arrays and radiations from wires.
5. To understand different types of antennas like aperture, reflector, broadband and Microstrip antennas.

Module-1	**08 hrs**

Introduction to Microwaves -History of Microwaves, Microwave Frequency bands, applications of Microwaves, Losses associated with microwave transmission, Concept of Impedance in Microwave transmission.

Waveguides-Rectangular waveguide, Introduction to Circular waveguide (No derivations and Numerical examples), Strip line, Micro strip line. **TEXT 1,2**

Teaching Learning Method:	Chalk and Talk, YouTube videos
RBT Level:	L1, L2

Module-2	**08 hrs**

Microwave Network Analysis - Network parameters for microwave circuits, Scattering Parameters. Microwave Passive devices and semiconductor Devices - Microwave passive devices - Directional Coupler, Power Divider, Magic Tee, Attenuator. Microwave Semiconductor Devices - Gunn Diodes, IMPATT diodes, PIN diodes. **TEXT 1,2**

Teaching Learning Method:	Lecture-based learning and Group learning
RBT Level:	L1, L2

Module-3	**08 hrs**

Microwave Tubes: Klystron- two cavity klystron amplifier and reflex klystron (klystron oscillator) Antenna Basics - Physical concept of radiation, near and far field regions, basic antenna parameters: radiation patterns, beam area, radiation Intensity, beam efficiency, reciprocity, directivity and gain, antenna apertures, effective height, bandwidth ,radiation efficiency, radio communication Link and antenna field zones. **TEXT 1,2,3.4**

Teaching Learning Method:	Lecture-based learning and Group learning
RBT Level:	L1, L2

Module-4	**08 hrs**

Radiations from wires: Short electric dipole, resistance of dipole, Half wave dipole antenna, folded dipole antennas.

Point Sources & their arrays - Arrays, Point source, Power theorem and its application, Examples of power patterns, Field patterns, Phase patterns, Array of isotropic point sources different cases, non-isotropic sources, principle of pattern multiplication, linear arrays of n elements of equal amplitude & spacing, broad side, end fire arrays. **TEXT 3,4**

Teaching Learning Method:	Lecture-based learning and Group learning
RBT Level:	L1, L2, L3

Module-5	**08 hrs**

Aperture and Reflector Antennas- Huygens' principle, Babinet's principle, Radiation from sectoral and pyramidal horns: design concepts, prime-focus parabolic reflector and cassegrain antennas.
Broadband Antennas- Log-periodic and Yagi-Uda antennas, frequency independent antennas, broadcast antennas. Micro strip Antennas- Basic characteristics of micro strip antennas, feeding methods. **TEXT 3,4**

Teaching Learning Method:	Lecture-based learning and Group learning
RBT Level:	L1, L2, L4

Course outcomes:

At the end of the course the student will be able to:

CO1. Identify the microwave frequency band, its applications and different types of waveguides
CO2. Analyse microwave networks, microwave passive devices and semiconductor devices.
CO3. Apply microwave design principle, microwave tubes and antenna basics.
CO4. Be able to analyse the radiation patterns from different types of wires, point sources and their arrays.
CO5. Illustrate and design antennas like aperture, reflector, and broadband. Microstrip antenna.

Suggested Learning Resources:

Text Books:

1. Collin RE. Foundations for microwave engineering. John Wiley & Sons; 2007.
2. Annapurna Das, Sisir K Das, Microwave Engineering, TMH Publication, 2001
3. J.D. Kraus, Antennas and wave propagation, McGraw Hill, 4th ediation 2010.
4. C.A. Balanis, Antenna Theory - Analysis and Design, John Wiley, 1982.

Reference Books

1. Microwave Devices and circuits- Liao / Pearson Education. 1992
2. M.Kulkarni., "Microwave devices and Radar Engg."Umesh Publications, 2011
3. R.E. Collin, Antennas and Radio Wave Propagation, McGraw Hill, 1985.
4. I.J. Bahl and P. Bhartia, Micro Strip Antennas, Artech House, 1980.

Web Links:

1. www.nptel.in
2. https://www.academia.edu/12559664/Collin_Foundations_for_Microwave_Engineering
3. https://www.academia.edu/13759443/Basic_Antennas_Understanding_Practical_Antennas_and_Design_Joel_R_Hallas_2009
4. www.youtube/microwave , www.youtube/antennas

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1: Creating physical modules

2: Exploring new technologies and presenting

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	1												2	
CO2	3	3	2											2	
CO3	3	2	3	2			1					1	2	2	
CO4	3	3	2	2			1					1	2	2	

CO5	3	3	2	2			**1**					**1**	**2**	**2**	

High-3, Medium-2, Low-1

V Semester

COMMUNICATION LAB II			
Course Code	**21ECL505**	**CIE Marks**	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	**SEE Marks**	50
Credits	01	**Exam Hours**	03

Course objectives:

This laboratory course enables students to

- Design and demonstrate communication circuits for different digital modulation techniques.
- To simulate Source coding Algorithms using C/C++/ MATLAB code.
- To simulate Error correcting and detecting codes using C/C++/ MATLAB code.
- Simulate the networking concepts and protocols using C/C++/ Network simulation tool.
- Understand entropies and mutual information of different communication channels.

Sl.No.	**Experiments**
	Implement the following using discrete components
1	FSK generation and detection
2	PSK generation and detection
3	DPSK Transmitter and receiver
4	QPSK Transmitter and Receiver
	Implement the following in C/C++/MATLAB/Scilab/Python or any other Suitable software
5	Write a program to encode binary data using Huffman code and decode it.
6	Write a program to encode binary data using a (7,4) Hamming code and decode it.
7	Write a program to encode binary data using a ((3,1,2)/suitably designed) Convolution code and decode it.
8	For a given data, use CRC-CCITT polynomial to obtain the CRC code. Verify the program for the cases a) Without error b) With error
	Implement the following algorithms in C/C++/MATLAB/Network simulator
9	Write a program for congestion control using leaky bucket algorithm.
10	Write a program for distance vector algorithm to find suitable path for transmission.
11	Write a program for flow control using sliding window protocols.
12	Configure a simple network (Bus/star) topology using simulation software **OR** Configure a simple network (Ring/Mesh) topology using simulation software.
	Demonstration Experiments (For CIE)
13	Configure and simulate simple Wireless Local Area network.
14	Simulate the BER performance of (2, 1, 3) binary convolutional code with generator sequences g(1) =(1 0 1 1) and g(2) =(1 1 1 1) on AWGN channel. Use QPSK modulation scheme. Channel decoding is to be performed through Viterbi decoding. Plot the bit error rate versus SNR (dB), i.e. $P_{e,b}$ versus E_b/N_0. Consider binary input vector of size 3 lakh bits. Also find the coding gain.
15	Simulate the BER performance of (7, 4) Hamming code on AWGN channel. Use QPSK modulation scheme. Channel decoding is to be performed through maximum-likelihood decoding. Plot the bit error rate versus SNR (dB), i.e. $P_{e,b}$ versus E_b/N_0. Consider binary input vector of size 5 lakh bits. Use the following parity check matrix for the (7, 4) Hamming code. Also

	find the coding gain. $H = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 0 & 1 \end{bmatrix}$
16	Simulate the BER performance of rate 1/3 Turbo code. Turbo encoder uses two recursive systematic encoders with $G(D) = [1, \frac{1+D^4}{1+D+D^2+D^3+D^4}]$ and pseudo-random interleaver. Use QPSK modulation scheme. Channel decoding is to be performed through maximum a-posteriori (MAP) decoding algorithm. Plot the bit error rate versus SNR (dB), i.e. $P_{e,b}$ versus E_b/N_0. Consider binary input vector of size of around 3 lakh bits and the block length as 10384 bits. Also find the coding gain.

Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

1. Design and test the digital modulation circuits and display the waveforms.
2. To Implement the source coding algorithm using C/C++/ MATLAB code.
3. To Implement the Error Control coding algorithms using C/C++/ MATLAB code.
4. Illustrate the operations of networking concepts and protocols using C programming and network simulators.

Suggested Learning Resources:

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. K Sam Shanmugam, "Digital and analog communication systems", John Wiley India Pvt. Ltd, 1996.
3. Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	2					1	1	1		1	3	3	
CO2	3	3	2					1	1	1		1	3	3	
CO3	3	3	2					1	1	1		1	3	3	
CO4	3	3	2					1	1	1		1	3	3	

` **High-3, Medium-2, Low-1**

V Semester

COMPUTER COMMUNICATION NETWORKS LAB			
Course Code:	21ECL5081	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	0:0:1:0(L - T –P)	**SEE Marks:**	50
Total Hours of Pedagogy:	12	**Total Marks:**	100
Credits:	1	**Exam Hours:**	03

Course objectives:

This course will enable students to:

1. Demonstrate the simulation of few protocols of data link layer and network layer.
2. Demonstrate the network communication between source and destination.
3. Demonstrate the detection and correction of error in data communication.
4. Simulate the configuration and verification of networking devices.

	Syllabus Contents
1	Write a C program to implement Bit Stuffing and DeStuffing. **RBT Level: L2, L3**
2	Write a C program to simulate a Character Stuffing and Destuffing for a given message. **RBT Level: L2, L3**
3	Write a C program to compute a Polynomial Checksum for a given binary data frame. **RBT Level: L2, L3**
4	Write a C program to simulate a Shortest Path Algorithm. **RBT Level: L2, L3**
5	Using TCP/IP Sockets, write a client-server program to make client to communicate with Server using socket programming techniques in python. **RBT Level: L2, L3**
6	Using TCP/IP Sockets, write to program to develop server and client file sharing system using Socket Programming in python. **RBT Level: L2, L3**
	Part B
7	**Configuring and Verifying LAYER 2 Switches**: For a given number of HOSTS, create a network by connecting Networking Devices, Configure and verify the same. Configuration includes HOSTNAME, BANNER, PASSWORD (CONSOLE, TELNET and ENABLE), MANAGEMENT IP and DEFAULT GATEWAY **RBT Level: L2, L3**
8	**Configuring and Verifying VLAN**: Create a network for a given number of HOSTS and Establish a communication between the hosts by connecting Switches, configure them and verify the same. Configuration includes Switch port configuration and encapsulation methods. **RBT Level: L2, L3**
9	**Configuring and Verifying IP Routing**: Using IP routing ,Establish a communication between the hosts by connecting the Network Devices, configure them and verify the same among different networks. Configuration includes: 1. Static Routing 2. Dynamic Routing (RIP/OSPF/EIGRP) **RBT Level: L2, L3**

10	**Configuring DHCP Server on a Router**: Configure DHCP server on a router to assign IP address dynamically to the hosts and verify the same. a. For One Broadcast Domain b. For Many Broadcast Domain **RBT Level: L2, L3**
11	**Configure a mail server**: Configure mail server using Packet tracer. **RBT Level: L2, L3**
12	Demonstration of Serial Communication using (i) RS232 (ii) MODEM COMMUNICATION (iii) FIBER OPTIC COMMUNICATION **RBT Level: L2**
	PART-C
13	[Simulation Case-Study] Dr. AIT is granted a block of addresses starting from 192.168.100.0/24. The Dr. AIT College committee decided to distribute these blocks of addresses to THREE Departments with each department receiving just FOUR Addresses. 1. Design the sub blocks and give the slash notation to each sub block
14	2. Simulate the above case using Cisco-packet Tracer. Note: while simulating Consider the following Constraints: a. Establish a communication within the Departments. b. Only HOD's of each Department can communicate (Single user from each Department) with each other.
15	Configure port security on the interface of the switch for the network topology.

Course outcomes:

At the end of the course the student will be able to:

CO1.Conduct an experiment to simulate various protocols of data link and network layer.

CO2.Configure and verify VLAN and switches.

CO3.Write the program to verify the detection and correction of error.

CO4.Demonstrate the data communication between two systems using the communication kit.

CO5.Write the program to transfer file and establish connection between two devices .

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	-	2	-	3	3	-	-	-	3	3	-	3	2	3	-
CO2	-	2	-	3	3	-	-	-	3	3	-	3	2	3	-
CO3	-	2	-	3	3	-	-	-	3	3	-	3	2	3	-
CO4	-	2	-	3	3	-	-	-	3	3	-	3	2	3	-
CO5	-	2	-	3	3	-	-	-	3	3	-	3	2	3	-

High-3, Medium-2, Low-1

V Semester

COMMUNICATION SIMULINK TOOLBOX			
Course Code:	21ECL5082	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	0:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	13	**Total Marks:**	100
Credits:	01	**Exam Hours:**	03

Course objectives:

- To impart knowledge of simulation software in digital communications
- To develop skills required to build and analyze the performance of various simulated communication systems under different conditions

Sl. No	Experiments
1	Modulation & demodulation of a random binary data stream using 16 – QAM.
2	Bit error rate (BER) improvement using Pulse Shaping on 16 – QAM signal. (Use forward error correction (FEC) coding.)
3	Perform OFDM modulation and obtain time domain and frequency domain plots to show a low rate signal, a high-rate signal, and a frequency selective multipath channel response.
4	(a) Simulate basic OFDM with no cyclic prefix. (b) Perform Equalization, Convolution, and Cyclic Prefix Addition on basic OFDM.
5	OFDM with FFT Based Oversampling - Modify an OFDM+ Cyclic Prefix signal to efficiently output an oversampled waveform from the OFDM modulator.
6	Simulate a basic communication system in which the signal is first QPSK modulated and then subjected to Orthogonal Frequency Division Multiplexing (OFDM).
7	Obtain the scatter plots & eye diagrams of a QPSK signal to visualize the signal behaviour in presence of AWGN.
8	(a) Generate a multiband signal using the Communications Toolbox. (b) Random noise generation using Simulink & display histogram plots of Gaussian, Rayleigh, Rician, and Uniform noise.
9	QPSK Transmitter and Receiver in Simulink.
10	Multipath Fading Channel in Simulink – For example: Simulate QPSK transmission over a • multipath Rayleigh fading channel and • a multipath Rician fading channel.
11	Adjacent and Co-Channel Interference using Simulink. • Use PSK-modulated signals to show the effects of adjacent and co-channel interference on a transmitted signal.
12	Modulation Classification with Deep Learning • Predict Modulation Type Using CNN

Course outcomes:

At the end of the course the student will be able to:

1. Perform sampling, aliasing, filtering, and quadrature modulation through simulation.
2. Plot signal space representation of digital modulation techniques.
3. Design and implement a pulse shape and matched filter to avoid inter-symbol interference and maximize receiver SNR.
4. Demonstrate advanced wireless communication techniques like Multipath fading, CCI etc. and model the same using MATLAB / Simulink

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1															
CO2															
CO3															
CO4															

High-3, Medium-2, Low-1

V Semester

ANTENNA DESIGN & TESTING			
Course Code:	21ECL5083	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	0:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	13	**Total Marks:**	100
Credits:	01	**Exam Hours:**	03

Course objectives:

1. To understand the various antenna parameters.
2. Conduct experiments to study the Radiation pattern of Antennas.
3. Design different types of antenna arrays and study the pattern characteristics (MATLAB)
4. Design of MMIC antennas like Patch Antenna and study the characteristics.

Sl. No	**Experiments**
1	To obtain the radiation pattern of a Yagi-Uda Antenna array and calculate its directivity
2	To obtain the radiation pattern of a Dipole Antenna array and calculate its directivity.
3	To calculate the aperture of a Dipole Antenna.
4	To obtain the near and far fields of a given antenna and compare the fields.
5	To obtain the Radiation pattern of a microstrip antenna.
6	To obtain the resonant frequency of a Yagi-Uda /Dipole antenna.
7	To obtain the bandwidth of a given Antenna.
8	Plot 2-D and 3-D radiation pattern of omnidirectional antenna using MATLAB.
9	Design and implementation of a broadside array using MATLAB.
10	Design and implementation of an endfire array using MATLAB.
	Demonstration Experiments (For CIE)
11	Design of a Patch Antenna using HFSS Software.
12	Design of a dipole Antenna using HFSS Software.

Course outcomes:
At the end of the course the student will be able to:

1. Analyze the radiation pattern and characteristics of antenna
2. Ability to design various antenna
3. Ability to use different software tools to study antenna characteristics
4. Analyze radiation pattern of linear array antennas

Suggested Learning Resources:

1. Antennas and Wave Propagation -John D Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition,
2. McGraw Hill Education, 2013.
3. https://www.mathworks.com/help/antenna/
4. Help and demo files of the HFSS and MATLAB software

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	2											2	2	
CO2	3	3	3										3	3	
CO3	2	2	2	2	3								2	2	
CO4	2	2	2	2									2	2	

High-3, Medium-2, Low-1

V Semester

MICROWAVES TOOLBOX			
Course Code:	21ECL5084	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	0:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	13	**Total Marks:**	100
Credits:	01	**Exam Hours:**	03

Course objectives:

- Identification of microwave components/devices.
- Study basic principles of operation of microwave devices/ components

Sl. No	Experiments
1	V- I Characteristics of Gunn-diode.
2	Study of characteristics of Magic Tee
3	Coupling and Isolation characteristics of microstrip directional coupler.
4	Determination of power division of microstrip power divider.
5	Determination of resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
6	Measurement of frequency, guide wavelength, power and attenuation in a microwave Test bench.
7	Study of characteristics of E plane Tee / H plane Tee.
8	To measure unknown impedance using Smith chart through test bench setup.
9	Measurement of VSWR and reflection coefficient and attenuation in a microwave test bench Setup.
10	Study propagation of wave using rectangular waveguide using MATLAB.
11	Study of impedance matching using MATLAB.
12	To calculate phase and group velocity using MATLAB.

Course outcomes:

At the end of the course the student will be able to:

1. Demonstrate the characteristics of microwave sources.
2. Demonstrate the characteristics of directional coupler
3. Study of microwave measurement procedure.
4. Apply MATLAB toolbox for study of microwaves phenomena.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	**3**	**3**	**2**									**2**	**2**	**2**	
CO2	**3**	**3**	**3**	**3**		**2**						**1**	**2**	**2**	
CO3	**2**	**2**	**2**	**2**	**3**								**2**	**2**	
CO4	**2**	**2**	**2**	**2**									**2**	**2**	

High-3, Medium-2, Low-1

VI Semester

TECHNOLOGICAL INNOVATION MANAGEMENT AND ENTREPRENEURSHIP			
Course Code:	21ECT601	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	52	**Total Marks:**	100
Credits:	04	**Exam Hours:**	03

Course objectives:

1. Understand basic skills of Management.
2. Understand the need for Entrepreneurs and their skills.
3. Identify the Management functions and Social responsibilities.
4. Understand the Ideation Process, creation of Business Model.

Module-1	**08 hrs**

Management: Nature and Functions of Management- Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession
(Selected topics of Chapter 1, Text 1).
Planning: Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making-Meaning, Types and Steps in Decision Making
(Selected topics from Chapters 4 & S, Text 1). L1,L2

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2

Module-2	**07 hrs**

Organizing and Staffing: Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalisation, Committees-Meaning, Types of Committees; Centralization Vs Decentralization of Authority and Responsibility; Staff"mg-Need and Importance, Recruitment and Selection Process
(Selected topics from Chapters 7, 8 & 11, Text 1).
Directing and Controlling: Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication - Meaning, Importance and Purposes of Communication; Leadership-Meaning, Characteristics, Behavioural Approach of Leadership.
(Selected topics from Chapters 15to 18and 9, Text 1).

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2

Module-3	**08 hrs**

Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance
(Selected topics from Chapter 3, Text 1).
Entrepreneurship: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship
(Selected topics from Chapter 2, Text 2).

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2

Module-4	**08 hrs**

Family Business: Role and Importance of Family Business, Contributions of Family Business in India, Stages of Development of a Family Business, Characteristics of a Family-owned Business in India, Various types of family businesses
(Selected topics from Chapter 4, (Page 71-75) Text 2).
Idea Generation and Feasibility Analysis- Idea Generation; Creativity and Innovation; Identification of Business Opportunities; Market Entry Strategies; Marketing Feasibility.
(Selected topics from Chapter 6(Page No. 111-117) & Chapter 7(Page No. 140-142), Text 2)

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	L1, L2

Module-5	**08 hrs**

Business model- Meaning, designing, analyzing and improvising; Business Plan - Meaning, Scope and Need; Financial, Marketing, Human Resource and Production/Service Plan; Business plan Formats; Project report preparation and presentation; Why some Business Plan fails?
(Selected topics from Chapter 8 (Page No 159-164, Text 2)

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2

Course outcomes:

At the end of the course the student will be able to:

CO 1. Understand the fundamental concepts of Management and Entrepre- neurship and opportunities in order to setup a business

CO 2. Identify the various organizations' architecture

CO 3. Describe the functions of Managers, Entrepreneurs and their social responsibilities

CO 4. Understand the components in developing a business plan

CO 5. Recognize the various sources of funding and institutions supporting entrepreneurs.

Suggested Learning Resources:

Text Books:

1. Principles of Management - P.C Tripathi, P.N Reddy, McGraw Hill Education, fYhEdition, 2017. ISBN-13:978-93-5260-5354.

2. Entrepreneurship Development Small Business Enterprises- Poomima MCharantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.

3. Dynamics ofEntrepreneurial Development and Management byVasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.

4. Robert D. Hisrich, Mathew J. Manimala, Michael PPeters and DeanA. Shepherd, "Entrepreneurship", S1h Edition, Tata Mc-Graw HillPublishing Co.Ltd.- New Delhi, 2012

Reference Books:

1. Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, I01h Edition 2016. ISBN- 978-93-392-2286-4.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

-

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3

High-3, Medium-2, Low-1

VI Semester

COMPUTER ORGANIZATION & ARM MICROCONTROLLERS			
Course Code:	21ECT602	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	52	**Total Marks:**	100
Credits:	04	**Exam Hours:**	03

Course objectives:

1. to explain the basic organization of a computer system.
2. to understand functioning of different sub systems, such as processor, Input/output, and memory.
3. to describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.
4. to Program ARM Cortex M3 for different applications.
5. to analyse the Thumb instruction set and different C-Programming concepts.

Module-1	**08 hrs**
Basic Structure of Computers: Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. **Input/Output Organization:** Accessing I/O Devices, Interrupts – Interrupt Hardware, Direct Memory Access, Buses, Interface Circuits, Standard I/O Interfaces – PCI Bus, SCSI Bus, USB. **Text 1**	
Teaching Learning Method: Chalk and Talk, PowerPoint Presentation, YouTube videos **RBT Level:** L1, L2	
Module-2	**08 hrs**
Memory System: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Replacement Algorithms, Performance Considerations. **Basic Processing Unit**: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hard-wired Control, Micro programmed Control. Basic concepts of pipelining, **Text 1**	
Teaching Learning Method: Chalk and Talk, PowerPoint Presentation, YouTube videos **RBT Level:** L1, L2	
Module-3	**08 hrs**
ARM Embedded Systems: Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions. **Text 2**	
Teaching Learning Method: Chalk and Talk, PowerPoint Presentation, YouTube videos **RBT Level:** L1, L2	
Module-4	**08 hrs**
Introduction to the ARM Instruction set: Introduction, Data processing instructions, Load – Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional Execution. **Text 2**	
Teaching Learning Method: Chalk and Talk, Power point presentations, Programming assignments **RBT Level:** L1, L2, L3	
Module-5	**08 hrs**

Introduction to the THUMB instruction set: Introduction, THUMB register usage, ARM – THUMB interworking, Other branch instructions, Data processing instructions, Stack instructions, Software interrupt instructions.

Efficient C Programming: Overview of C Compilers and optimization, Basic C Data types, C looping structures. **Text 2**

Teaching Learning Method:	Chalk and Talk, Power point presentations, Programming assignments
RBT Level:	**RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Conduct the following experiments by writing Assembly Language Program (ALP) using ARM Cortex M3 Registers using an evaluation board/simulator and the required software tool

Sl. No.	Experiments	12 hrs
1.	Write an ALP to find the sum of first 10 integer numbers.	
2.	Write an ALP to calculate the value of the polynomial function.	
3.	Write an ALP to store data in desired Memory location.	
4.	Write a C program to Output the message using UART of LPC1768.	
5.	Write a C Program to interface LED using LPC 1768.	
6.	Write a C Program to interface Relay using LPC 1768.	
7.	Write a C Program for DC motor/Stepper motor rotation using LPC 1768.	
8.	Write a C Program to interface a DAC and generate Triangular and Square waveforms.	
9.	Write a C program to demonstrate the use of an External interrupt in LPC 1768	

Demonstration Experiments (For CIE only not for SEE)

Conduct the following experiments on an ARM CORTEX M3 evaluation board using evaluation version of Embedded 'C' & Keil µvision-4 tool/compiler.

10.	Write a C program to interface a Real Time Clock (RTC) of LPC 1768.
11.	Write a program to read on-chip ADC value and display it on UART terminal using LPC 1768
12.	Write a C program to interface Keypad using LPC 1768.

Course outcomes:

At the end of the course the student will be able to:

CO 1: Understand the basic structure and Input output organization of a computer system.

CO 2: Explain functioning of different sub systems, such as processor, Input/output, and memory.

CO 3: Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.

CO 4: Apply the instruction set to Program ARM Cortex M3 for different applications.

CO5: Analyse Thumb Instruction set and C-Programming Concepts to Program ARM Cortex M3.

Suggested Learning Resources:

Text Books:

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5th Edition, Tata McGraw Hill, 2002. (Listed topics only from Chapters 1, 2, 4, 5, 8).

2. Andrew N Sloss, Dominic System and Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publisher, 1st Edition, 2008

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Programming Assignments / Mini Projects can be given to improve programming skills

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2												3	
CO2	3	2												3	
CO3	3	2												3	
CO4	3	2	2		2		1		1					3	
CO5	3	2	2		2		1		1					3	

High-3, Medium-2, Low-1

VI Semester

VLSI DESIGN AND TESTING			
Course Code:	21ECT603	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	3

Course objectives:

1. Impart knowledge of MOS transistor theory and CMOS technology
2. Learn the operation principles and analysis of inverter circuits.
3. Infer the operation of Semiconductor memory circuits.
4. Demonstrate the concept of CMOS testing.

Module-1	**8 Hrs**
Introduction: A Brief History, MOS Transistors, CMOS Logic (1.1 to 1.4 of TEXT1) **MOS Transistor Theory:** Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (2.1, 2.2, 2.4 and 2.5 of TEXT1).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on transistor working Self-study topics: MOSFET Scaling and Small-Geometry Effects RBT Level: L1, L2, L3
Module-2	**08 Hrs**
Fabrication: CMOS Fabrication and Layout, Introduction, CMOS Technologies, Layout Design Rules, (1.5 and 3.1 to 3.3 of TEXT1). **Delay:** Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths (4.1 to 4.5 of TEXT1, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation, YouTube videos, Videos on fabrication Self-study topics: Layouts of complex design using Euler's method RBT Level: L1, L2, L3
Module-3	**08 Hrs**
Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM) (10.1 to 10.6 of TEXT2)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, PowerPoint Presentation, YouTube videos on Standard cell memory Design Self-study topics: Memory array design RBT Level: L1, L2, L3
Module-4	**08 Hrs**
Faults in digital circuits: Failures and faults, Modelling of faults, **Temporary faults Test generation for combinational logic circuits**: Fault diagnosis of digital circuits, test generation techniques for combinational circuits, Detection of multiple faults in combinational logic circuits. (1.1 to 1.3, 2.1 to 2.3 of TEXT3)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, PowerPoint Presentation, YouTube videos, videos on testing algorithms for test generation Self-study topics: Testable combinational logic circuits RBT Level: L1, L2, L3

Module-5	07 Hrs

Test generation for sequential circuits: Testing of sequential circuits as iterative combinational circuits, state table verification, test generation based on circuits structure, functional fault models, test generation based on functional fault models.

Design of testable sequential circuits: Controllability and Observability, Adhoc design rules, design of diagnosable sequential circuits, The scan path technique, LSSD, Random Access scan technique, partial scan. (4.1 to 4.5, 5.1 to 5.7 of TEXT3)

Teaching Learning Method:	Chalk and talk method/Power point presentation, YouTube videos
RBT Level:	Self-study topics: Memory testing techniques RBT Level: L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.

CO2. Draw the basic gates using the stick and layout diagram with the knowledge of physical design aspects.

CO3. Interpret memory elements along with timing considerations.

CO4. Interpret testing and testability issues in combinational logic design.

CO5. Interpret testing and testability issues in Sequential logic design.

Suggested Learning Resources:

Text Books:

1: "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education. 2015

2: "CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill, 2019.

3: "Digital Circuit Testing and Testability", Lala Parag K, New York, Academic Press, 1997

Reference Books:

1: "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

2: "Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits", Vishwani D Agarwal, Springer, 2002.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1: Model displayed for clear understanding of fabrication process of MOS transistor

2: Practise session can be held to understand the significance of various layers in MOS process, with the help of coloured layouts

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	3		2								1	1	1
CO2	3	3	2										1	1	1
CO3	3	2	1										1	1	1
CO4	3	3	2										1	1	1
CO5	3	2	3										1	1	1

High-3, Medium-2, Low-1

VI Semester

ARTIFICIAL NEURAL NETWORK			
Course Code:	21ECT6041	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	3

Course objectives:

1. To provide a strong foundation of fundamental concepts and structures in Neural Networks.
2. To understand the Analysis of different techniques and algorithms in Neural Networks.
3. To study the concepts of setting parameters and multilayered Networks.
4. To understand the concepts of Prediction, Polynomial Neural Networks.
5. To analyze the Optimization techniques in Neural Networks
6. To enable the student to apply these techniques in applications which involve neural models.

Module-1	**08 hrs**
Introduction, Fundamental concepts and models of Artificial Neural Network, Biological Neural Networks, structure and function of single neuron, neural network architectures, modelling of neural network, Neural learning process.	
Teaching Learning Method: **RBT Level:**	L1, L2

Module-2	**09 hrs**
Supervised Learning for single layer network: Perceptron, linear separability, Perceptron Training Algorithm, Delta rule. Supervised Learning for Multi- layer network: multilevel discrimination, preliminaries, Back propagation, setting parameter values.	
Teaching Learning Method: **RBT Level:**	L1, L2

Module-3	**08 hrs**
Prediction networks: Introduction, Recurrent network, Radial Basis Functions, Polynomial networks: Higher order network, Sigma–pi network, Function link architecture, Pi-sigma network	
Teaching Learning Method: **RBT Level:**	L1, L2

Module-4	**08 hrs**
Unsupervised learning: Winner take all networks. Hamming networks, Maxnet, Simple competitive learning, Hebb rule, Optimization Methods: Hop filed networks, Travelling Sales person problem, Iterated Gradient Descent	
Teaching Learning Method: **RBT Level:**	L1, L2

Module-5	**06 hrs**
Introduction to Neural Network Algorithms- Support Vector Machine, Generative Adversarial Network, Convolutional Neural Network, Machine learning, Deep learning **Case studies on neural network modelling:** Facial Recognition, Stock Market Prediction Weather Forecasting, Voice Recognition	

Teaching Learning Method:	
RBT Level:	L2, L3, L4

Course outcomes:

At the end of the course the student will be able to:

CO1. Understand the basic concepts of Neural Networks.

CO2. Analysis and development of different techniques in neural networks.

CO3. Analysis the concepts of Prediction Networks.

CO4. Understand and analysis of the concepts of Polynomial networks in Artificial

CO5. Use different optimization, machine learning technique for different model and enveloping the application.

Suggested Learning Resources:

Text Books:

1. Kishan Mehrotra, C. K. Mohan, Sanjay Ranka,Penram, "Elements of Artificial Neural Networks", 2007.
2. J. Zurada, Jaico, "Introduction to Artificial Neural Systems", *2003.*
3. Neural Networks A Classroom Approach- Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition 2019
4. Mohamad H Hassoun " Fundamentals of Artificial Neural Networks, PHI 2019 edition

Reference Books

1. Simon Hayking, "Neural Networks: A Comprehensive Foundation",2nd Edition, PHI.
2. Laurene Fausett, "Fundamentals of Neural Networks: Architecture, Algorithms and Applications", Person Education, 2004.

Web Links: nptl.iitm.ac.in

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity 1: Project on Voice recognition system

Activity 2: Stock Market Prediction

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	2	2	1	-	-	2	-	-	-	3	3	3	2
CO2	3	3	2	2	1	-	-	2	-	-	-	3	3	3	2
CO3	3	2	2	2	1	-	-	2	-	-	-	3	3	3	2
CO4	3	3	2	2	2	-	-	2	-	-	-	3	3	3	2
CO5	3	1	1	2	1	-	-	2	-	-	-	3	3	3	2

High-3, Medium-2, Low-1

VI Semester

CRYPTOGRAPHY			
Course Code:	21ECT6042	**CIE Marks:**	40+5+5
Teaching Hours/Week (L:T:P:S):	3: 0: 0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	3	**Exam Hours:**	03

Course objectives:

This course will enable students to:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Information Security with knowledge of mathematical concepts required for cryptography.
- Core Competence: To equip students with a basic foundation of Cryptography by delivering the basics of symmetric key and public key cryptography and design of pseudo random sequence generation technique

Module-1	**08 hrs**
Basic Concepts of Number Theory and Finite Fields: Divisibility and The Division Algorithm Euclidean algorithm, Modular arithmetic, Groups, Rings and Fields, Finite fields of the form GF(p), Polynomial Arithmetic, Finite Fields of the Form GF(2m) (Text 1: Chapter 3)	
Teaching Learning Method:	Chalk and Talk, YouTube videos, Flipped Class Technique Programming on implementation of Euclidean algorithm, multiplicative inverse, Finite fields of the form GF(p), construction of finite field over GF(2m).
RBT Level:	L1, L2, L3
Module-2	**08 hrs**
Introduction: Computer Security Concepts, A Model for Network Security (Text 1: Chapter 1) **Classical Encryption Techniques**: Symmetric cipher model, Substitution techniques, Transposition techniques (Text 1: Chapter 1)	
Teaching Learning Method:	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Programming on Substitution and Transposition techniques. Self-study topics: Security Mechanisms, Services and Attacks.
RBT Level:	L1, L2, L3
Module-3	**08 hrs**
Block Ciphers: Traditional Block Cipher structure, Data encryption standard (DES) (Text 1: Chapter 2: Section1, 2) The AES Cipher. (Text 1: Chapter 4: Section 2, 3, 4) **More on Number Theory**: Prime Numbers, Fermat's and Euler's theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 5)	
Teaching Learning Method:	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of SDES using programming languages like C++/Python/Java/Scilab. Self-study topics: DES S-Box- Linear and differential attacks
RBT Level:	L1, L2, L3
Module-4	**08 hrs**

ASYMMETRIC CIPHERS: Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 1, 3, 4)	
Teaching Learning Method:	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of Asymmetric key algorithms using programming languages like C++/Python/Java/Scilab. Numerical examples on Elliptic Curve Cryptography
RBT Level:	L1, L2, L

Module-5	**08 hrs**

Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16)	
Teaching Learning Method:	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of simple stream ciphers using programming languages like C++/Python/Java/Scilab.
RBT Level:	L1, L2, L3

Course outcomes:

At the end of the course, the student will be able to:

At the end of the course the student will be able to:

1. Explain traditional cryptographic algorithms of encryption and decryption process.
2. Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the data.
3. Apply concepts of modern algebra in cryptography algorithms.
4. Design pseudo random sequence generation algorithms for stream cipher systems.

Suggested Learning Resources:

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.

Reference Books:

1. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003

Weblink:

https://nptel.ac.in/courses/106105031

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1															
CO2															
CO3															
CO4															
CO5															

High-3, Medium-2, Low-1

VI Semester

PYTHON PROGRAMMING			
Course Code:	21ECT6043	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	3	**Exam Hours:**	03

Course objectives:

1. To acquire the fundamentals of Python programming language.
2. To attain an understanding of functions and collection types.
3. To familiarize the concepts of sequence types, data structures, and error handling in Python.
4. To realize the concepts of object-oriented in Python.
5. To get familiarised with the concepts of file handling and regular expressions.

Module-1	**08 hrs**

Introduction: Introducing Python, Setting Up Python in Windows, introducing IDLE.

Parts of Python programming: Identifiers, Variables, Keywords, statements and expressions, variables, operators, datatypes-Built-in datatypes, sequences in Python, indentation, comments, Input and Output statements.

Control Flow - if, if-elif-else, while loop, for loop, infinite loop, break, continue, return, and pass statements.

Teaching Learning Method:	Chalk and Talk, Power Point Presentation
RBT Level:	L1, L2, L3

Module-2	**08 hrs**

Functions - Defining Functions, Calling Functions, positional Arguments, Keyword Arguments, Default Arguments, Variable-length arguments, Recursive Functions, Anonymous Functions, and Function Decorators.

Strings and Lists: Creation, Basic operations, built-in methods, del statement.

Teaching Learning Method:	Chalk and Talk, Power Point Presentation
RBT Level:	L1, L2, L3

Module-3	**08 hrs**

Tuples, and Dictionaries: Creating Tuples, Accessing the Tuple Elements, Basic Operations on Tuples, Operations on Dictionaries, Dictionary methods, using foe loop with dictionaries, converting lists into dictionaries, Converting Strings into Dictionary,

Data Structures in Python: Linked Lists, Stacks, Queues, Deques. Programming Examples.

Exceptions: Errors in a Python Program, Exception Handling, The Except Block, User Defined Exceptions.

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-4	**08 hrs**

Object Oriented Programming in Python: Features of Object -Oriented Programming System (OOPS), Creating a class, The Self Variable, constructor, Types of variables, Namespaces, Types of Methods, passing members of one class to another class, Inner classes.

Inheritance and Polymorphism: Constructors in Inheritance, overriding Super class constructors and methods, The super() method, Types of Inheritance: Single/Multiple, Method Resolution order, Polymorphism, Operator Overloading, Method overloading, Method Overriding. Programming Examples	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-5	**08 hrs**
Files in Python: Types of files, Opening and closing file, Working with Text files, Working with Binary Files, with statements, Pickle in Python, The seek() and tell() methods, Random accessing Binary files, zipping, and unzipping Files, reading and writing to CSV files. **Regular Expressions**: Regular Expression, Sequence Characters in Regular Expression, Quantifiers in Regular Expression, Special Characters in Regular Expression, Using Regular Expression on Files, Retrieving Information from a HTML File.	
Teaching Learning Method:	Chalk and Talk, Power Point Presentation
RBT Level:	L1, L2, L3

Course outcomes:

At the end of the course, the student will be able to:

CO1. Apply the knowledge of Python scripting elements, Python constructs, datatypes, to solve engineering problems.

CO2. Identify the problem to apply the concepts of control structures, functions and error handling to solve them using the Python programming language

CO3. Apply the knowledge of Python and use the language scripting elements to manage the data, build the data structures, and handle errors.

CO4. Designing the solution to real-world problems through object-oriented concepts such as Inheritance, Polymorphism, and operator overloading.

CO5. Demonstrating the concepts of file handling and regular expressions

Suggested Learning Resources:

Text Books:

1: Core Python Programming: Dr. R. Nageshwara Rao, Dream Tech Press,2018

2: Introduction to Python Programming, Gowrishankar S, Veena A, CRC Press,2019

Reference Books:

1: Think Python, Allen Downey, Green Tea Press.

2: Core Python Programming, W.Chun, Pearson.

3: Introduction to Python, Kenneth A. Lambert, Cengage

4: Learning Python, Mark Lutz, Orielly

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity 1: Group activity for a group of 4 or 5 students -5 marks

Activity 2: Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	1	1	1				1					2		
CO2	2	2	3	1	2			1					2		
CO3	2	3	3	2	2			1					2		
CO4	2	3	3	1	2			1					2		
CO5	1	3	2	1	2			1					2		

High-3, Medium-2, Low-1

VI Semester

MICRO ELECTRO MECHANICAL SYSTEMS			
Course Code:	21ECT6044	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3: 0: 0:1	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

1. **Preparation**: To prepare students with fundamental knowledge/ overview in the field of Micro Electro Mechanical Systems.
2. **Core Competence**: To equip students with a basic foundation in electronic engineering, mechanical engineering, electrical engineering, chemistry, physics and mathematics fundamentals required for comprehending the operation and application of MEMS circuits, design.
3. **Professionalism & Learning Environment:** To inculcate in students an ethical and professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context, and life-long learning needed for a successful professional career.

Module 1	**08 hrs**

Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization, Applications and Markets.

Text1:**1.1,1.2,1.3,1.4,1.5,1.6,1.7,1.8,1.9**

Teaching Learning Method:	Chalk and talk method, Animation of MEMS products and applications.
RBT Level:	L1, L2, L3

Module 2	**08 hrs**

Working Principles of Microsystems: Introduction, Microsensors, Micro actuation, MEMS with Micro actuators, Micro accelerometers, Microfluidics.Text**1: 2.1,2.2,2.3,2.4,2.5,2.6**

Engineering Science for Microsystems Design and Fabrication: Introduction, Atomic Structure of Matter, Ions and Ionization Molecular Theory of Matter and Intermolecular Forces, Plasma Physics, Electrochemistry.**Text1: 3.1,3.2,3.3, 3.4, 3.7,3.8**

Teaching Learning Method:	Power Point Presentation, You Tube videos, Animations of MEMS Microsensors, Micro actuators, Micro accelerometers and Microfluidics, molecules, Ions and matter
RBT Level:	L1, L2, L3

Module 3	**08 hrs**

Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.**Text1:4.1,4.2,4.3,4.4,4.5,4.6,4.7**

Teaching Learning Method:	Chalk and talk method, Power Point Presentations and supporting You Tube Videos Solve numerical related to Thin Plates, and Vibration. Self-study topics: solve numerical related to the topics
RBT Level:	L1,L2, L3

Module 4	**08 hrs**

Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling in Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer. **Text1:6.1,6.2,6.3,6.4,6.5,6.6,6.7,6.8**	
Teaching Learning Method:	Chalk and Talk Method, You Tube Videos, Solve numerical related to scaling in Geometry Self-study topics: solve numerical of the topics
RBT Level:	L1, L2, L3

Module 5	**08 hrs**
Overview of Micromanufacturing: Introduction, Bulk Micro manufacturing, Surface Micro machining, The LIGA Process, Summary on Micro manufacturing. **Text1:9.1,9.2,9.3,9.4,9.5** **Microsystem Packaging**: Introduction, Overview of Mechanical Packaging of Microelectronics, Microsystem Packaging. **Text1:11.1,11.2,11.3**	
Teaching Learning Method:	Power Point Presentation, YouTube videos, Animation of MEMS micro manufacturing Supporting animation videos on packaging.
RBT Level:	L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Appreciate the technologies related to Micro Electro- Mechanical Systems.
2. Understand design and fabrication processes involved with MEMS devices.
3. Analyze the MEMS devices and develop suitable mathematical models
4. Understand design of scaling factors in MEMS devices.
5. Know various application areas, mechanical packaging for MEMS devices.

Suggested Learning Resources:

Text Book:

1. Tai-Ran Hsu, MEMS and Microsystems: DesignandManufacture,1st Ed, Tata Mc Graw Hill.

Reference Books:

1. Hans H Gatzen, Volker Saile, JurgLeuthold, Microand Nano Fabrication: Tool sand Processes, Springer, 2015.
2. DilipKumar Bhattacharya, Brajesh Kumar Kaushik, Microelectromechanical Systems (MEMS), Cengage Learning.
3. Chang Liu, Foundations of MEMS, Pearson Ed.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1: Develop mini projects and Final year projects using MEMS components to address the real-world problems

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2											2	3	
CO2	3	3	3		2								3	3	
CO3	3	3	3	2									1	3	
CO4		3	3				2						1	3	
CO5													1	2	

High-3, Medium-2, Low-1

VI Semester

COMMUNICATION ENGINEERING			
Course Code:	**21ECT6051**	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	**3:0:0:0**	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

1. Describe essential elements of an electronic communication system.
2. Understand Amplitude, Frequency & Phase modulations, and Amplitude demodulation.
3. Define the sampling theorem and methods to generate pulse modulations.
4. Learn the various methods of digital modulation techniques and compare the different schemes.
5. Introduce the basic concepts of information theory and coding
6. Understand the basic concepts of wireless and cellular communications.

Module-1	**08 Hrs**
Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, Signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation (Text 1: 1.1 to 1.10)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power Point Presentation Self-study topics: Classification of Signals and systems RBT Level: L1, L2, L3

Module-2	**08 Hrs**
Amplitude Modulation Techniques: Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM, (TEXT 1: 4.1, 4.2, 4.4, 4.6) **Angle Modulation Techniques**: Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation (TEXT1: 5.1, 5.2, 5.5)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method/Power point presentation Self-study topics: DSBSC, SSB and VSB modulation techniques and comparison. RBT Level: L1, L2, L3

Module-3	**08 Hrs**
Sampling Theorem and Pulse Modulation Techniques: Digital Versus Analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals (TEXT 1: 7.2 to 7.8)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method Self-study topics: Differential PCM and Delta Modulation RBT Level: L1, L2, L3

Module-4	**08 Hrs**
Digital Modulation Techniques: Types of digital Modulation, ASK, FSK, PSK, QPSK. (TEXT 1: 9.1 to 9.5) **Information Theory, Source and Channel Coding:** Information, Entropy and its properties, Shannon,-Hartley Theorem, Objectives of source coding, Source coding technique, Shannon source coding theorem, Channel coding theorem, Error Control and Coding. [Text1: 10.1,10.2, 10.11.2, 11.1 to 11.3, 11.8, 11.9, 11.12]	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power Point Presentation.

	Self-study topics: Quadrature Amplitude Modulation, Comparison of Digital Modulation techniques. RBT Level: L1, L2, L3

Module-5	**07 Hrs**

Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next generation networks, Applications of wireless communication (TEXT 2: 1.1 to 1.7)

Principles of Cellular Communications: Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequency reuse distance (TEXT 2: 4.1 to 4.7)

Teaching Learning Method:	Chalk and talk method/Power point presentation
RBT Level:	Self-study topics: Basic propagation mechanisms, Multipath fading. RBT Level: L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Describe the scheme and concepts of radiation and propagation of communication signals through air.

CO2. Understand the AM and FM modulation techniques and represent the signal in time and frequency domain relations.

CO3. Understand the process of sampling and quantization of signals and describe different methods to generate digital signals.

CO4. Describe the basic digital modulation techniques, channel capacity, source coding technique and the channel coding.

CO5. Compare the different wireless communication systems and describe the structure of cellular Communication.

Suggested Learning Resources:

Text Books:

1: T L Singal, Analog and Digital Communications, McGraw Hill Education (India) Private Limited, 2012, 0-07-107269-1

2: T L Singal, Wireless Communications, McGraw Hill Education (India) Private Limited, 2016, ISBN:0-07-068178-3.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Wherever necessary MatLab/Labview tools must be used.

1.Write Matlab Code for the following circuits, observe the waveform

i. AM, FM, QPSK, BPSK, TDM, PWM etc Generation and Demodulation.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	3		2			1	1	1			1	1	1
CO2	3	3	3		3			1	1				1	1	1
CO3	3	3	3		1			1	1				1	1	1
CO4	3	3	3		1			1	1				1	1	1
CO5	3	3	3										1	1	1

High-3, Medium-2, Low-1

VI Semester

MICROCONTROLLERS			
Course Code:	21ECT6052	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

This course will enable students to:

• Understand the difference between a microprocessor and a microcontroller and embedded microcontrollers.
• Familiarize the basic architecture of 8051 micro controller.
• Program 8051microprocessor using Assembly Level Language and C.
• Understand the interrupt system of 8051 and the use of interrupts.
• Understand the operation and use of inbuilt Timers/Counters and the Serial port of 8051.
• Interface 8051 to external memory and I/O devices using its I/O ports.

Module-1	**08 hrs**
8051 Microcontroller: Microprocessor Vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing. **Text2 :** Chapter 1 section 1.1 to 1.3, chapter 3 sections 3.1 to 3.3	
Teaching Learning Method: Chalk and talk method, Power Point Presentation, **RBT Level:** L1, L2, L3	

Module-2	**08 hrs**
8051 Instruction Set: Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Bit manipulation instructions. Simple Assembly language program examples (without loops) to use these instructions. **Text2 :** Chapter 5 , chapter 6, chapter 7, chapter 8	
Teaching Learning Method: Chalk and talk method, Power Point Presentation **RBT Level:** L1, L2, L3	

Module-3	**08 hrs**
8051 Jump and Call instructions & Embedded C Jump and Call Instructions, Calls & Subroutine instructions. Assembly language program examples of subroutines and involving loops. 8051 Programming in C: Data Types and Time delay in 8051 C, I/O programming in 8051 C, Logical Operations in C. **Text2 :** chapter 8 section 8.1 to 8.4.**Text1** : chapter 7 section 7.1 to 7.3	
Teaching Learning Method: Chalk and talk method, Power Point Presentation **RBT Level:** L1, L2, L3	

Module-4	**08 hrs**
8051 Timers and Serial Port 8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode- 2 on a port pin. 8051 Serial Communication- Basics of Serial Data Communication, RS- 232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially.	

Text1: Chapter 9 section 9.1 Chapter 10 section 10.1 to 10.5	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power Point Presentation, L1, L2, L3

Module-5	**08 hrs**

8051 Interrupts and Interfacing Applications.8051 Interrupts. 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a timer interrupt. Interfacing 8051 to ADC-0804, DAC, LCD and Stepper motor and their 8051 Assembly and C language interfacing programming.

Text 1: Chapter 11 section 11.1 and 11.2 Chapter 13 section 13.1 to 13.2, chapter 12 section 12.1, chapter 17 section 17.2

Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power Point Presentation L1, L2, L3

Course outcomes:

At the end of the course, the student will be able to:

CO1. Explain the difference between Microprocessors & Microcontrollers, Architecture of 8051 Microcontroller, Interfacing of 8051 to external memory and instruction set of 8051.

CO2. Develop 8051 Assembly level programs using the 8051-instruction set.

CO3. Develop 8051 Assembly / C language program to generate timings and waveform using 8051 timers, to send & receive serial data using 8051 serial ports.

CO4. Develop 8051 Assembly / C language programs to generate square wave on 8051 I/O port pin using interrupt and C Programme to send & receive serial data using 8051 serial port.

CO5. Interface various peripheral devices to 8051 using I/O ports.

Suggested Learning Resources:

Text Books:

1: Kenneth J. Ayala, "The 8051 Microcontroller", Kenneth J Ayala, 3rd Edition, Thomson/Cengage Learning.

2: Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay, "The 8051 Microcontroller and Embedded Systems – using assembly and C", PHI, 2006 / Pearson, 2006.

Reference Books:

1. "The 8051 Micro controller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.

2. "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

Web Links: https://swayam.gov.in/nd1_noc20_cs25

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity 1:

Activity 2:

Activity 3:

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	3					3	1	2		1	1	2	3
CO2	2	3	3		3			3	1	2		1	1	2	3
CO3	2	3	3		3			3	1	2		1	1	2	3
CO4	2	3	3		3			3	1	2		1	1	2	3
CO5	2	3	3	2	3			3	1	2		1	1	2	3

High-3, Medium-2, Low-1

VI Semester

BASIC VLSI DESIGN			
Course Code:	21ECT6053	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	(L:T:P :: 3:0:0)	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03 hrs

Course objectives:

1. Impart knowledge of MOS transistor theory and CMOS technologies
2. Impart knowledge on architectural choices and performance trade-offs involved in designing and realizing the circuits in CMOS technology
3. Cultivate the concepts of subsystem design processes
4. Demonstrate the concepts of CMOS testing

Module-1	**08 Hrs**
Introduction: A Brief History, MOS Transistors, MOS Transistor Theory, Ideal I-V Characteristics, Nonideal I-V Effects, DC Transfer Characteristics (1.1, 1.3, 2.1, 2.2, 2.4, 2.5 of TEXT2). **Fabrication:** nMOS Fabrication, CMOS Fabrication [P-well process, N-well process, Twin tub process], BiCMOS Technology (1.7, 1.8, 1.10 of TEXT1).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2
Module-2	**08 Hrs**
MOS and BiCMOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout. Basic Circuit Concepts: Sheet Resistance, Area Capacitances of Layers, Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit, Inverter Delays, Driving Large Capacitive Loads (3.1 to 3.3, 4.1, 4.3 to 4.8 of TEXT1).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method/Power point presentation RBT Level: L1, L2, L3
Module-3	**08 Hrs**
Scaling of MOS Circuits: Scaling Models & Scaling Factors for Device Parameters Subsystem Design Processes: Some General considerations, An illustration of Design Processes, Illustration of the Design Processes: Regularity, Design of an ALU Subsystem, The Manchester Carry chain and Adder Enhancement Techniques (5.1, 5.2, 7.1, 7.2, 8.2, 8.3, 8.4.1, 8.4.2 of TEXT1).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3
Module-4	**08 Hrs**
Subsystem Design: Some Architectural Issues, Switch Logic, Gate (restoring) Logic, Parity Generators, Multiplexers, The Programmable Logic Array (PLA) (6.1 to 6.3, 6.4.1, 6.4.3, 6.4.6 of TEXT1). **FPGA Based Systems:** Introduction, Basic concepts, Digital design and FPGAs, FPGA based System design, FPGA architecture, Physical design for FPGAs (1.1 to 1.4, 3.2, 4.8 of TEXT3).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3
Module-5	**07 Hrs**

Memory, Registers and Aspects of system Timing: System Timing Considerations, Some commonly used Storage/Memory elements (9.1, 9.2 of TEXT1).

Testing and Verification: Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability (12.1, 12.1.1, 12.3, 12.5, 12.6 of TEXT 2).

Teaching Learning Method:	Chalk and talk method/Power point presentation
RBT Level:	RBT Level: L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.

CO2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.

CO3. Interpret Memory elements along with timing considerations.

CO4. Demonstrate knowledge of FPGA based system design.

CO5. Interpret testing and testability issues in VLSI Design and analyse CMOS subsystems.

Suggested Learning Resources:

Text Books:

1: "Basic VLSI Design"- Douglas A Pucknell & Kamran Eshraghian, PHI, 3rd Edition.

2: "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.

3: "FPGA Based System Design", Wayne Wolf, Pearson Education, 2004, Technology and Engineering.

Web Links:

https://nptel.ac.in/courses/117101058

https://nptel.ac.in/courses/117106093

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Wherever necessary Cadence/Synopsis/Menta Graphics tools must be used.

1.Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

i. An inverter

ii. A Buffer

iii. Transmission Gate

iv. Basic/universal gates

v. Flip flop -RS, D, JK, MS, T

vi. Serial & Parallel adder

vii. 4-bit counter [Synchronous and Asynchronous counter]

2. Design an op-amp with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:

a. Draw the schematic and verify the following

i) DC Analysis

ii) AC Analysis

iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS

d. Extract RC and back annotate the same and verify the Design

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	3		2								1	1	1
CO2	3	3	2										1	1	1
CO3	3	2	1										1	1	1
CO4	3	3	2										1	1	1
CO5	3	2	3										1	1	1

High-3, Medium-2, Low-1

VI Semester

ELECTRONICS CIRCUITS WITH VERILOG			
Course Code:	21ECT6054	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	(L:T:P :: 3:0:0)	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

1. To understand the basic Verilog HDL design flow.
2. To understand the basic Verilog programming concepts.
3. To describe the simple logic circuits using dataflow, gate-level, and behavioural level modelling.
4. To model digital systems using advanced concepts of Verilog HDL.

Module-1	**08 Hrs**
Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL flow, why Verilog HDL?, trends in HDLs. (Text 1) **Hierarchical Modelling Concepts:** Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. (Text 1)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
Module-2	**08 Hrs**
Basic Concepts: Lexical conventions, datatypes, system tasks, compiler directives. (Text 1) **Modules and Ports:** Module definition, port declaration, connecting ports, hierarchical name referencing. (Text 1)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
Module-3	**08 Hrs**
Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. (Text1) **Dataflow Modeling**: Continuous assignments, delay specification, expressions, operators, operands, operator types. (Text 1)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
Module-4	**08 Hrs**
Behavioral Description: Behavioral Description Highlights, Structure of the HDL Behavioral Description, Sequential Statements, IF Statement, The case Statement , Verilog casex and casez The wait-for Statement. The Loop Statement, For-Loop, While-Loop, Verilog repeat, Verilog forever (content with respect to Verilog only) (Text 2)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
Module-5	**07 Hrs**
Structural Description: Highlights of Structural Description, Organization of Structural Description Binding (4.1, 4.2, 4.3 till example 4.9) (Text 2) **Tasks and Functions:** Differences between tasks and functions, declaration, invocation, automatic tasks and functions. (Text 1)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Understand the Verilog HDL design flow.

CO2. Describe the basic concepts of Verilog HDL programming

CO3. Design of digital electronics circuits using dataflow, behavioural, gate-level, and structural modelling.

CO4. Design complex digital circuits using advanced Verilog concepts.

Suggested Learning Resources:

Text Books:

1: "Verilog HDL: A Guide to Digital Design and Synthesis", Samir Palnitkar, Pearson education, Second edition.

2: "HDL programming (VHDL and Verilog)", Nazeih M Botros, John Wiley India Pvt. Ltd., 2008.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Wherever necessary Xilinx/Model sim, Questa tools must be used.

1.Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

i. An inverter

ii. A Buffer

iii. Transmission Gate

iv. Basic/universal gates

v. Flip flop -RS, D, JK, MS, T

vi. Serial & Parallel adder

vii. 4-bit counter [Synchronous and Asynchronous counter]

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	CO1	3	3	3		2								1	1
CO2	CO2	3	3	2										1	1
CO3	CO3	3	2	1										1	1
CO4	CO4	3	3	2										1	1

High-3, Medium-2, Low-1

VI Semester

SENSORS & ACTUATORS			
Course Code:	21ECE6055	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

- To provide the fundamental knowledge about sensors and measurement system.
- To impart the knowledge of static and dynamic characteristics of instruments and understand the factors in selection of instruments for measurement.
- To discuss the principle, design and working of transducers for the measurement of physical time varying quantities.
- Understand the working of various actuators suitable in industrial process control systems.
- Understand the principle and application of smart sensors.

Module-1

Sensors and measurement system: Sensors and transducers, Classifications of transducers-primary & secondary, active & passive, analog and digital transducers. Smart sensors.

Measurement: Definition, significance of measurement, instruments and measurement systems. mechanical, electrical and electronic instruments. Elements of generalized measurement system with example. Input-output configuration of measuring instruments and measurement systems, methods of correction for interfering and modifying inputs.

Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, More examples relating to applications
RBT Level:	L1, L2, L3

Module-2

Static and Dynamic Characteristics: Static calibration and error calibration curve, accuracy and precision, indications of precision, static error, scale range and scale span, reproducibility and drift, repeatability, signal to noise ratio, sensitivity, linearity, hysteresis, threshold, dead zone and dead time, resolution, signal to noise ratio, factors influencing the choice of transducers/instruments. Dynamic response – Dynamic characteristics, Transfer function of generalized first order system, time constant. Transfer function of generalized second order system, natural frequency and Damping ratio.

Teaching Learning Method:	Chalk and talk method, Power point presentation, VI Lab to demonstrate the characteristics of sensors, More examples relating to applications
RBT Level:	L1, L2, L3

Module-3

Measurement of Temperature: RTD, Thermistor, Thermocouple, laws of thermocouple, Thermopile, AD590.

Measurement of Displacement: Introduction, Principles of Transduction, Variable resistance devices, variable Inductance Transducer, Variable Capacitance Transducer, Hall Effect Devices, Proximity Devices, Digital Transducer.

Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, Virtual instrumentation Lab to demonstrate the characteristics of sensors
RBT Level:	L1, L2, L3

Module-4	
Measurement of Strain: Introduction, Types of Strain Gauges, Theory of operation of resistance strain gauges, Types of Electrical Strain Gauges –Wire gauges, unbounded strain gauges, foil gauges, semiconductor strain gauges (principle, types & list of characteristics only), Strain gauge Circuits – Wheatstone bride circuit, Applications. **Measurement of Force & Torque:** Introduction, Force measuring sensor –Load cells – column types devices, proving rings, cantilever beam, pressductor. Hydraulic load cell, electronic weighing system. Torque measurement: Absorption type, transmission type, stress type & deflection type.	
Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, More examples relating to applications
RBT Level:	L1, L2, L3
Module-5	
Actuators and process control system: Introduction. Block diagram and description of process control system with an example. Introduction, Block diagram of Final control operation, Signal conversions analog, digital, pneumatic signal. Actuators, Control elements. **Electrical actuating systems:** Solid-state switches, Solenoids, Electric Motors- Principle of operation and its application: D.C motors, AC motors, Synchronous Motor, Stepper motors. **Pneumatic Actuators**: Principle and working of pneumatic actuators. (Numerical problems on the topic). **Hydraulic Actuators:** Principle and working of Hydraulic actuators. (Numerical problems on the topic).	
Teaching Learning Method:	Chalk and talk method, Power point presentation, More examples relating to applications
RBT Level:	L1, L2, L3
Course outcomes: **At the end of the course the student will be able to:** **CO1:** Discuss the fundamental concepts related to sensors and measurement, functional elements of measurement system, I/O Characteristics of measurement system. **CO2:** Interpret and analyse the static and dynamic characteristics of instruments. **CO3:** Elucidate the working principle and usage of different transducers for temperature, displacement and level measurement. **CO4:** Discuss the principle and working of different types of actuators used in industrial application. **CO5:** Discuss the principle and working of strain, force and torque measurement	
Suggested Learning Resources: **Text Books:** 1.Electrical and Electronic Measurements and Instrumentation, A K Sawhney, 17th Edition, (Reprint 2004), Dhanpat Rai & Co. Pvt. Ltd., 2004. 2. Instrumentation: Devices and Systems, C S Rangan, G R Sarma, V S V Mani, 2nd Edition (32 Reprint), McGraw Hill Education (India), 2014. 3. Process Control Instrumentation Technology by C D Johnson, 7th Edition, Pearson Education Private Limited, New Delhi 2002.	
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning **Activity 1:** **Activity 2:** **Activity 3:**	

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1															
CO2															
CO3															
CO4															
CO5															

High-3, Medium-2, Low-1

VI Semester

VLSI LAB			
Course Code	21ECL606	**CIE Marks**	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	**SEE Marks**	50
Credits	01	**Exam Hours**	03

Course objectives:

This laboratory course enables students to

1. Design, model, simulate and verify CMOS digital circuits
2. Design layouts CMOS digital circuits
3. Perform physical verification of CMOS digital circuits
4. Perform RTL- flow and understand the stages in ASIC design.

Sl. No.	Experiments
1	DC, Transient analysis of CMOS logic-Universal gates schematic
2	DC, Transient analysis of CMOS full adder schematic
3	DC, Transient analysis of Pass transistor and transmission gates schematic
4	DC, Transient analysis of Sequential circuits schematic 1. Clocked D Latch 2. Master-Slave Edge Triggered Register
5	DRC and LVS analysis of CMOS Inverter layout
6	DRC and LVS analysis of Common Source Amplifier Layout
7	DRC and LVS analysis of Common Drain Amplifier Layout
8	DRC and LVS analysis of Differential Amplifier Layout
09	Synthesis and Simulation of Inverter using Verilog code
10	Synthesis and Simulation of Buffer Verilog code
11	Synthesis and Simulation of Basic/Universal Gate using Verilog code
12	Synthesis and Simulation of JK, MSJK flip-flops using Verilog code

Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

CO1. Design and simulate basic CMOS circuits like different logic structures.

CO2: Design and simulate basic CMOS circuits like inverter, common source amplifier and Differential Amplifier.

CO3: Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list.

CO4: Design and simulate combinational and sequential digital circuits using Verilog HDL.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1															
CO2															
CO3															
CO4															

` **High-3, Medium-2, Low-1**

VI Semester

MINI PROJECT			
Course Code:	21ECM607	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	0:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	26	**Total Marks:**	100
Credits:	02	**Exam Hours:**	03

Course objectives: The student will be able to learn,

1. Identification of problem, formulation and methodology.
2. To gain technical knowledge by literature survey.
3. Justify the technical aspects with a comprehensive and systematic approach.
4. Engineering solutions to meet industrial and societal needs.

Mini Project Guidelines:

The project topic, title and synopsis have to be finalized and submitted to their respective internal guide(s). The detailed Synopsis (approved by the department Project Review Committee) has to be submitted during the 1st week after the commencement of 6th semester.

Formation of Groups:

Students are free to choose their project partners from within the programme or any other programme. The project work is to be carried out by a team of two to four students. Each student in the team must contribute towards the successful completion of the project.

The project may be carried out In-house / Industry / R & D Institution.

Selection of Project Topic:

The topics of the project work must be in the field of respective program. The projects as far as possible should have societal relevance with focus on sustainability.

Course outcomes:

At the end of the course the student will be able to:

CO 1 Acquire knowledge within the chosen domain.
CO 2 Usage of Tools based on the problem.
CO 3 Implement using resource management skills.
CO 4 Demonstrate, Present and Report writing.
CO 5 Exhibit life -long learning & Professional ethics.

Assessment Details (both CIE and SEE):

CIE Assessment:

The following are the weightings given for the various stages of the project.

1. Identification of Problem and Introduction 20%
2. Literature Survey and Identifying Research Gap 20%
3. Methodology, H/W & S/W Specifications 20%
4. Design requirements and Specifications 20%
5. Presentation and Viva voce 20%

SEE Assessment:

The following are the weightages given during Viva Examination.

1. Written presentation of synopsis 10%
2. Presentation/Demonstration of the project 30%
3. Methodology and Experimental Results & Discussion 30%
4. Report 10%
5. Viva Voce 20%

COs	Mapping with Pos

CO1	PO1, PO2, PO5, PO7, PO8, PO9, PO10, PO11
CO2	PO1, PO2, PO5, PO9, PO10, PO11
CO3	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11
CO4	PO1, PO2, PO5, PO6, PO8, PO9, PO10, PO11, PO12
CO5	PO1, PO2, PO5, PO8, PO10, PO11, PO12

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	-	-	2	-	2	1	1	1	1	-	**3**	**2**	**-**
CO2	1	1	-	-	3	-	-	-	2	1	1	-	**2**	**2**	**1**
CO3	1	1	3	3	2	1	1	1	1	1	1	-	**-**	**2**	**2**
CO4	1	1	-	-	1	1	-	3	3	1	2	3	**2**	**2**	**1**
CO5	2	2	-	-	1	-	-	3	-	1	2	3	**1**	**2**	**3**

High-3, Medium-2, Low-1

Semester VI

INNOVATION/ENTREPRENEURSHIP/SOCIETAL INTERNSHIP			
Course Code:	21ECI608	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):		**SEE Marks:**	50
Total Hours of Pedagogy:		**Total Marks:**	100
Credits:	3	**Exam Hours:**	3

Course objectives:

1. Understand the process of applying engineering knowledge to produce product and provide services.
2. Explain the importance of management and resource utilization
3. Comprehend the importance of team work, protection of environment and sustainable solutions.
4. Imbibe values, professional ethics for life long learning.

Guidelines

Research/Industrial Internship - At the End of the sixth / Seventh semester (in two cycles to accommodate all the students of the University) Research/Industrial Internship shall be carried out – Based on industrial/Govt./NGO/MSME/Rural Internship/Innovation/Entrepreneurship. All the students admitted shall have to undergo a mandatory internship of 24 weeks during the vacation of VI/VII semesters. A University Viva-Voce examination shall be conducted during VII/VIII semester and the prescribed credit shall be included in VII/VIII semester. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements. Research internship Students have to take up research internships at Centers of Excellence (CoE) / Study Centers established in the same institute and /or out of the institute at reputed research organizations / Institutes. A research internship is intended to give you the flavour of current research going on on a particular topic/s. The internships serve this purpose. They help students get familiarized with the field, the skill needed the effort amount and kind of effort required for carrying out research in that field.

Industry internships: This is an extended period of work experience undertaken by university/Institute students looking to supplement their degree with professional development. The students are allowed to prepare themselves for the workplace and develop practical skills as well as academic ones. It also helps them learn to overcome unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with "unexpected contingencies" helps students recognize, appreciate, and adapt to organization realities by tempering knowledge with practical constraints.

Those, who have not pursued /completed the internship will be declared as failed and have to complete during subsequent SEE examination after they satisfy the internship requirements.

Course outcomes:

At the end of the course the student will be able to:

CO1. Apply engineering and management principles

CO2. Analyze real-time problems and suggest alternate solutions

CO3. Communicate effectively and work.
CO4. Imbibe the practice of professional ethics and need for lifelong learning.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO11	PO12	PSO1	PSO2	PSO3
CO1		2	3	2		2				1			3		2
CO2				3	2	2		1					1	1	2
CO3					1		2	3	3					2	2
CO4					1		3			2	3		2	3	2
CO5															

High-3,Medium-2, Low-1

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.
(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

Ref. No: AIT /EC /BOS / 467 /2023-24 **Date:** 12-08-2023
3

To
Dean (Academic)
Dr Ambedkar Institute of Technology
Bengaluru-56

Sir,

Sub: Regarding the details of the BOS meeting held on 12-08-2023

The External BOS 2023-24 meeting was held in blended mode in the department of the Electronics and communication Engineering and through Google meet link: https://meet.google.com/iun-vhbc-tfs on Saturday, 12-08-2023 10:30 am.

The BOS committee has approved the following:

1. NEP based Scheme and I & II semester syllabus of UG Courses of the 2023 Batch Students.
2. NEP based Scheme and III & IV semester syllabus of UG Courses of the 2022 Batch Students.
3. NEP Based Scheme and V & VI semester Syllabus of UG Courses of the 2021 Batch Students.
4. VII & VIII semester Syllabus of UG Courses of the 2020 Batch Students.
5. Skill Lab for 2023 batch students.
6. Scheme and Syllabus of I and II-year PG course.
7. The List of BOE members.
8. The list of Valuers / Examiners.

Thanking you

Tarulipa V Nandy
CHAIRMAN BOS
Dept. of ECE

HOD
Dept. of Electronics and Communication Engg.
Dr. Ambedkar Institute of Technology
Bengaluru - 560056

Enclosures:

1. List of Members of BOS.
2. Curriculum Design –UG
3. Minutes of the BOS Meeting.
4. Scheme & Syllabus of I/II Semester Basic Electronics and Communication Engineering for the academic year 2023-24.
5. Scheme & Syllabus of 3rd and 4th Semesters for the academic year 2023-24.
6. Scheme & Syllabus of 5th and 6th Semesters for the academic year 2023-24.
7. Scheme & Syllabus of 7th and 8th Semesters for the academic year 2023-24.
8. List of BOE Members.
9. List of valuers / Examiners.

Members of BOS:

Sl No.	*CATEGORY*	*Nomination of the Committee*	*Name of the Person with Designation*
1	Head of the Department	**Chairperson**	Dr. Mahalinga V Mandi, Dean (P&D), Professor & Head, Department of ECE, Dr. AIT, Bengaluru-56
2	Faculty Members at Different Levels Bearing Different Specializations	**Member 1.**	Dr. Umadevi H. Professor, Department of ECE, Dr. AIT, Bengaluru-56
		Member 2.	Dr. Ramesh S, Dean (Exam), Professor, Department of ECE, Dr. AIT, Bengaluru-56
		Member 3.	Smt. Sudha B S. Associate Professor, Department of ECE, Dr. AIT, Bengaluru-56
		Member 4.	Dr. Shivaputra Assistant Professor Department of ECE, Dr. AIT, Bengaluru-56
		Member 5.	Dr. Meenakshi.L.R. Assistant Professor, Department of ECE, Dr. AIT, Bengaluru-56
		Member 6.	Mr. Mohan Kumar V Assistant Professor, Department of ECE, Dr. AIT, Bengaluru-56
		Member 7.	Dr. Jambunath S Baligar Associate Professor Department of ECE, Dr. AIT, Bengaluru-56
		Member 8.	Dr. Chetan. S Assistant Professor, Department of ECE, Dr. AIT, Bengaluru-56
3	Subject Experts from outside the College Nominated by Academic Council	**Member 1.**	Dr. Devendra Jalihal Professor, EEE department IIT Madras, Chennai-600 036

		Member 2.	Prof. Santanu Mahapatra Professor, Department of Electronic Systems Engineering, Indian Institute of Science Bangalore, Bengaluru- 560012
		Member 3.	Dr. Mandeep Singh Professor, Department of ECE, NITK, Surathkal
		Member 4.	Prof. P.Nagaraju Associate Professor, Dept. of TCE, RVCE, Bengaluru-560 059
4	Expert from outside College, Nominated by Vice Chancellor (VTU)	**VTU Nominee**	Dr. Manajanaik N Professor, Department of ECE, UBDT, Davangere, Karnataka
5	Representative from Industry /Corporate Sector/Allied area related to Placement Nominated by Academic council	**Member 1.**	Mr. Kubendra.K Senior Design Engineer VLSI Group, Samsung India,Outer ring Road, Near Marathahalli, Bengaluru
		Member 2.	Mr. Somshekar H Mobileum India Pvt ltd., Director of Engineering.
		Member 3.	Mr. Sampath Kumar Srinivas Mitel, Senior Staff Software Engineer Manyata Tech Park, Bangalore
6	Post Graduate Meritorious alumnus nominated by Principal	**Member**	Mr. Premkumar M N Senior Manager, Intel, India Bengaluru

Tarakeshwar V. Nandi

CHAIRMAN

BOS Dept. of ECE

HOD

Dept. of Electronics and Communication Engg.,
Dr. Ambedkar Institute of Technology
Bengaluru - 560056

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.
(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

MINUTES OF THE MEETING OF THE BOARD OF STUDIES 2023-24

DATED: Saturday, 12th August 2023

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.
(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

BOS Meeting Notice

Sub: Board of Studies Meeting is convened on 12-08-2023

With reference to the above subject, External Board of Studies Meeting of the department is convened on Saturday, the 12th August 2023 at 10:30 a.m. in Department of ECE for finalizing the scheme and syllabus of UG in B.E. (E & C) and PG, M.Tech in VLSI Design and Embedded Systems for the academic year 2023-24 with the following agenda.

Agenda:

1. Approval of the NEP Scheme and Syllabus of 1st to 8th Semesters B.E (E &C) for the Batch-2023
2. Approval of the NEP Scheme and Syllabus of 3rd to 8th Semester B.E(E & C) for the Batch -2022
3. Approval of the NEP Scheme and Syllabus of 5th to 8th Semester B.E(E & C) for the Batch-2021
4. Approval of the Scheme and Syllabus of 7th to 8th Semester B.E(E & C) for the Batch-2020
5. Approval of Basic IoT Skill Lab for the Batch-2023 students.
6. Approval of the Scheme and Syllabus for the 1st and 2nd Semester PG for the Batch-2023
7. Approval of the Scheme and Syllabus for the 3rd and 4th Semester PG for the Batch-2022.
8. Approval of the courses for the Major, Minor Degree
9. Approval of List of Examiners

Minutes of Board of Studies (BOS) Meeting:

The Meeting of Board of Studies (BOS) for Department of Electronics and Communication Engineering was held on 12-08-2023 at 10:30 a.m. under the Chairmanship of the Dr. Mahalinga V. Mandi, Dean (P&D), Professor and Head, Department of Electronics and Communication Engineering in the department of Electronics and Communication engineering and through Google meet link: https://meet.google.com/iun-vhbc-tfs.

At the very outset, the Chairman welcomed all the Internal and External members of BOS to the meeting and gave a preliminary presentation on the agenda items with reference to the scheme and syllabus of UG and PG for the academic year 2023-24

The chairman along with BOS coordinators gave a detailed presentation of the courses to be offered to the students in both Core and Elective subjects in semester wise at the Under Graduate level and Post Graduate level, also briefed the members about the Curriculum Design of the Department for the UG and PG Courses.

PROCEEDINGS/RESOLUTIONS:

The following are the Suggestions of the members of BOS with reference to the presentations:

I and II semester for 2023 batch:

- Subject Expert Devendra Jalihal Suggested to reduce the syllabus for "Basic electronics" (Module 1) for ECE
  Sol. Internal BOS members clarified that most of the topics will be dealt up to Remembering & Understand level (L1, L2)

- Subject Expert Mandeep Singh suggested to include recent edition text books for the course Introduction to Electronics Engineering (22EST104C/204C).
  Sol. Recent edition text books prescribed for subject Introduction to Electronics Engineering (22EST104C/204C).

III and IV Semesters for 2022 batch:

- Subject Expert Devendra Jalihal suggested to rearrange the contents of the topic Fourier Transforms in the subject "Signals and Systems".
  Sol. Topic Fourier Transforms in the subject "Signals and Systems" is rearranged as per the suggestions.

- Subject Expert Dr. Nagaraju P remarked regarding the IPCC subject Analog Electronic Circuits (21ECT303) that JFET experiment was added in practical component while only concepts of MOSFET were dealt in theory.
  Sol. JFET experiments in practical component is replaced by MOSFET experiments.

- Subject Expert Dr. Nagaraju P suggested to reduce the contents of 7th and 8th experiments in Analog and Digital Electronics Lab (22ECL305).
  Sol. Redundant experiments are removed as per suggestions.

- Subject Expert Dr. Nagaraju P suggested to include Proportional controller concept in module 3 in the IPCC subject Modern Control Systems as these concepts were included in practical component.
  Sol. Proportional Controller Concepts included in module 3.

V and VI Semesters for 2021 batch:

- Industry Expert Sampath Kumar Srinivas seek clarification regarding the duration for mini project.
- Industry Expert Sampath Kumar Srinivas suggested to include IPV6 concept in **Computer Communication Networks (21ECT503).**
  Sol. IPV6 concept included as per suggestion.

- Subject Expert Dr. Nagaraju P suggested to include recent edition books for the subject Microwave and Antenna.
  Sol. Prescribed Textbooks updated to recent editions.

- Industry Expert Kubendra suggested to include RISC V concepts in Microprocessor and Microcontroller subject.
  Sol. RISCV concepts included as Module 4 and Module 5 in Microprocessor and Microcontroller subject.

- Subject Expert Dr. Nagaraju P suggested to include Embedded C experiments instead of Assembly Programs in the subject CO & ARM Processor.
  Sol. Assembly Programs replaced with embedded C programs.

- Subject Expert Dr. Nagaraju P suggested to update prescribed text books for the subject ANN
  Sol. Prescribed text books updated to recent editions.

- Discussed about the Scheme and syllabus of 7th and 8th semester for 2020 batch
- No comments on final year subjects, so retained same syllabus.
- Discussed about the Scheme and syllabus of 1st and 2nd year PG program.
- Subject Expert Devendra Jalihal remarked that the number of electives are more.
  Sol. PG coordinator clarified that scheme and syllabus is framed as per VTU guidelines.
- Subject Expert Dr. Nagaraju P suggested to include recent edition text books.
  Sol. Recent edition text books are prescribed.

- The meeting was ended with vote of thanks by Dr. Mahalinga V. Mandi, Dean (P&D), Professor and Head, Department of ECE.

Finally, the BOS members approved the following after incorporating the suggested modifications

- Approved the Curriculum Design for the semesters I to VIII of UG Course for the students of the Batch 2023
- Approved the NEP Based Syllabus of Basic Electronics and Communication Engineering for the semesters I/II of UG Course for the academic year 2023-24.
- Approved the NEP Based Scheme and syllabus for semesters III and IV of UG Course for the academic year 2023-24.
- Approved the NEP Based Scheme and syllabus for semesters V and VI of UG Course for the academic year 2023-24.
- Approved the Scheme and syllabus for semesters VII and VIII of UG Course for the academic year 2023-24.
- Approved Basic IoT Skill Lab for 2023 batch students.
- Approved I and II-year scheme and syllabus of PG Course for academic year 2023-24.
- Approved the courses for the Major, Minor Degree
- Approved the List of BOE members.
- Approved the list of Valuers / Examiners.

Mahalinga V. Mandi

CHAIRMAN

BOS Dept. of ECE

BOS Coordinators	**Signatures**
1. **Prof. B. S. Sudha**	Sudha B S 1/12/2023
2. **Mr. Anand H D**	

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.
(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

List of BOE Members:

SL. NO.	NAME AND ADDRESS
1.	Dr. Mahalinga V. Mandi, Dean (P & D), Professor and Head, Department of ECE
External BOE members:	
1.	Dr. Dinesh P., Professor and Dean, Department of ECE, DSCE, Bengaluru
2.	Prof. Nagraju P, Associate Professor, Department of TCE, RVCE, Bengaluru
3.	Dr. Rajeshwari Hegade, Professor and Head, Department of TCE, BMSCE, Bengaluru-19
4.	Dr. Revanna, Associate Professor, Department of ECE, Govt. Engineering College, Ramanagara
Internal BOE Members:	
1.	Dr. Umadevi H., Professor
2.	Smt. Sudha B. S., Associate Professor
3.	Dr. Shivaputra, Assistant Professor
4.	Smt. Meenakshi L. Rathod, Assistant Professor
5.	Mr. Mohankumar V., Assistant Professor
6.	Smt. Girija S., Assistant Professor

Mahalinga V. Mandi

CHAIRMAN

BOS, Dept. of ECE

HOD

Dept. of Electronics and Communication Engg.
Dr. Ambedkar Institute of Technology
Bengaluru - 560056

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY

(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

12-08-2023

Attendance list:

Sl. No	Position	Name		Signature with date
1.	Chairman	**Dr. Mahalinga V. Mandi** Professor and Head Department of ECE, Dr. AIT, Bengaluru-56		Mahalinga V. Mandi 12/8/23
2.	VTU Nominee	**Dr. Manajanaik N** Professor, Department of ECE, UBDT, Davangere, Karnataka		ABSENT
3.	External Subject Experts	1.	**Dr. Devendra Jalihal** Professor, EEE department IIT Madras, Chennai-600 036	Present Online.
		2.	**Dr. Santanu Mahapatra** Professor, Department of Electronic Systems Engineering, Indian Institute of Science Bangalore,560012	ABSENT
		3.	**Dr. Mandeep Singh** Professor, Department of ECE, NITK, Surathkal	Present Online.
		4.	**Dr. P. Nagaraju** Associate Professor, Dept. of TCE, RVCE, Bengaluru-560 059	P. Nagaraju 12/08/2023
4.	Industry Expert	1.	**Mr. Kubendra K** Senior Design Engineer VLSI Group, Samsung India, Outer ring Road, Near Marathahalli, Bengaluru	Present Online.
		2.	**Mr. Somshekar H** Mobileum India Pvt ltd., Director of Engineering.	ABSENT
		3.	**Mr. Sampath Kumar Srinivas** Mitel, Senior Staff Software Engineer Manyata Tech Park, Bangalore	S. Sampath Kumar 12/8/2023

5.	**Alumni with PG Degree**	**Mr. Premkumar M N** Senior Manager, Intel, India Bengaluru		ABSENT.
6.	**Internal Members**	1.	**Dr. Umadevi H.** Professor, Department of ECE, Dr.AIT, Bengaluru-56	H Umadevi 12/8/2023
		2.	**Dr. Ramesh S.** Professor, Dean (E) Department of ECE, Dr. AIT, Bengaluru-56	12-8-23
		3.	**Smt. Sudha B. S.** Associate Professor, Department of ECE, Dr. AIT, Bengaluru-56	Sudha B.S 12/8/2023.
		4.	**Dr. Shivaputra** Assistant Professor Department of ECE, Dr. AIT, Bengaluru-56	on Leave
		5.	**Dr. Meenakshi L. R.** Assistant Professor, Department of ECE, Dr. AIT, Bengaluru-56	12/08/2023.
		6.	**Mr. Mohan Kumar V.** Assistant Professor, Department of ECE, Dr. AIT, Bengaluru-56	12/08/2023
		7.	**Dr. Jambunath S. Baligar** Associate Professor Department of ECE, Dr. AIT, Bengaluru-56	12/8/23
		8.	**Dr. Chetan S.** Assistant Professor, Department of ECE, Dr. AIT, Bengaluru-56	12/8/23
7.	**Student Representatives:**	1.	Yogesh.N.V 1DA21EC170	Yogeshv
		2.	Yalawathi.V 1DA21EC168	Yalawathi N
		3.	Shulini RR 1DA22EC426	Shulini RR
		4.	LIKHITHA.B 1DA20EC066	Likhitha
		5.	Divyashree.K 1DA20EC041	Diya

		6.	Jagruthi.S 1DA20EC053	Jagruthi
		7.	Spndhu.Hosamani 1DA22LVS03	
		8.	Rashmi.R 1DA22LVS02	Rashmi

Dayalipa V. Nandi 12/8/23

Signature

HOD, Dept. of ECE

BOS Chairman

HOD

Dept. of Electronics and Communication Engg.

Dr. Ambedkar Institute of Technology

Bengaluru - 560056