Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY

(An Autonomous Institute affiliated to VTU, Accredited by NAAC with 'A+' grade)

BDA Outer Ring Road, Mallathalli,Bengaluru-56

Board Of Studies 2023-24

Approved PG Scheme and Syllabus

For

Academic Year (AY) : 2023-24

Submitted by

Department of Electronics and Communication Engineering

To

DEAN (Academic)

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.

(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

Ref. No: AIT /EC /BOS / /2023-24 **Date**: 12-08-2023

To
Dean (Academic)
Dr Ambedkar Institute of Technology
Bengaluru-56

Sir,

Sub: Regarding the details of the BOS meeting held on 102-08-2023

The External BOS 2023-24 meeting was held in blended mode in the department of the Electronics and communication Engineering and through Google meet link: https://meet.google.com/iun-vhbc-tfs on Saturday, 12-08-2023 10:30 am.

The BOS committee has approved the following:

1. NEP based Scheme and I & II semester syllabus of UG Courses of the 2023 Batch Students.
2. NEP based Scheme and III & IV semester syllabus of UG Courses of the 2022 Batch Students.
3. NEP Based Scheme and V & VI semester Syllabus of UG Courses of the 2021 Batch Students.
4. VII & VIII semester Syllabus of UG Courses of the 2020 Batch Students.
5. Skill Lab for 2023 batch students.
6. Scheme and Syllabus of I and II-year PG course.
7. The List of BOE members.
8. The list of Valuers / Examiners.

Thanking you

CHAIRMAN BOS
Dept. of ECE

Enclosures:

1. List of Members of BOS.
2. Curriculum Design –UG
3. Minutes of the BOS Meeting.
4. Scheme & Syllabus of I/II Semester Basic Electronics and Communication Engineering for the academic year 2023-24.
5. Scheme & Syllabus of 3rd and 4th Semesters for the academic year 2023-24.
6. Scheme & Syllabus of 5th and 6th Semesters for the academic year 2023-24.
7. Scheme & Syllabus of 7th and 8th Semesters for the academic year 2023-24.
8. List of BOE Members.
9. List of valuers / Examiners.

Members of BOS:

Sl No.	*CATEGORY*	*Nomination of the Committee*	*Name of the Person with Designation*
1	Head of the Department	**Chairperson**	Dr. Mahalinga V Mandi, Dean (P&D), Professor & Head, Department of ECE, Dr. AIT, Bengaluru-56
2	Faculty Members at Different Levels Bearing Different Specializations	**Member 1.**	Dr. Umadevi H. Professor, Department of ECE, Dr. AIT, Bengaluru-56
		Member 2.	Dr. Ramesh S, Dean (Exam), Professor, Department of ECE, Dr. AIT, Bengaluru-56
		Member 3.	Smt. Sudha B S. Associate Professor, Department of ECE, Dr. AIT, Bengaluru-56
		Member 4.	Dr. Shivaputra Assistant Professor Department of ECE, Dr. AIT, Bengaluru-56
		Member 5.	Dr. Meenakshi.L.R. Assistant Professor, Department of ECE, Dr. AIT, Bengaluru-56
		Member 6.	Mr. Mohan Kumar V Assistant Professor, Department of ECE, Dr. AIT, Bengaluru-56
		Member 7.	Dr. Jambunath S Baligar Associate Professor Department of ECE, Dr. AIT, Bengaluru-56
		Member 8.	Dr. Chetan. S Assistant Professor, Department of ECE, Dr. AIT, Bengaluru-56
3	Subject Experts from outside the College Nominated by Academic Council	**Member 1.**	Dr. Devendra Jalihal Professor, EEE department IIT Madras, Chennai-600 036

		Member 2.	Prof. Santanu Mahapatra Professor, Department of Electronic Systems Engineering, Indian Institute of Science Bangalore, Bengaluru- 560012
		Member 3.	Dr. Mandeep Singh Professor, Department of ECE, NITK, Surathkal
		Member 4.	Prof. P.Nagaraju Associate Professor, Dept. of TCE, RVCE, Bengaluru-560 059
4	Expert from outside College, Nominated by Vice Chancellor (VTU)	**VTU Nominee**	Dr. Manajanaik N Professor, Department of ECE, UBDT, Davangere, Karnataka
5	Representative from Industry /Corporate Sector/Allied area related to Placement Nominated by Academic council	**Member 1.**	Mr. Kubendra.K Senior Design Engineer VLSI Group, Samsung India,Outer ring Road, Near Marathahalli, Bengaluru
		Member 2.	Mr. Somshekar H Mobileum India Pvt ltd., Director of Engineering.
		Member 3.	Mr. Sampath Kumar Srinivas Mitel, Senior Staff Software Engineer Manyata Tech Park, Bangalore
6	Post Graduate Meritorious alumnus nominated by Principal	**Member**	Mr. Premkumar M N Senior Manager, Intel, India Bengaluru

CHAIRMAN

BOS Dept. of ECE

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.
(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

MINUTES OF THE MEETING OF THE BOARD OF STUDIES 2023-24

DATED: Saturday, 12th August 2023

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.
(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

BOS Meeting Notice

Sub: Board of Studies Meeting is convened on 12-08-2023

With reference to the above subject, External Board of Studies Meeting of the department is convened on Saturday, the 12th August 2023 at 10:30 a.m. in Department of ECE for finalizing the scheme and syllabus of UG in B.E. (E & C) and PG in M.Tech in VLSI Design and Embedded Systems for the academic year 2023-24 with the following agenda.

Agenda:

1. Approval of the NEP Scheme and Syllabus of 1st to 8th Semesters B.E (E &C) for the Batch-2023
2. Approval of the NEP Scheme and Syllabus of 3rd to 8th Semester B.E(E & C) for the Batch -2022
3. Approval of the NEP Scheme and Syllabus of 5th to 8th Semester B.E(E & C) for the Batch-2021
4. Approval of the Scheme and Syllabus of 7th to 8th Semester B.E(E & C) for the Batch-2020
5. Approval of Basic IoT Skill Lab for the Batch-2023 students.
6. Approval of the Scheme and Syllabus for the 1st and 2nd Semester PG for the Batch-2023
7. Approval of the Scheme and Syllabus for the 3rd and 4th Semester PG for the Batch-2022.
8. Approval of the courses for the Major, Minor Degree
9. Approval of List of Examiners

Minutes of Board of Studies (BOS) Meeting:

The Meeting of Board of Studies (BOS) for Department of Electronics and Communication Engineering was held on 12-08-2023 at 10:30 a.m. under the Chairmanship of the Dr. Mahalinga V. Mandi, Dean (P&D), Professor and Head, Department of Electronics and Communication Engineering in the department of Electronics and Communication engineering and through Google meet link: https://meet.google.com/iun-vhbc-tfs.

At the very outset, the Chairman welcomed all the Internal and External members of BOS to the meeting and gave a preliminary presentation on the agenda items with reference to the scheme and syllabus of UG and PG for the academic year 2023-24

The chairman along with BOS coordinators gave a detailed presentation of the courses to be offered to the students in both Core and Elective subjects in semester wise at the Under Graduate level and Post Graduate level, also briefed the members about the Curriculum Design of the Department for the UG and PG Courses.

PROCEEDINGS/RESOLUTIONS:

The following are the Suggestions of the members of BOS with reference to the presentations:

I and II semester for 2023 batch:

- Subject Expert Devendra Jalihal Suggested to reduce the syllabus for "Basic electronics" (Module 1) for ECE
  Sol. Internal BOS members clarified that most of the topics will be dealt up to Remembering & Understand level (L1, L2)

- Subject Expert Mandeep Singh **s**uggested to include recent edition text books for the course Introduction to Electronics Engineering (22EST104C/204C).
  Sol. Recent edition text books prescribed for subject Introduction to Electronics Engineering (22EST104C/204C).

III and IV Semesters for 2022 batch:

- Subject Expert Devendra Jalihal suggested to rearrange the contents of the topic Fourier Transforms in the subject "Signals and Systems".
  Sol. Topic Fourier Transforms in the subject "Signals and Systems" is rearranged as per the suggestions.

- Subject Expert Dr. Nagaraju P remarked regarding the IPCC subject Analog Electronic Circuits (21ECT303) that JFET experiment was added in practical component while only concepts of MOSFET were dealt in theory.
  Sol. JFET experiments in practical component is replaced by MOSFET experiments.

- Subject Expert Dr. Nagaraju P suggested to reduce the contents of 7th and 8th experiments in Analog and Digital Electronics Lab (22ECL305).
  Sol. Redundant experiments are removed as per suggestions.

- Subject Expert Dr. Nagaraju P suggested to include Proportional controller concept in module 3 in the IPCC subject Modern Control Systems as these concepts were included in practical component.
  Sol. Proportional Controller Concepts included in module 3.

V and VI Semesters for 2021 batch:

- Industry Expert Sampath Kumar Srinivas seek clarification regarding the duration for mini project.
- Industry Expert Sampath Kumar Srinivas suggested to include IPV6 concept in **Computer Communication Networks (21ECT503)**.
  Sol. IPV6 concept included as per suggestion.

- Subject Expert Dr. Nagaraju P **s**uggested to include recent edition books for the subject Microwave and Antenna.
  Sol. Prescribed Textbooks updated to recent editions.

- Industry Expert Kubendra suggested to include RISC V concepts in Microprocessor and Microcontroller subject.
  Sol. RISCV concepts included as Module 4 and Module 5 in Microprocessor and Microcontroller subject.

- Subject Expert Dr. Nagaraju P **s**uggested to include Embedded C experiments instead of Assembly Programs in the subject CO & ARM Processor.
  Sol. Assembly Programs replaced with embedded C programs.

- Subject Expert Dr. Nagaraju P **s**uggested to update prescribed text books for the subject ANN
  Sol. Prescribed text books updated to recent editions.

- Discussed about the Scheme and syllabus of 7th and 8th semester for 2020 batch
- No comments on final year subjects, so retained same syllabus.
- Discussed about the Scheme and syllabus of 1st and 2nd year PG program.
- Subject Expert Devendra Jalihal remarked that the number of electives are more.
  Sol. PG coordinator clarified that scheme and syllabus is framed as per VTU guidelines**.**
- Subject Expert Dr. Nagaraju P suggested to include recent edition text books.
  Sol. Recent edition text books are prescribed**.**

- The meeting was ended with vote of thanks by Dr. Mahalinga V. Mandi, Dean (P&D), Professor and Head, Department of ECE.

Finally, the BOS members approved the following after incorporating the suggested modifications

- Approved the Curriculum Design for the semesters I to VIII of UG Course for the students of the Batch 2023
- Approved the NEP Based Syllabus of Basic Electronics and Communication Engineering for the semesters I/II of UG Course for the academic year 2023-24.
- Approved the NEP Based Scheme and syllabus for semesters III and IV of UG Course for the academic year 2023-24.
- Approved the NEP Based Scheme and syllabus for semesters V and VI of UG Course for the academic year 2023-24.
- Approved the Scheme and syllabus for semesters VII and VIII of UG Course for the academic year 2023-24.
- Approved Basic IoT Skill Lab for 2023 batch students.
- Approved I and II-year scheme and syllabus of PG Course for academic year 2023-24.
- Approved the courses for the Major, Minor Degree
- Approved the List of BOE members.
- Approved the list of Valuers / Examiners.

CHAIRMAN

BOS Dept. of ECE

BOS Coordinators **Signatures**

1. **Dr. J S Baligar**
2. **Dr. Chetan S**

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.

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Department of Electronics & Communication Engineering

List of BOE Members:

SL. NO.	NAME AND ADDRESS
1.	Dr. Mahalinga V. Mandi, Dean (P & D), Professor and Head, Department of ECE
External BOE members:	
1.	Dr. Dinesh P., Professor and Dean, Department of ECE, DSCE, Bengaluru
2.	Prof. Nagaraju P, Associate Professor, Department of TCE, RVCE, Bengaluru
3.	Dr. Rajeshwari Hegade, Professor and Head, Department of TCE, BMSCE, Bengaluru-19
4.	Dr. Revanna, Associate Professor, Department of ECE, Govt. Engineering College, Ramanagara
5.	Dr. Rohith S, Associate Professor, Department of ECE, NCET, Bengaluru
6.	Dr. Shanthi P, Associate Professor, Department of TCE, RVCE, Bengaluru
Internal BOE Members:	
1.	Dr. Umadevi H., Professor
2.	Dr. J S Baligar, Associate Professor
3.	Dr. Shivaputra, Assistant Professor
4.	Dr. Shilpa K C, Assistant Professor
5.	Dr. Chetan S, Assistant Professor
6.	Mr. Siddesha K, Assistant Professor

CHAIRMAN

BOS Dept. of ECE

Scheme of Syllabus

(2023 Batch)

Dr. Ambedkar Institute of Technology

Scheme of Teaching and Examinations – 2022

M.Tech VLSI Design and Embedded Systems

Choice Based Credit System (CBCS) and Outcome Based Education(OBE)

(Applicable for 2023 Batch)

I SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours per Week			Examination				Credits
				Theory	Practical /Seminar	Tutorial/ Skill Development Activities	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	P	T/SDA					
1	BSC	22LVS11	Mathematical foundation Course	03	00	00	03	50	50	100	3
2	IPCC	22LVS12	Digital System Design Using Verilog	03	02	00	03	50	50	100	4
3	PCC	22LVS13	Digital VLSI design	03	00	02	03	50	50	100	4
4	PCC	22LVS14	VLSI Design Verification and Testing	02	00	02	03	50	50	100	3
5	PCC	22LVS15	Advanced Embedded Systems	02	00	02	03	50	50	100	3
6	MCC	22RMI16	Research Methodology and IPR	03	00	00	03	50	50	100	3
7	PCCL	22LVSL17	VLSI Design and Embedded Systems Lab-I	01	02	00	03	50	50	100	2
8	AUD/AEC	22AUD18/22AEC18	BOS recommended ONLINE courses	Classes and evaluation procedures are as per the policy of the online course providers.							PP
			TOTAL	**17**	**04**	**06**	**21**	**350**	**350**	**700**	**22**

Note: BSC-Basic Science Courses, PCC: Professional core. IPCC-Integrated Professional Core Courses, MCC- Mandatory Credit Course, AUD/AEC –Audit Course / Ability Enhancement Course(A pass in AUD/AEC is mandatory for the award of the degree), PCCL-Professional Core Course lab, OEC-Open Elective Course – Interdisciplinary course which help to learn another area of study and also helps in project work, **L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities**(Hours are for Interaction between faculty and students),

Integrated Professional Core Course (IPCC): **Integrated Professional Core Course (IPCC)**: Refers to Professional Theory Core Course Integrated with practical of the same course. The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.

Audit Courses /Ability Enhancement Courses Suggested by BOS (ONLINE courses): Audit Courses: These are prerequisite courses suggested by the concerned Board of Studies. Ability Enhancement Courses will be suggested by the BoS if prerequisite courses are not required for the programs. **Ability Enhancement Courses**:

- These courses are prescribed to help students to enhance their skills in in fields connected to the field of specialisation as well allied fields that leads to employable skills. Involving in learning such courses are impetus to lifelong learning.
- The courses under this category are online courses published in advance and approved by the concerned Board of Studies.
- Registration to Audit /Ability Enhancement Course shall be done in consultation with the mentor and is compulsory during the concerned semester.
- In case a candidate fails to appear for the proctored examination or fails to pass the selected online course, he/she can register and appear for the same course if offered during the next session or register for a new course offered during that session, in consultation with the mentor.
- The Audit Ability Enhancement Course carries no credit and is not counted for vertical progression. However, a pass in such a course is mandatory for the award of the degree.

Skill development activities: Under Skill development activities in a concerning course, the students should

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.
Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Dr. Ambedkar Institute of Technology

Scheme of Teaching and Examinations – 2022

M.Tech VLSI Design and Embedded Systems

Choice Based Credit System (CBCS) and Outcome Based Education(OBE)

(Applicable for 2023 Batch)

II SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week			Examination				Credits
				Theory	Practical/Seminar	Tutorial/ Skill Development Activities	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	P	T/SDA					
1	PCC	22LVS21	Analog IC Design	02	00	02	03	50	50	100	3
2	IPCC	22LVS22	Embedded OS	03	02	00	03	50	50	100	4
3	PEC	22LVS23X	Professional elective 1	02	00	02	03	50	50	100	3
4	PEC	22LVS24X	Professional elective 2	02	00	02	03	50	50	100	3
5	MPS	22LVS25	Mini Project with Seminar	00	04	02	--	100	--	100	3
6	PCCL	22LVSL26	VLSI Design and Embedded Systems Lab-II	01	02	00	03	50	50	100	02
7	AUD/ AEC	22AUD27	Suggested ONLINE courses	Classes and evaluation procedures are as per the policy of the online course providers.							
			TOTAL	**10**	**08**	**08**	**15**	**350**	**250**	**600**	**18**

Note: BSC-Basic Science Courses, PCC: Professional core. IPCC-Integrated Professional Core Courses, MCC- Mandatory Credit Course, AUD/AEC –Audit Course / Ability Enhancement Course(A pass in AUD/AEC is mandatory for the award of the degree), PCCL-Professional Core Course lab, OEC-Open Elective Course – Interdisciplinary course which help to learn another area of study and also helps in project work, **L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities**(Hours are for Interaction between faculty and students),

Professional Elective 1		Professional Elective 2	
Course Code under 22LVS23X	**Course title**	**Course Code under 22LVS24X**	**Course title**
22LVS231	ASIC design	22LVS241	Algorithms for VLSI Physical Design
22LVS232	Digital IC design	22LVS242	Synthesis and Optimization of Digital Circuits
22LVS233	System Verilog Programming	22LVS243	ARM Programming and Optimization
22LVS234	Multicore Architectures	22LVS244	High Speed VLSI Design
22LVS235	Static Timing Analysis	22LVS245	Design of VLSI systems

Note:

1 Mini Project with Seminar: This may be hands-on practice**,** survey report, data collection and analysis, coding, mobile app development, field visit and report preparation, modelling of system, simulation, analysing and authenticating, case studies, etc.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a senior faculty of the department. Students can present the seminar based on the completed mini-project. Participation in the seminar by all postgraduate students of the program shall be mandatory.

The CIE marks awarded for Mini-Project work and Seminar, shall be based on the evaluation of Mini Project work and Report, Presentation skill and performance in Question and Answer session in the ratio 50:25:25. Mini-Project with Seminar shall be considered as a head of passing and shall be considered for vertical progression as well as for the award of degree. Those, who do not take-up/complete the Mini Project and Seminar shall be declared as fail in that course and have to complete the same during the subsequent semester. There is no SEE for this course.

2. Internship: All the students shall have to undergo a **mandatory internship of 06 weeks during the vacation of II and III semesters**. A University examination shall be conducted during III semester and the prescribed internship credit shall be counted in the same semester. The internship shall be considered as a head of passing and shall be considered for vertical progression as well as for the award of degree. Those, who do not take-up/complete the internship shall be declared as fail in the internship course and have to complete the same during the subsequent University examination after satisfying the internship requirements.

Scheme of Syllabus

2022 Batch

Dr. Ambedkar Institute of Technology

Scheme of Teaching and Examinations – 2022

M.Tech VLSI Design and Embedded Systems

Choice Based Credit System (CBCS) and Outcome Based Education(OBE)

(Applicable for 2022 Batch)

III SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week			Examination				Credits
				Theory	Practical/ Mini-Project/ Internship	Tutorial/ Skill Development Activities	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	P	SDA					
1	PCC	22LVS31	Low Power VLSI design	03	00	02	03	50	50	100	4
2	PEC	22LVS32X	Professional elective 3	03	00	00	03	50	50	100	3
3	OEC	22LVS33X	Open elective Courses-1	03	00	00	03	50	50	100	3
4	PROJ	22LVS34	Project Work phase -1	00	06	00	--	100	--	100	3
5	SP	22LVS35	Societal Project	00	06	00	--	100	--	100	3
6	INT	22LVSI36	Internship	(06 weeks Internship Completed during the intervening vacation of II and III semesters.)			03	50	50	100	6
TOTAL				**09**	**12**	**03**	**12**	**400**	**200**	**600**	**22**

Note: BSC-Basic Science Courses, PCC: Professional core. IPCC-Integrated Professional Core Courses, MCC- Mandatory Credit Course, AUD/AEC –Audit Course / Ability Enhancement Course(A pass in AUD/AEC is mandatory for the award of the degree), PCCL-Professional Core Course lab, OEC-Open Elective Course – Interdisciplinary course which help to learn another area of study and also helps in project work, **L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities**(Hours are for Interaction between faculty and students),

Professional elective 3		Open elective -1	
Course Code under 22LVS32X	**Course title**	**Course Code under 22LVS33X**	**Course title**
22LVS321	Advanced Computer Architecture	22LVS331	Hardware modelling using VHDL
22LVS322	CMOS RF Circuit Design	22LVS332	Pattern Recognition & Machine Learning
22LVS323	Embedded Linux System Design and Development	22LVS333	Internet of Things
22LVS324	SOC Design	22LVS334	High Frequency GaN Electronic Devices
22LVS325	Fin-FETs and Other Multi-Gate Transistors	22LVS335	Advances in Image Processing

Note:

1. **Project Work Phase-1:** The project work shall be carried out individually. However, in case a disciplinary or interdisciplinary project requires more participants, then a group consisting of not more than three shall be permitted.

Students in consultation with the guide/co-guide (if any) in disciplinary project or guides/co-guides (if any) of all departments in case of multidisciplinary projects, shall pursue a literature survey and complete the preliminary requirements of the selected Project work. Each student shall prepare a relevant introductory project document, and present a seminar.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, all Guide/s and co-guide/s (if any) and a senior faculty of the concerned departments. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.

2. Societal Project: Students in consultation with the internal guide as well as with external guide (much preferable) shall involve in applying technology to workout/proposing viable solutions for societal problems.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.

Those, who have not pursued /completed the Societal Project, shall be declared as fail in the course and have to complete the same during subsequent semester/s after satisfying the Societal Project requirements. There is no SEE (University examination) for this course.

3. Internship: Those, who have not pursued /completed the internship, shall be declared as fail in the internship course and have to complete the same during subsequent University examinations after satisfying the internship requirements. Internship SEE (University examination) shall be as per the University norms.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.

Dr. Ambedkar Institute of Technology

Scheme of Teaching and Examinations – 2022

M.Tech VLSI Design and Embedded Systems

Choice Based Credit System (CBCS) and Outcome Based Education(OBE)

(Applicable to 2022 Batch)

IV SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work	Duration in hours	CIE Marks	SEE Marks Viva voce	Total Marks	
				L	P					
1	Project	22LVS41	Project work phase -2	--	08	03	100	100	200	18
			TOTAL	--	**08**	**03**	**100**	**100**	**200**	**18**

Note:

1. Project Work Phase-2:

Students in consultation with the guide/co-guide (if any) in disciplinary project or guides/co-guides (if any) of all departments in case of multidisciplinary projects, shall continue to work of Project Work phase -1to complete the Project work. Each student / batch of students shall prepare project document, and present a seminar.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, all Guide/s and co-guide/s (if any) and a senior faculty of the concerned departments. The CIE marks awarded for project work phase -2, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.

SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check, shall be as per the University norms.

Total Credits 22+18+22+18 = **80**

I Semester Syllabus

(2023 BATCH)

Subject Title**: Mathematical foundation Course**		
Subject Code**: 22LVS11**	No. of Credits**: 03 = 3:0:0 (L:T:P)**	No. of lecture hours per week**: 04**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE **= 40+10+50 =100**	Total No. of lecture hours**: 40**

Course Objective: This course will enable the students:

1. To provide to the students a good understanding of the concepts and methods in linear algebra like vector spaces, orthogonalization and QR decompositions
2. To provide a deep insight into the concepts of probability
3. To study random variables, probability distributions and density functions
4. To study the engineering applications of random variables

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Linear Algebra I:** Introduction to vector spaces and sub-spaces, definitions, illustrative examples and simple problems. Linearly independent and dependent vectors-definition and problems. Basis vectors, dimension of a vector space.	**08**	L1,L2, L3
2	**Linear Algebra II:** Computation of Eigen values and Eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process. QR decomposition, singular value decomposition.	**08**	L1,L2, L3
3	**Probability Theory:** Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, Characteristic functions, probability generating and moment generating functions illustrations. Poisson,GaussianandErlangdistributionsexamples.	**08**	L1,L2, L3
4	**Joint probability distributions:** Definition and properties of Joint CDF, PDF, PMF, conditional distributions. Expectation, covariance and correlation. Independent random variables. Central limit theorem-Illustrative examples	**08**	L1,L2, L3
5	**Random processes:** Random processes. Classification of random processes. Wide sense stationarity. Point processes. Poisson processes. Markov chains. Ergodic random process. Auto correlation function-properties, Gaussian random process. (Blended Learning)	**08**	L1,L2, L3

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After successful completion of the course, the students will be able to:

CO1: Solve a variety of problems including engineering application problems using linear algebra.

CO2: Connect linear algebra to other fields both within and without mathematics.

CO3: Learn the idea of random variables (discrete/continuous) and probability distributions in analysing the probability models arising in control systems and system communications.

CO4: Analyzer and processes through parameter-dependent variables in various random processes Follow complex logical arguments and develop modest logical arguments.
CO5: Demonstrate skills in understanding the mathematical knowledge.

Course outcome and program outcome mapping

CO1: PO1, PO2

CO2: PO1, PO2

CO3: PO1, PO3

CO4: PO1, PO4

CO5: PO1, PO3

TEXT BOOKS:

1. David C. Lay, Linear Algebra and its Applications, Pearson Education (Asia) Pvt. Ltd.
2. Scott L. Miller and Donald Childers, Probability and Random Processes, Academic Press

REFERENCE BOOKS/WEBLINKS:

1. Gilbert Strang, "Linear Algebra and its Applications", 3rd Edition, Thomson Learning Asia, 2003.
2. Kenneth Hoffman and Ray Kunze, "Linear Algebra," 2nd edition, Pearson Education (Asia) Pte. Ltd/ Prentice Hall of India, 2004.
3. A Papoullis and S U Pillai, "Probability, Random Variables and Stochastic Processes", McGraw Hill, 2002
4. Peyton Z Peebles, "Probability, Random Variables and Random Signal Principles", TMH, 4th Edition, 2007.

Subject Title: **DIGITAL SYSTEM DESIGN USING VERILOG**		
Subject Code**: 22LVS12**	No. of Credits**: 04 = 3:2:0 (L:T:P)**	No. of lecture hours per week**: 04**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 50**

Course Learning Objectives

1 Understand digital system design methodologies.

2 Understand usage of Verilog in digital system design.

3 Understand various digital circuits, memory circuits and state logic for control circuits.

5 Understand FPGA design and floating point arithmetic.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**Introduction to Verilog:** Computer-Aided Design, Hardware Description Languages, Verilog Description of Combinational Circuits, Verilog Modules, Verilog Assignments, Procedural Assignments, Modeling Flip-Flops Using Always Block, Always Blocks Using Event Control Statements, Delays in Verilog, Compilation, Simulation, and Synthesis of Verilog Code. **[TEXT 1]**	8	L1,L2,L3
2	**Verilog Data Types and Operators**, Simple Synthesis Examples, Verilog Models for Multiplexers, Modeling Registers and Counters Using Verilog Always Statements, Behavioral and Structural Verilog, Constants, Arrays, Loops in Verilog, Testing a Verilog Model. **Floating-Point Arithmetic**: Representation of Floating-Point Numbers, Floating-Point Multiplication, Floating-Point Addition, Other Floating-Point Operations. **[TEXT 1]**	8	L1,L2 ,L3
3	**Additional Verilog topics**: Verilog Functions, Verilog Tasks, Multivalued Logic and Signal Resolution, Built-in Primitives, User-Defined Primitives, SRAM Model, Rise and Fall Delays of Gates, Named Association, Generate Statements, System Functions, Compiler Directives, File I/O Functions, Timing Checks. **[TEXT 1]**	8	L1,L2, L3,L4
4	**Design Examples**: BCD to 7-Segment Display Decoder, A BCD Adder, 32-Bit Adders, Traffic Light Controller, State Graphs for Control Circuits, Scoreboard and Controller, Synchronization and Debouncing, A Shift-and-Add Multiplier, Array Multiplier, A Signed Integer/Fraction Multiplier, Binary Dividers. **[TEXT 1]**	8	L1,L2, L3,L4
5	**Designing with Field Programmable Gate Arrays**: Implementing Functions in FPGAs, Implementing Functions Using Shannon's Decomposition, Carry Chains in FPGAs, Cascade Chains in FPGAs. **[TEXT 1]**	8	L2,L3, L4.

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Develop a Verilog code for digital circuits/systems
CO2	Develop floating point based arithmetic building blocks for ALU sub-systems.
CO3	Apply advanced Verilog features to develop digital systems.
CO4	Realize the various ALU sub-system blocks using behavioural methodology.
CO5	Implement digital circuits using Field Programmable Gate Arrays.

Course outcome and program outcome mapping

CO1	PO1, PO2
CO2	PO2, PO3, PO4
CO3	PO3, PO4, PO5, PO6
CO4	PO4, PO5, PO6, PO7
CO5	PO5, PO6

TEXT BOOKS:

1. Byeong Kil Lee, Charles H Roth, and Lizy Kurian John, "*Digital Systems Design Using Verilog*", First Edition, Boston, MA : Cengage Learning, 2016.

REFERENCE BOOKS/WEBLINKS:

1. J. Bhaskar, "A Verilog HDL Primer", Third Edition, BS publications, Reprint 2023.
2. Samir Palnitkar, "A Guide to Digital Design and Synthesis", Sun Soft press, Reprint 2003.
3. Peter Ashenden ,"Digital Design: An Embedded Systems Approach Using Verilog", Morgan Kaufmann publishers, Elsvier, Reprint 2010.
4. www.ntpel.com

Session No	**Practical Session**	No of Hours	Blooms Taxonomy Level
1	Develop Verilog code for the multiplication of two unsigned binary numbers and signed binary numbers using the state machine. Verify the program with the help of a test bench.	2	L3, L4.
2	Develop Verilog code for the given sequence generation using the Mealy and More state machine. Verify the program with the help of a test bench.	2	L3, L4.
3	Develop a Verilog code for the division of two binary numbers. Verify the program with the help of a test bench.	2	L3,L4
4	Develop Verilog code for the multiplication of two floating point numbers. Verify the program with the help of a test bench.	2	L3,L4
5	Develop Verilog code for the SRAM model. Verify the program with the help of a test bench.	2	L3, L4.

BOS Chairman Dean(Academics) Principal

Subject Title**: Digital VLSI design**		
Subject Code**: 22LVS13**	No. of Credits**: 04 = 3:2:0 (L:T:P)**	No. of lecture hours per week**: 04**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 50**

Course Learning Objectives: This course will enable the students to:

1. Understand the MOSFET structures (fabrication processes) and operations.
2. Ability to explain VLSI Design Methodologies.
3. Learn Static and Dynamic operation principles, analysis and design of inverter circuit.
4. Concepts and techniques involved in the digital circuits design.
5. Outline the comprehensive coverage of Methodologies and Design practice that are used to reduce the Power Dissipation of large scale digital circuits.
6. Analyze the IC design process.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**MOS Transistor**: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects. **Modelling of MOS Transistor using SPICE:** Basic Concepts, The LEVEL 1 Model Equations, The LEVEL 2 Model Equations ,The LEVEL 3 Model Equations, Capacitance Models, Comparison of the SPICE MOSFET Models, Typical SPICE Model Parameters (from appendix) **[TEXT 1]**	**10**	L1,L2, L3
2	**MOS Inverters-Static Characteristics**: Introduction, Resistive-Load Inverter, Inverters with n Type MOSFET Load. **MOS Inverters-Static Characteristics**: CMOS Inverter. **MOS Inverters**: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitic, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters. **[TEXT 1]**	**10**	L1,L2, L3
3	**COMBINATIONAL MOS LOGIC CIRCUITS :** Introduction MOS Logic Circuits with Depletion nMOS Loads, CMOS Logic Circuits, Complex Logic Circuits ,CMOS Transmission Gates (Pass Gates). **[TEXT 1]**	**10**	L1,L2, L3
4	**SEQUENTIAL MOS LOGIC CIRCUITS**: Introduction, Contents Behavior of Bistable Elements, The SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, CMOS D-Latch and Edge-Triggered Flip-Flop Schmitt Trigger Circuit(Ref Appendix of the chapter). **[TEXT 1]** **Bi-CMOS Logic Circuits**: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs . Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits,BiCMOS Applications. **[TEXT 1]**	**10**	L1,L2, L3
5	**DYNAMIC LOGIC CIRCUITS**: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits. **[TEXT 1]**	**10**	L1,L2, L3, L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Model the MOS transistor (PSPICE model) using the theoretical equations

CO2	Design the CMOS inverter using the specifications
CO3	Design and simulate the combinational logic circuits using the different techniques
CO4	Construct and analyse the transistor level flip flops and latches using the CMOS and BICMOS technology.
CO5	Analyse and model the high performance dynamic CMOS circuits
Course outcome and program outcome mapping	
CO1	PO1,PO2,PO8,PO9,PO10
CO2	PO1, PO2, PO3, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Sung Mo Kang &Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", McGraw-Hill (Third Edition), 2005.

REFERENCE BOOKS/WEBLINKS:

1. Sung Mo Kang &Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", McGraw-Hill (Fourth Edition), 2014.
2. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
3. Wayne, Wolf, "Modern VLSI design: System on Silicon" Pearson Education", Second Edition, 2008.
4. Douglas A Pucknell & Kamran Eshragian , "Basic VLSI Design" PHI 3rd Edition (original Edition – 1994).
5. www.ntpel.com

BOS Chairman Dean(Academics) Principal

Subject Title**:** **VLSI Design Verification and Testing**		
Subject Code**: 22LVS14**	No. of Credits**: 03 = 2:2:0 (L:T:P)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE **= 40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Learn the basics of testing and verification and the role of testing and verification in VLSI design.
2. Able to identify the types of faults and apply the appropriate fault model to detect them.
3. Study of various fault diagnosing techniques and test generation methods.
4. Study of verification tools and simulators.
5. Able to understand the levels of verification and applying the verifying strategies at various levels of VLSI design.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**Introduction to Testing:** Introduction**,** Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing. **Fault Modelling**: Defects errors and faults, Functional versus Structural testing, Levels of fault models, Single stuck-at fault-Fault equivalence, Equivalence of Single Stuck-at Faults, Fault collapsing, Fault dominance and Check point theorem. **Logic and Fault simulation:** Simulation for design verification, simulation for test evaluation, Modelling Circuits for simulation, Algorithms for true value simulation: compiled code simulation, Event driven Simulation, Algorithms for Fault simulation: Serial, Parallel, Deductive, Concurrent fault simulation, Roth's TEST-DETECT algorithm, Differential fault simulation. **[TEXT 2]**	**8**	L1,L2, L3
2	**Test Generation for Combinational logic circuits**: Fault Diagnosis of Digital Systems, Test Generation Techniques for Combinational Logic Circuits, Detection of Multiple Faults in Combinational Logic Circuits. **Test generation for Sequential circuits**: Testing of sequential circuits as Iterative combinational circuits, state table verification, random testing, transition count testing, signature analysis. **[TEXT 1]**	**8**	L1,L2, L3,L4
3	**Design of Testable Sequential Circuits:** What is testability, Controllability and Observability, Design of testable combinational logic Circuits, testable design of sequential circuits, The Scan-Path Technique for Testable Sequential Circuits, Level-Sensitive Scan Design, Random Access Scan Technique, Built-in Test, Design for autonomous self-test, designing testability into logic boards. **[TEXT 1]**	**8**	L1,L2, L3,L4
4	**What is verification**: What is a test bench, The importance of verification, Reconvergence model, what is being verified: Formal verification, Equivalence checking, Model checking, Functional verification, test bench generation, Functional verification approaches: Black-Box verification, White-box verification, Grey-box verification, Testing versus verification: Scan-based testing, design for verification. **Verification Tools:** Linting tools: Limitations of linting tools, linting verilog source code, linting VHDL source code, Code reviews, Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, **[TEXT3]**	**8**	L1,L2, L3
5	**The Verification Plan:** The role of verification plan: specifying the verification plan, defining the first success, Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, Verification strategies: verifying strategies, verifying the response, Random verification, From specifications to features: Component-level features, system-	**8**	L1,L2, L3

	level features, error types to look for, From features to testcases: prioritize, group into testcases, design for verification, from testcases to testbenches: verifying testbenches. **[TEXT3]**		

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Understand the need for testing, testing philosophy; Remember, Apply and Analyse various fault models and different types of simulation techniques.
CO2	Contemplate on various test generation methods applicable to both combinational and sequential logic circuits.
CO3	Understand and Exploit the features of testable design, Scan based techniques, Built-in Test and Autonomous Self-test strategies for today's VLSI design testing.
CO4	Remember and Understand the need for verification, compare it with testing and explain model check, verification approaches and verification tools and simulators.
CO5	Understand and Perform extensive study on verification plan from specification to first time success, random verification and explain about levels of verification and verification strategies.

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4,PO5
CO4	PO7,PO8
CO5	PO3,PO4

TEXT BOOKS:

1. P K Lala**," Fault Tolerant & Fault Testable Hardware Design", B S publications, 2014.**
2. M L Bushnell and V D Agrawal, "**Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits**", First Edition, Kluwar Academic Publishers, New York, 2002.
3. Janick Bergeron, "**Writing Test Benches: Functional Verification of HDL Models**", Second Edition, Kluwar Academic Publishers, 2003.

REFERENCE BOOKS/WEBLINKS:

1. Abramovici M, Breuer M A and Friedman A D, "Digital Systems Testing and Testable Design", Wiley, 1994.
2. P K Lala, "Digital Circuit Testing and Testability", First Edition, Academic Press, 1997.
3. Bhasker J, Chadha and Rakesh, "Static Timing Analysis for Nanometer Designs-A Practical Approach", First Edition, Springer Publications, 2009.
4. Wang, Wu and Wen, "VLSI Test Principles and Architectures", Morgan Kaufmann publishers, 2006.
5. Neil Weste and K. Eshrangian, "Principles of CMOS VLSI Design: A System Perspective," 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
6. https://nptel.ac.in/courses/106103116

Subject Title: **Advanced Embedded Systems**		
Subject Code: **22LVS15**	No. of Credits: **03 = 2:2:0 (L:T:P)**	No. of lecture hours per week: **04**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **40**

Course Learning Objectives: This course will enable the students to:

1. Understand the need of embedded systems.
2. Get exposure to the basic hardware components and their selection methods based on the characteristics and quality attributes of an embedded system.
3. Acquire the knowledge of the ARM based embedded systems, architectural features of ARM Cortex-M processors.
4. Describe the fundamental issues of embedded system design and development.
5. Get exposure to Multi-core architectures of embedded systems.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Embedded System:** Embedded vs General computing system, application and purpose of Embedded System, Core of an Embedded System, Memory, Sensors, Actuators, LED, Optocoupler, keyboard, Communication Interface, Embedded firmware, Other system components, PCB and Passive components, Characteristics and Quality Attributes of Embedded Systems.(TEXT 1)	8	L1,L2, L3,L4
2	**ARM Embedded Systems:** The RISC Design Philosophy, The ARM Design Philosophy, Embedded System Hardware, Embedded System Software. **ARM Processor Fundamentals**: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts, and the Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families. (TEXT2)	8	L1,L2, L3,L4
3	**ARM Cortex-M3/M4 Processors:** ARM Cortex-M processors, Architecture, Instruction Set, ARM Cortex-M3/M4 Processors based MCU (LPC1768 microcontroller). (TEXT 3)	8	L1,L2, L3,L4
4	**Embedded System Design and Development:** Hardware Software Co-Design, embedded firmware design approaches, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Challenges in embedded computing system design, The embedded system design process-Requirements, Specification, Architecture design, Designing hardware and software components, System integration, Design flows. (TEXT 1 & 4)	8	L1,L2, L3,L4
5	**Multi-Core Architectures for Embedded Systems:** Introduction, Architectural Considerations, Interconnection Networks, Software Optimizations, Case Studies: HiBRID-SoC for Multimedia Signal Processing, VIPER Multiprocessor SoC, Defect-Tolerant and Reconfigurable MPSoC, Homogeneous Multiprocessor for Embedded Printer Application, General Purpose Multiprocessor DSP, Multiprocessor DSP for Mobile Applications, Multi-Core DSP Platforms. (TEXT 5)	8	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

	After studying this course, students will be able to:
CO1	Identify the basic building blocks, characteristics and quality attributes of embedded systems.
CO2	Understand the fundamental issues of ARM processor and ARM based embedded systems.
CO3	Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
CO4	Design simple Embedded systems
CO5	Use Multi-core architectures in embedded system design and debugging.
Course outcome and program outcome mapping	
CO1	PO2, PO3, PO4, PO5, PO12
CO2	PO2, PO3, PO4, PO5, PO6, PO12
CO3	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO4	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO5	PO1, PO2, PO3, PO4, PO5, PO6, PO8, PO12

TEXT BOOKS:

1. **Introduction to Embedded Systems,** Shibu K V, Tata McGraw Hill Education, 2009.
2. Sloss Andrew N, Symes Dominic, Wright Chris, "**ARM System Developer's Guide: Designing and Optimizing**", Morgan Kaufman Publication, 2004.
3. Joseph Yiu, **"The Definitive Guide to the ARM Cortex-M3 and Cotrx-M4 Processors"**, Newnes, (Elsevier), 2014.
4. Marilyn Wolf, "**Computers as Components- Principles of Embedded Computing System Design",** Morgan Kaufman Publications, 2017.
5. Georgios Kornaros, **"Multi-Core Embedded Systems",** CRC Press, 2010.

REFERENCE BOOKS/WEBLINKS:

1. "Multicore Programming", Increased Performance through Software Multi–threading by Shameem Akhter and Jason Roberts, Intel Press, 2006.
2. James K Peckol, "Embedded Systems – A Contemporary Design Tool", John Wiley, 2008.
3. Embedded Systems- Architecture, Programming and Design, Raj Kamal, Tata McGraw-Hill, 2008.
4. www.ntpel.com

Course Title: RESEARCH METHODOLOGY AND IPR		
Course Code: **22RM16**		CIE + Assignment + Group Activity + Seminar + SEE Marks = 30 + 10 + 5 + 5 + 50 = 100
Credits: 03		
Hours: 50 Hrs. (L:T:P:S:3:0:0:0)		SEE Duration: 3 Hrs.
Course Learning Objectives:		
1	To make students learn the research methodology and the technique of defining a research problem	
2	To understand the functions of the literature review in research, carrying out a literature search, developing theoretical and conceptual frameworks and writing a review.	
3	To discuss the research designs, sampling designs, measurement and scaling techniques and also different methods of data collections.	
4	To parametric tests of hypotheses and various forms of the intellectual property	

UNIT – I	
Research Methodology: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research, and Problems Encountered by Researchers in India. Defining the Research Problem: Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration.	**10 Hrs**
UNIT – II	
Reviewing the literature: Place of the literature review in research, bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed. Research Design: Meaning of Research Design, Need for Research Design, features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs.	**10 Hrs**
UNIT – III	
Design of Sampling: Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs. Measurement and Scaling: Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement Tools, Scaling, Scale Classification Bases, Scaling Technics, Multidimensional Scaling, Deciding the Scale. Data Collection: Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method.	**10 Hrs**
UNIT – IV	
Testing of Hypotheses: Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule, Procedure for Hypothesis Testing, Hypothesis Testing for Mean, Proportion, Variance, for Difference of Two Mean, for Difference of Two Proportions, for Difference of Two Variances, P-Value approach, Power of Test, Limitations of the Tests of Hypothesis. Chi-square Test: Test of Difference of more than Two Proportions, Test of Independence of Attributes, Test of Goodness of Fit, Cautions in Using Chi Square Tests.	**10 Hrs**
UNIT – V	
Interpretation and Report Writing: Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports. Intellectual Property: The Concept, Intellectual Property	**10 Hrs**

System in India, Development of TRIPS Complied Regime in India, Patents Act, 1970, Trade Mark Act, 1999, The Designs Act, 2000, The Geographical Indications of Goods (Registration and Protection) Act1999, Copyright Act,1957, Conditions on Patent Applicants, Process Patents, Other Use without Authorization of the Right Holder	

Course Outcomes: The students will be able to	
1	Discuss research methodology and the technique of defining a research problem
2	Explain the functions of the literature review in research, carrying out a literature search, developing theoretical and conceptual frameworks and writing a review.
3	Explain various research designs, sampling designs, measurement and scaling techniques and also different methods of data collections. impact in the changing global business environment and leading International Instruments concerning IPR.
4	Explain several parametric tests of hypotheses, Chi-square test, art of interpretation and writing research reports
5	Discuss various forms of the intellectual property, its relevance and business impact in the changing global business environment and leading International Instruments concerning IPR.
Reference Books:	
1	Research Methodology: Methods and Techniques, C.R. Kothari, Gaurav Garg, New Age International, 4 th Edition, 2018.
2	Research Methodology a step-bSy-step guide for beginners. Ranjit Kumar, SAGE Publications, 3 rd Edition, 2011. (For the topic Reviewing the literature under module 2),
3	Study Material, (For the topic Intellectual Property under module 5), Professional Programme Intellectual
4	Property Rights, Law and Practice, The Institute of Company Secretaries of India, Statutory Body Under an Act of Parliament, September 2013

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓			✓
CO2	✓	✓				
CO3	✓		✓	✓	✓	
CO4	✓		✓			
CO5	✓			✓	✓	

Subject Title**:** **VLSI Design and Embedded Systems Lab-I**		
Subject Code**: 22LVSL17**	No. of Credits**: 02 = 0:0:2 (L:T:P)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + SEE = **50+50=100**	Total No. of lecture hours**: 26**

Course Learning Objectives: This course will enable the students to:

1. Design and implementation of basic digital blocks using VERILOG and FPGA Kits.
2. To learn the programming skills in data flow, structural, and behavioural
3. Design of states machines
4. Analyze LPC 1768 MCU
5. Develop assembly and Embedded C programming of ARM Cortex-M3 Processor and Develop 32-bit microcontroller based Embedded system applications

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
	PART A		
VLSI FRONT END DESIGN PROGRAMS:			
1	Write a Verilog code for the following 8 bit adder circuits and implement using chip-scope techniques. 1. Carry Ripple Adder 2. Carry Look Ahead adder 3. Carry Skip Adder 4. BCD Adder & Subtractor	**3**	L3,L4
2	Write a Verilog code for the following 8 bit multiplier circuits and implement using chip-scope techniques. 1. Array Multiplication (Signed and Unsigned) 2. Booth Multiplication (Radix-4)	**3**	L3,L4
3	Write a Verilog code for the following 8/4 circuits and implement using chip-scope techniques. 1. Magnitude Comparator 2. LFSR 3. Parity Generator 4. Universal Shift Register	**3**	L3,L4
4	Write Verilog Code for 3-bit Arbitary Counter to generate 0,1,2,3,6,5,7 and repeats.	**3**	L3, L4
5	Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.	**3**	L3, L4
6	Design a FIFO and LIFO buffers in Verilog and Verify its Operation.	**3**	L3,L4
7	Design a coin operated public Telephone unit using Mealy FSM model with specified operations.	**3**	L3,L4
	PART-B		
	ARM Cortex M3 Programs:		
1	Write an Assembly language program to link multiple object files and link them together.	**3**	L3,L4
2	Write Embedded C program to read on-chip ADC value and display it on terminal of LPC 1768.	**3**	L3,L4
3	Write Embedded C program to interface LED and Relay to LPC 1768 MCU.	**3**	L1,L2, L3,L4

4	Write Embedded C Program to interface RTC to LPC1768.	**3**	L1,L2, L3,L4
5	Write Embedded C program to design a Stopwatch using interrupts.	**3**	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- The internal assessment will be based on Record, Conduction, Question and Answer session.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Design digital circuits for specific applications.
CO2	Verify the digital circuits using chip scope techniques.
CO3	Develop a Verilog code based on states machines.
CO4	Analyze the architecture of ARM Cortex-M3.
CO5	Create different assembly and Embedded C programs.
CO6	Design and testing programs for different embedded applications using LPC1768.

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4
CO4	PO2,PO6
CO5	PO2, PO3, PO4, PO5, PO12
CO6	PO2, PO3, PO4, PO5,PO12

TEXT BOOKS:

1. J. Bhaskar, “A Verilog HDL Primer”, Third Edition, BS publications, Reprint 2023.
2. Samir Palanithkar, “Verilog HDL”, Second Edition, 2012.
3. Joseph Yiu, “The Definitive Guide to the ARM CORTEX-M3”, Second Edition, Newnes, 2008.

REFERENCE BOOKS/WEBLINKS:

1. Byeong Kil Lee, Charles H Roth, and Lizy Kurian John, “*Digital Systems Design Using Verilog*”, First Edition, Boston, MA: Cengage Learning, 2016.

Subject Title**:** **Audit Course / Ability Enhancement Course**		
Subject Code**:** **22AUD18/22AEC18**	No. of Credits**: PP**	No. of lecture hours per week**:**
Exam Duration**: 3 Hours**	CIE + SEE =	Total No. of lecture hours**:**
List of ONLINE Audit Course / Ability Enhancement Courses		
Course Type	**Course Title**	**Duration**
MOOC - Swayam NPTEL	VLSI Interconnects	8 weeks
MOOC - Swayam NPTEL	System Design through Verilog	8 weeks
MOOC - Swayam NPTEL	Hardware modelling using Verilog	8 weeks
MOOC - Swayam NPTEL	Understanding Incubation And Entrepreneurship	12 weeks
MOOC - Swayam NPTEL	C based VLSI design	12 weeks
MOOC - Swayam NPTEL	The Joy of Computing using Python	12 weeks
MOOC - Swayam NPTEL	Semiconductor Devices and Circuits	12 weeks

II Semester Syllabus

(2023 BATCH)

Subject Title: **Analog IC Design**		
Subject Code: **22LVS21**	No. of Credits: **03 = 3:2:0 (L:T:P)**	No. of lecture hours per week: **04**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **40**

Course Learning Objectives: This course will enable the students to:

1. Understand the MOSFET operations in detail.
2. Understand the small signal circuit concepts of MOSFET.
3. Analysis of analog circuits parameters based on the small signal circuits.
4. Applications OP-Amp in an analog building blocks.
5. Design and develop ADC and DAC using different architectures.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Basic MOS Device Physics:** General considerations, MOS I/V Characteristics, second order effects, MOS device models. **Single stage Amplifier:** CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models. **[Text 1]**	**8**	L1,L2, L3
2	**Differential Amplifiers:** Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell. **Passive and active Current mirrors:** Basic current mirrors, Cascade mirrors, active current mirrors. **[Text 1]**	**8**	L1,L2, L3, L4
3	**Frequency response of CS stage:** source follower, Common gate stage, Cascade stage and Difference pair. Noise in CS stage, C- G stage, source follower, cascade stage, differential pair. **[Text 2]**	**8**	L1,L2, L3, L4
4	**Operational Amplifiers:** One Stage OP-Amp. Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, PSRR. Compensation of 2stage OP-Amp, Other compensation techniques. **[Text 2]** **Oscillators:** Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. **PLL:** Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.	**8**	L1,L2, L3, L4
5	**Band gap References** and Switched capacitor filters. **[Text1]** **Chip Input and Output (I/O) Circuits:** Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and its Prevention. [**TEXT 1**]	**8**	L1,L2, L3, L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Model the MOSFET using small signal and large signal analysis
CO2	Design and analyze the CMOS analog circuits.
CO3	Calculate the frequency response of the analog circuits
CO4	Model/synthesis/analyze the OPAMP, OSCILLATORS and PLL circuits
CO5	Understand and design the bandgap reference circuits, switched capacitor filters and chip I/O pad circuits

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3
CO3	PO4,PO5
CO4	PO5,PO6
CO5	PO6,PO7

TEXT BOOKS:

1. Behzad Razavi, **Design of Analog CMOS Integrated Circuits**", TMH, 2007.
2. R. Jacob Baker, "**CMOS Circuit Design, Layout, and Simulation**", Second Edition, Publisher: Wiley-IEEE Press, 1997.
3. Phillip E. Allen, Douglas R. Holberg, **CMOS Analog Circuit Design**, Second Edition, Oxford University Press, 2002.

REFERENCE BOOKS/WEBLINKS:

1. R. Jacob Baker, "**CMOS Circuit Design, Layout, and Simulation**", Third Edition, Publisher: Wiley-IEEE Press, 2010.
2. Philip E. Allen, Douglas R. Holberg, "**CMOS Analog Circuit Design**", Oxford University Press, Third Edition, 2013.
3. nptel.ac.in/courses/117106093/.

Subject Title: **EMBEDDED OS**		
Subject Code**: 22LVS22**	No. of Credits**: 04 = 3:2:0 (L:T:P)**	No. of lecture hours per week**: 04**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 50**

Course Learning Objectives

1 Introduce the fundamental concepts of the OS and real time embedded systems.

2 Apply concepts relating to embedded operating systems such as scheduling techniques, Dynamic priority policies.

3 Describe concepts related to multi resource services like blocking, Deadlock, live lock & soft real-time services.

4 Understand the embedded OS related concepts.

5 Expose to different available RTOS through their case studies.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**Real-Time Systems and Resources:** Brief history of Real Time Systems, A brief history of Embedded Systems. Resource Analysis, Real-Time Service Utility, scheduling classes, Scheduler concepts, OS basics, Types of OS, OS in an embedded device, State transition diagram. (Text 1)	8	L1,L2,L3
2	**Processing with Real Time Scheduling:** Introduction, Pre-emptive Fixed Priority Scheduling Policies with timing diagrams, Problems and issues, Feasibility, Rate Monotonic least upper bound (No derivation), Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies. (Text 1)	8	L1,L2 ,L3
3	**I/O Resources**: Worst case execution time, Execution efficiency, I/O Architecture. **Memory:** Physical hierarchy, Shared Memory, ECC Memory. **Multi-resource Services:** Blocking, Deadlock and livelock, Priority inversion. **Soft real-time services:** Missed deadline, QoS. (Text 1)	8	L1,L2, L3
4	**Embedded OS Concepts:** Tasks, Process and Threads, Process and thread creations, Simple Programs, Semaphores, Mutex, Mailboxes, Message queues, Pipes, Multithreading, Programs related to semaphores, message queue, Examples of Embedded OS. (Text 2)	8	L1,L2, L3
5	**Case Studies:** FreeRTOS, RTLinux, VxWorks, MicroC/OS-II, Embedded Linux, Comparison of available RTOS, Selection criteria of RTOS for an application. (Text 1)	8	L2,L3, L4.

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Discuss the fundamentals of various real time services, real time service utilities, and real time embedded system.
CO2	Apply priority based static and dynamic real time scheduling techniques for the given real time embedded system specifications.
CO3	Analyze deadlock conditions, shared memory problem, priority inversion, missed deadlines and QoS of real time embedded systems. Develop the programs for multithreaded applications using different embedded OS concepts.

	Choose the appropriate available OS to improve the real time embedded system performance.
CO4	Realize the various ALU sub-system blocks using behavioural methodology.
CO5	Implement digital circuits using Field Programmable Gate Arrays.
Course outcome and program outcome mapping	
CO1	PO1, PO2, PO6, PO12
CO2	PO1, PO2, PO4, PO5, PO12
CO3	PO1, PO2, PO6, PO12
CO4	PO1, PO2, PO5, PO6, PO12 PO1, PO2, PO4, PO5, PO6, PO12
CO5	PO5, PO6

TEXT BOOKS:

1. "**Real-Time Embedded Components and Systems",** Sam Siewert, Cengage Learning India Edition, 2007.
2. "**Embedded/Real-time Systems**", Dr K.V.K.K. Prasad, Dreamtech press, 2017.

REFERENCE BOOKS/WEBLINKS:

1. James W S Liu, "**Real Time System**", Pearson education, 2008.
2. Qing Li, "**Real Time Concepts for Embedded Systems**", Elsevier, 2011.
3. Rajkamal, "Embedded Systems- Architecture, Programming, and Design", TMH, 2007.
4. W. Richard Stevens, Stephan A. Rago, "Advanced UNIX Programming", 2nd Edition, Pearson, 2006.
5. Dr. Craig Hollabaugh, "Embedded Linux: Hardware, Software and Interfacing", 1st Edition, Pearson, 2008.
6. nptel.ac.in/courses
7. http://www.FreeRTOS.org

Session No	**Practical Session**	No of Hours	Blooms Taxonomy Level
1	Create periodic, aperiodic and sporadic tasks for different attributes, assign priorities, modify priorities, schedule using RM/EDF/LLF/other algorithm in any online scheduler and analyze the results with respect to CPU utilization and turnaround time.	2	L3, L4.
2	Develop and execute a program using any thread library to create the number of thread specified by the user, each thread independently generates a random integer as an upper limit and then computes and prints the number of primes less than or equal to that upper limit, along with that upper limit.	2	L3, L4.
3	Create multitasking program to demonstrate task synchronization.	2	L3,L4
4	Create multitasking program to demonstrate IPC using mailbox.	2	L3,L4
5	Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.	2	L3, L4.

II

Semester

Professional Elective-1

22LVS23X

Subject Title**: ASIC DESIGN**		
Subject Code**: 22LVS231**	No. of Credits**: 03 = 3:2:0 (L:T:P)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE **= 40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Explain ASIC methodologies and programmable logic cells to implement a function on IC.
2. Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.
3. Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs.
4. Design CAD algorithms and explain how these concepts interact in ASIC design

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**Introduction To ASICs**, Full Custom, Semi-Custom and Programmable ASICS, ASIC Design Flow, ASIC Cell Libraries. **CMOS Logic:** Datapath Logic Cells: Datapath Elements, Adders: Carry Skip, Carry Bypass, Carry Save, Carry Select, Conditional Sum, Multiplier (Booth Encoding), Data Path Operators, I/O Cells.**[TEXT1]**	**8**	L1,L2, L3
2	**ASIC Library Design:** Logical Effort: Predicting Delay, Logical Area and Logical Efficiency, Logical Paths, Multi Stage Cells, Optimum Delay and Number Of Stages. **Programmable ASIC Logic Cells:** MUX as Boolean Function Generators, Actel ACT: ACT 1, ACT 2 And ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX.**[TEXT1]**	**8**	L1,L2, L3
3	**Programmable ASIC I/O Cells:** Xilinx and Altera I/O Block. **Low-Level Design Entry:** Schematic Entry: Hierarchical Design, Netlist Screener. **ASIC Construction:** Physical Design, CAD Tools. **Partitioning:** Goals and Objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead Algorithms. **[TEXT1]**	**8**	L1,L2, L3
4	**Floor Planning and Placement:** Goals and Objectives, Floor Planning Tools, Channel Definition, I/O And Power Planning and Clock Planning. **Placement:** Goals and Objectives, Min-Cut Placement Algorithm, Iterative Placement Improvement, Physical Design Flow. **[TEXT1]**	**8**	L1,L2, L3
5	**Routing:** Global Routing: Goals and Objectives, Global Routing Methods, Back-Annotation. Detailed Routing: Goals and Objectives, Measurement of Channel Density, Left-Edge and Area-Routing Algorithms. Special Routing, Circuit Extraction and DRC. **[TEXT1]**	**8**	L1,L2, L3

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort and FPGA architectures.
CO2	Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow.
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay.

CO4	Understand and identify different Programmable ASIC Logic Cells.
CO5	Create floor plan including partition and routing with the use of CAD algorithms.
Course outcome and program outcome mapping	
CO1	PO1,PO2
CO2	PO2, PO3,PO4,PO5
CO3	PO2,PO3,PO4,PO5
CO4	PO2,PO3, PO4,PO5
CO5	PO3,PO4, PO5,PO6

TEXT BOOKS:

1. Michael John Sebastian Smith, "**Application - Specific Integrated Circuits**" Addison Wesley Professional; 2005.

REFERENCE BOOKS/WEBLINKS:

1. Neil H.E. Weste, David Harris, and Ayan Banerjee, "**CMOS VLSI Design: A Circuits and Systems Perspective**", 3rd edition, Addison Wesley/ Pearson education, 2011.
2. Vikram Arkalgud Chandrasetty,"**VLSI Design: A Practical Guide for FPGA and ASIC Implementations**", Springer, 2011, ISBN: 978-1-4614-1119-2.
3. Rakesh Chadha, Bhasker J., "**An ASIC Low Power Primer**", Springer, 2012, ISBN: 978-1-4614-4270-7.

Subject Title**:** **Digital IC design**		
Subject Code**: 22LVS232**	No. of Credits**: 03 = 2:2:0 (L:T:P)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE **= 40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Learn circuit-oriented approach towards digital design
2. Illustrate the impact of interconnect wiring on the functionality and performance of a digital gate.
3. Infer different approaches to digital timing and clocking circuits
4. Understand the impact of clock skew on the behaviour of digital synchronous circuits
5. Explain the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Implementation Strategies For Digital ICS**: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future.	**8**	L1,L2, L3
2	**Coping With Interconnect**: Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability-Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques, Reduced-Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip.	**8**	L1,L2, L3,L4
3	**Timing Issues In Digital Circuits**: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Latch-Based Clocking, SelfTimed Circuit Design, Self-Timed Logic - An Asynchronous Technique, Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self-Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL.	**8**	L1,L2, L3,L4
4	**Designing Memory and Array Structures**: Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Non-volatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References, Drivers/Buffers, Timing and Control.	**8**	L1,L2, L3, L4
5	**Designing Memory and Array Structures:** Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Data retention dissipation, Case Studies in Memory	**8**	L1,L2, L3, L4

	Design: The Programmable Logic Array (PLA), A 4 Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor Memory Trends and Evolutions.		

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.
CO2	Use the approaches to minimize the impact of interconnect parasitic on performance, power dissipation and circuit reliability
CO3	Impose the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.
CO4	Infer the reliability of the memory
CO5	Solve application specific integrated circuit problems

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4,PO5
CO4	PO7,PO8
CO5	PO3,PO4

TEXT BOOKS:

1. Jan M Rabey, Anantha Chandrakasan, BorivojeNikolic,, **Digital Integrated Circuits-A Design Perspective**, PHI, 2nd Edition, 2003.
2. M. Smith, **Application Specific Integrated circuits**, Addison Wesley, 1997.

REFERENCE BOOKS/WEBLINKS:

1. H. Veendrick, **—MOS IC‘s: From Basics to ASICs**, Wiley-VCH, 1992.

Subject Title**:** **SYSTEM VERILOG PROGRAMMING**		
Subject Code**: 22LVS233**	No. of Credits**: 03 = 3:2:0 (L:T:P)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

This course will enable the students to:

1. Understand digital system verification using object oriented methods
2. Learn the System Verilog language for digital system verification.
3. Create/build test benches for the basic design/methodology.
4. Use constrained random tests for verification
5. Understand concepts of functional coverage

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**Verification Guidelines**: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components. **Data Types**: Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with type def, creating user defined structures, type conversion, Enumerated types, constants and strings, Expression width.	**8**	L1,L2, L3
2	**Procedural Statements and Routines**: Procedural statements, Tasks, Functions and void functions, Task and function overview, Routine arguments, returning from a routine, Local data storage, time values. **Converting the test bench and design**: Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.	**8**	L1,L2, L3
3	**Randomization**: Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Iterative and array constraints, Random control. and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL.	**8**	L1,L2, L3
4	**Threads and Interprocess Communication**: Working with threads, Disabling threads, Interprocess communication, Events, semaphores, Mailboxes, Building a test bench with threads and Interprocess Communication.	**8**	L1,L2, L3
5	**Functional Coverage**: Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.	**8**	L1,L2, L3

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

	After studying this course, students will be able to:
CO1	Write test benches for moderately complex digital circuits.
CO2	Use System Verilog language features to implement digital systems.
CO3	Apply constrained random tests benches using System Verilog.
CO4	Understand building of test bench for threads and interprocess Communication.
CO5	Appreciate functional coverage and coverage strategies.
Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Chris Spear, 'System Verilog for Verification – A guide to learning the Test bench language features', Springer Publications, 2nd Edition, 2010.

REFERENCE BOOKS/WEBLINKS:

1. Stuart Sutherland, Simon Davidmann, Peter Flake, ―System Verilog for Design A guide to using system verilog for Hardware design and modelling, Springer Publications, 2nd Edition, 2006.

Subject Title**:** **Multicore Architectures**		
Subject Code**: 22LVS234**	No. of Credits**: 03 = 3:2:0 (L:T:P)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE **= 40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Provide the knowledge of Multi– core architecture and system overview of threading.
2. Cover fundamental concepts of Parallel programming and its constructs.
3. Describe in detail the concepts of Threading APIs.
4. Get exposure to different concepts of OpenMP.
5. Provide Solutions to common parallel programming problems.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction to Multi– core Architecture:** Motivation for Concurrency in software, Parallel Computing Platforms, Parallel Computing in Microprocessors, Differentiating Multi–core Architectures from Hyper–Threading Technology, Multithreading on Single–Core versus Multi–Core Platforms Understanding Performance, Amdahl's Law, Growing Returns: Gustafson's Law. **System Overview of Threading:** Defining Threads, System View of Threads, Threading above the Operating System, Threads inside the OS, Threads inside the Hardware, What Happens When a Thread Is Created, Application Programming Models and Threading, Virtual Environment: VMs and Platforms, Runtime Virtualization, System Virtualization. (Text: Chapters 1 and 2)	**10**	L1,L2, L3
2	**Fundamental Concepts of Parallel Programming:** Designing for Threads, Task Decomposition, Data Decomposition, Data Flow Decomposition, Implications of Different Decompositions, and Challenges You will Face, Parallel Programming Patterns. **A Motivating Problem:** Error Diffusion, Analysis of the Error Diffusion Algorithm. **An Alternate Approach:** Parallel Error Diffusion, Other Alternatives. **Threading and Parallel Programming Constructs:** Synchronization, Critical Sections, Deadlock, Synchronization Primitives, Semaphores, Locks, Condition Variables, Messages, Flow Control–based Concepts, Fence, Barrier, Implementation dependent Threading Features. (Text: Chapters 3 and 4)	**10**	L1,L2, L3
3	**Threading APIs:** Threading APIs for Microsoft Windows, Win32/MFC Thread APIs, Threading APIs for Microsoft Dot–NET Framework, Creating Threads, Managing Threads, Thread Pools, Thread Synchronization, POSIX Threads, Creating Threads, Managing Threads, Thread Synchronization, Signaling, Compilation and Linking. (Text: Chapter 5)	**10**	L1,L2, L3
4	**OpenMP:** A Portable Solution for Threading Challenges in Threading a Loop, Loop–carried Dependence, Data– race Conditions, Managing Shared and Private Data, Loop Scheduling and Portioning, Effective Use of Reductions, Minimizing Threading Overhead, Work–sharing Sections, Performance–	**10**	L1,L2, L3,L4

	oriented Programming, Using Barrier and No wait, Interleaving Single– thread and Multi– thread Execution, Data Copy–in and Copy–out, Protecting Updates of Shared Variables, Intel Task queuing Extension to OpenMP, OpenMP Library Functions, OpenMP Environment Variables, Compilation, Debugging, performance. (Text: Chapter 6)		
5	**Solutions to Common Parallel Programming Problems:** Too Many Threads, Data Races, Deadlocks, and Live Locks, Deadlock, Heavily Contended Locks, Priority Inversion, Solutions for Heavily Contended Locks, Non–blocking Algorithms, ABA Problem, Cache Line Ping– ponging, Memory Reclamation Problem, Recommendations, Thread–safe Functions and Libraries, Memory Issues, Bandwidth, Working in the Cache, Memory Contention, Cache related Issues, False Sharing, Memory Consistency, Current IA– 32 Architecture, Itanium Architecture, High–level Languages, Avoiding Pipeline Stalls on IA–32, Data Organization for High Performance. (Text: Chapter 7)	**10**	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Apply the knowledge of parallel programming to solve the design problems.
CO2	Analyze the dataflow among different cores of the multicore processor.
CO3	Use different Threading APIs for programming multicore architectures.
CO4	Explain the different aspects of OpenMP in parallel programming.
CO5	Solve common parallel programming problems for multicore architectures.

Course outcome and program outcome mapping

CO1	PO2, PO3, PO4, PO5, PO12
CO2	PO2, PO3, PO4, PO5, PO6, PO12
CO3	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO4	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO5	PO1, PO2, PO3, PO4, PO5, PO6, PO8, PO12

TEXT BOOKS:

1. Shameem Akhter and Jason Roberts "**Multicore Programming, Increased Performance through Software Multi–threading**" Intel Press, 2006.ISBN 0-9764832-4-6.

REFERENCE BOOKS/WEBLINKS:

1. Calvin Lin, Lawrence Snyder, "**Principles of Parallel Programming**" Pearson Education, 2009. ISBN-13: 978-0321487902.
2. Michael J. Quinn ,"**Parallel Programming in C with MPI and OpenMP**", Tata McGraw Hill, 2004. ISBN 13: 9780070582019.
3. David E, Culler, Jaswinder Pal Singh with Anoop Gupta "**Parallel Computer Architecture A Hardware/ Software Approach**", eBook ISBN: 9780080573076 Hardcover ISBN: 9781558603431.

Subject Title**: Static Timing Analysis (STA)**		
Subject Code**: 22LVS235**	No. of Credits**: 03 = 3:2:0 (L:T:P)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Understand timing analyses at various process, environment and interconnect corners.
2. Apply the learnt concepts of STA to evaluate the delay of the circuits.
3. Understand and analyze the signal integrity issues for the IC.
4. Generate the timing analysis report using EDA tool.
5. Understand verification and analyze the generated report to identify issues for the violation
6. Learn different techniques to meet timing in an IC design.
7. Set up the timing analysis environment and perform the timing analysis for various cases.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction**: Nanometer Designs, What is Static Timing Analysis?. Why Static Timing Analysis?, Crosstalk and Noise, Design Flow, CMOS Digital Designs, FPGA Designs, Asynchronous Designs, STA at Different Design Phases, Limitations of Static Timing Analysis, Power Considerations, Reliability Considerations, **STA Concepts**: CMOS Logic Design, Basic MOS Structure, CMOS Logic Gate, Standard Cells, Modeling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions .	**8**	L1,L2, L3
2	**Standard Cell Library**: Pin Capacitance, Timing Modeling, Timing Models - Combinational Cells, Timing Models - Sequential Cells, State-Dependent Models, Interface Timing Model for a Black Box, Advanced Timing Modeling, Power Dissipation Modeling, Other Attributes in Cell Library, Characterization and Operating Conditions.	**8**	L1,L2, L3
3	**Interconnect Parasitics:** RLC for Interconnect, Wireload Models, Representing Coupling Capacitances, Hierarchical Methodology, Reducing Parasitics for Critical Nets. **Delay Calculation**: Overview, Cell Delay using Effective Capacitance, Interconnect Delay, Slew Merging, Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation, Slack Calculation.	**8**	L1,L2, L3
4	**Configuring the STA Environment**: What is the STA Environment? Specifying Clocks, Generated Clocks, Constraining Input Paths, Constraining Output Paths, Timing Path Groups, Modeling of External Attributes, Design Rule Checks, Virtual Clocks, Refining the Timing Analysis, Point-to-Point Specification, Path Segmentation.	**8**	L1,L2, L3,L4
5	**Timing Verification**: Setup Timing Check, Hold Timing Check, Multicycle Paths, Crossing Clock Domains, False Paths, Half- Cycle Paths, Removal Timing Check, Recovery Timing Check, Timing across Clock Domains, **Examples**: Slow to Fast Clock Domains, Fast to Slow Clock Domains, Half-cycle Path - Case 1, Half-cycle Path - Case 2, Fast to Slow Clock Domain, Slow to Fast Clock Domain, Multiple Clocks.	**8**	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Evaluate the delay of any given digital circuits.
CO2	Prepare the resources to perform the static timing analysis using EDA tool
CO3	Prepare timing constraints for the design based on the specification.
CO4	Generate the timing analysis report using EDA tool for different checks.
CO5	Perform verification and analyze the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing.

Course outcome and program outcome mapping

CO1	PO1, PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4,PO5
CO4	PO7, PO8,
CO5	PO3, PO4

TEXT BOOKS:

1. J. Bhasker, R Chadha, "**Static Timing Analysis for Nanometer Designs: A Practical Approach**", Springer, 2009.

REFERENCE BOOKS/WEBLINKS:

1. Sridhar Gangadharan, Sanjay Churiwala, "**Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)**", Springer, 2013.
2. Naresh Maheshwari and Sachin Sapatnekar, "**Timing Analysis and Optimization of sequential Circuits**", Springer Science and Business Media, 1999.

II Semester

Professional Elective-2

22LVS24X

Subject Title**: Algorithms for VLSI Physical Design**		
Subject Code**: 22LVS241**	No. of Credits**: 03 = 3:2:0 (L:T:P)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE **= 40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Explain the need for synthesis and verification for digital circuits
2. Describe the VLSI Automation algorithms used for physical design
3. Understand the problem of placement and routing and identify algorithms to address these problems.
4. Illustrate the concept of cell routing constrained and unconstrained via minimization.
5. Get the knowledge of compaction problem and basic ways to tackle it.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**Logic Synthesis & Verification:** Introduction to combinational logic synthesis, Binary Decision Diagram, **High Level Synthesis**: Hardware models for High-level synthesis, Internal representation of the input algorithm (Data Flow Graph). [TEXT 2]	**10**	L1,L2, L3
2	**VLSI Automation Algorithms**: **Partitioning:** problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms [TEXT 1]	**10**	L1,L2, L3
3	**Placement, Floor Planning & Pin Assignment**: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment [TEXT 1]	**10**	L1,L2, L3
4	**Global Routing**: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches **Detailed Routing**: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms [TEXT 1]	**10**	L1,L2, L3,L4
5	**Over The Cell Routing & Via Minimization**: two layers over the cell routers, constrained & unconstrained via minimization **Compaction:** problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction [TEXT 1]	**10**	L1,L2, L3,L4

***BTL**: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Understand and exploit the features of logic synthesis and high level synthesis at introductory level in the VLSI design which happens before the physical design.
CO2	Understand the partitioning process, formulate the problem, classify and exemplify the different partitioning algorithms.
CO3	Understand the placement, floor-planning and pin assignment process, formulate the problem, classify and exemplify the different algorithms.

CO4	Understand the placement floor-planning and pin assignment process, formulate the problem, classify and exemplify the different algorithms.
CO5	Understand the over the cell routing and compaction process, formulate the problem, and exemplify the different algorithms.
Course outcome and program outcome mapping	
CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO4,PO5,PO7
CO4	PO1,PO2,PO3,PO4
CO5	PO4,PO6,PO7,PO12

TEXT BOOKS:

1. Naveed Shervani, "**Algorithms for VLSI physical design Automation**", Kluwer Academic Publisher, Second edition.
2. Sabih H. Gerez, "Algorithms for VLSI Design Automation", JOHN WILEY & SONS, 2000.

REFERENCE BOOKS/WEBLINKS:

1. Christophn Meinel & Thorsten Theobold, "**Algorithm and Data Structures for VLSI Design**", KAP, 2002.
2. Rolf Drechsheler : "**Evolutionary Algorithm for VLSI**", Second edition
3. Trimburger, "**Introduction to CAD for VLSI**", Kluwer Academic publisher, 2002
4. Andrew B. Kahng • Jens Lienig, Igor L. Markov, Jin Hu "**VLSI Physical Design:From Graph Partitioning to Timing Closure**", Springer publications, 2011.

Subject Title: **Synthesis and Optimization of Digital Circuits (SODC)**		
Subject Code: **20LVS242**	No. of Credits**: 3=3:2:0 (LTP)**	No. of lecture hours/week **:03**
Exam Duration :**03 Hours**	CIE +(Assignment+Seminar)+ SEE = **30+(10+10)+50=100**	Total No. of Contact Hours **:40**

Course Learning Objectives

1 Explain the need for synthesis and optimization for digital circuits

2 Describe the basic optimization techniques used in circuits design

3 Explain the advanced tools and techniques in digital systems design. These include Hardware Modelling and Compilation Techniques

4 Illustrate the concept of scheduling and resource binding for optimization.

5. Describe the logic-Level synthesis and optimization techniques for combinational and Sequential circuits.

UNIT No	**Syllabus Contents**	No of Hours	Blooms Taxonomy Level
1	**Introduction:** Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization. **Graphs:** Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications. **[Text1]**	8	L1,L2, L3,
2	**Hardware Modelling:** Hardware Modelling Languages, distinctive features, structural hardware language, Behavioural hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques. [**Text1]**	8	L1,L2, L3, L4
3	**Two Level Combinational Logic Optimization**: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations. **Multiple Level Combinational Optimizations**: Models and transformations for combinational networks, algebraic model: Substitution, Extraction and Algebraic Kernels, Decomposition. [**Text1]**	8	L1,L2, L3, L4
4	**Schedule Algorithms:** A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits. **Cell Library Binding:** Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Anti-fuse based F.P.G.As), rule based library binding. [**Text1]**	8	L1,L2, L3, L4

5	**Sequential Circuit Optimization:** Sequential circuit optimization using state based models: State minimization, state Encoding, Other Optimization Methods and Recent Developments.**[Text1]**	8	L1,L2, L3, L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

CO1	Describe and identity different process of synthesis and optimization, graph theory and its algorithms to optimize a Boolean equation.
CO2	Explain the different types of hardware modelling techniques.
CO3	Illustrate the different two level and multilevel optimization algorithms for combinational circuits.
CO4	Describe the different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models.
CO5	Analyze the different type of simulator and design of the testability technique.

Course outcome and program outcome mapping

CO1	PO2,PO5,PO12
CO2	PO2,PO3,P05
CO3	PO4,PO5
CO4	PO5,PO6
CO5	PO6,PO7
CO6	PO2,PO3,PO7,PO12

Text Book:

1. Giovanni De Micheli, "**Synthesis and Optimization of Digital Circuits**", Tata McGraw-Hill, 2003.

REFERENCE BOOKS/WEBLINKS:

1. Edwars M.D., **Automatic Logic synthesis Techniques for Digital Systems**, Macmillan New Electronic Series, 1992.
2. Sneh Saurabh, "**Introduction to VLSI Design Flow**", Cambridge University press, 2023.

Subject Title**: ARM Programming and Optimization**		
Subject Code**: 22LVS243**	No. of Credits**: 03 = 3:2:0 (L:T:P)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE **= 40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Understanding the programmer's model of ARM processor.
2. Use of available optimization methods for ARM architectures.
3. Realizing real time signal processing applications & primitive OS operations on different ARM architectures.
4. To analyze and demonstrate different applications on ARM development boards.
5. Understand the different memory optimization methods for ARM architectures

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	Introduction, Data Path Architecture, Registers, Modes, Exceptions **Programming in C for ARM**: Overview of C Compilers and optimization, basic C data types, C looping structures, register allocation, function calls, pointer aliasing, structure arrangement, bit fields, unaligned Data and endianess, division, floating point, inline functions and inline assembly, portability issues. (Text 1)	**8**	L1,L2, L3
2	**Writing and Optimizing ARM Assembly Code:** Writing assembly code, profiling and cycle counting, instruction scheduling, register allocation, conditional execution, looping constructs, Bit manipulation, efficient switches. Handling unaligned data. (Text 1)	**8**	L1,L2, L3
3	**Digital Signal Processing on ARM**: Representing a digital signal, Introduction to DSP on the ARM, FIR filters: Realization of filters on ARM7 and Cortex M3, IIR Filters: Realization of filters on ARM7 and Cortex M3, CMSIS DSP Library. (Text 1)	**8**	L1,L2, L3
4	**Firmware:** Firmware and Boot loader **Embedded Operating Systems:** Fundamental Components, Simple Operating System. (Text 1)	**8**	L1,L2, L3,L4
5	**Memory Protection Unit:** Over view of the MPU's, MPU registers, setting up the MPU, Memory barrier and memory configuration, Using sub-region disable, Consideration when using MPU, Other usages of MPU. (Text 2)	**8**	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Describe the programmer's model of ARM processor and Apply the optimization methods available for ARM architectures to design embedded software in C to meet given constraints.
CO2	Apply the optimization methods available for ARM architectures to design embedded software in assembly code to meet given constraints.
CO3	Realize real time signal processing applications on different ARM architectures by making use of software libraries.
CO4	Realize primitive OS operations on different ARM architectures by making use of software libraries.
CO5	Analyze the memory protection and optimization methods available for ARM architectures.

Course outcome and program outcome mapping

CO1	PO2, PO3, PO4, PO5, PO12
CO2	PO2, PO3, PO4, PO5, PO6, PO12
CO3	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO4	PO1, PO2, PO3, PO4, PO5, PO6, PO12
CO5	PO1, PO2, PO4, PO5, PO6, PO12

TEXT BOOKS:

1. Andrew N Sloss, Dominic Symes, Chris Wright, "**ARM System Developers Guide**", 2008, Elsevier, Morgan Kaufman publishers, ISBN-13:9788181476463.
2. ,Joseph Yiu, **The definitive Guide to the ARM Cortex- M3 & M4 Processors,** 3rd Edition, 2014, Newnes (Elsevier), ISBN: 978-93-5107-175-4.

REFERENCE BOOKS/WEBLINKS:

1. **ARM System on Chip Architecture**, Steve Furber, 2nd Edition, 2001, Pearson Education Limited, ISBN-13:9780201675191.
2. Technical reference manual for ARM processor cores, including Cortex M series, ARM 11, ARM 9 & ARM 7 processor families.

Subject Title**:** **High Speed VLSI Design**		
Subject Code**: 22LVS244**	No. of Credits**: 03 = 3:2:0 (L:T:P)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE **= 40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Learn sources of process – driven performance variation in quarter-micron CMOS and apply the rules of thumb.
2. Comprehend non-clocked static circuit families, used to implement combinatorial logic.
3. Interpret the design styles used for clocked and non-clocked systems.
4. Explore the design parameters such as on-chip device length tolerance, supply rail inconsistency and temperature variations.
5. Understand clocking styles, jitters and skews.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Process Variability:** Introduction**,** Front-end -of-line variability considerations, charge loss mechanisms, back-end-of- line variability considerations.**[Text 1]**	**8**	L1,L2, L3
2	**Non-Clocked logic styles**: Introduction, static CMOS structures, DC VS logic, Non-clocked pass-gate families. **Clocked logic styles**: Introduction, single-rail domino logic styles. Dual-rail domino structures, latched domino structures, clocked pass gate logic. **[Text 1]**	**8**	L1,L2, L3
3	**Circuit Design margin and design variability:** Introduction, process induced variation, design induced variations, and application induced variations', Noise. **Latching Strategies:** Introduction, basic latch design, latching single ended logic, latching differential logic, race-free latched for pre-charge logic.**[Text 1]**	**8**	L1,L2, L3
4	**Interface Techniques:** Introduction, signaling standard, chip-chip communication networks, ESD protection, Driver design techniques, receiver design techniques.**[Text 1]**	**8**	L1,L2, L3,L4
5	**Clocking styles:** Introduction, clock jitter and skew, clock generation and clock distribution.**[Text 1]**	**8**	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Accomplish their goal in achieving the tradeoffs in performance, power, area, reliability and cost by the selection of design styles
CO2	Analyze strengths and weakness of clocked and non-clocked logic circuit families in terms of characteristics.
CO3	Interpret the performance considerations to enable high speed communication; by choosing the input and output convention compatible with signal levels required for the design.
CO4	Analyze Interface techniques for signaling standard and communications.
CO5	Design clocking styles clock distributions and jitters.

Course outcome and program outcome mapping	
CO1	PO1,PO2
CO2	PO2, PO3, PO4
CO3	PO3, PO5, PO6
CO4	PO4,PO5,PO6,PO7
CO5	PO5, PO6, PO7

TEXT BOOKS:

1. Kerry Bernstein, "High Speed CMOS Design Styles", Kluwer, 1999.

REFERENCE BOOKS/WEBLINKS:

1. Howard Johnson & Martin Graham, "**High Speed Digital Design: A Handbook of Black Magic**", Prentice Hall PTR, 1993.
2. William S. Dally & John W. Poulton, "**Digital Systems Engineering**", Cambridge University Press, 1998.
3. Masakazu Shoji, "High Speed Digital Circuits", Addison Weley Publishing Company, 1996.

Subject Title**: Design of VLSI systems**		
Subject Code**: 22LVS245**	No. of Credits**: 03 = 3:2:0 (L:T:P)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE **= 40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Give in-depth knowledge about VLSI design methodologies
2. Understand the coding concept of the VLSI design of ASIC design
3. Analyse the performance of VLSI arithmetic blocks using CAD tools
4. Design arithmetic blocks using the CMOS for ALU
5. Evaluate the circuit design/fabrication cost.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**VLSI System Design Methodology:** Structure Design, Strategy, Hierarchy, Regularity, Modularity, and Locality. System on Chip Design options: Programmable logic and structures, Programmable interconnect, programmable gate arrays, Sea of gate and gate array design, standard cell design, full custom mask design. **Chip Design Methods:** Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System	**10**	L1,L2, L3
2	**Design Capture Tools:** HDL Design, Schematic Design, Layout Design, Floor planning and Chip Composition. Design Verification Tools: Simulation Timing Verifiers, Net List Comparison Layout Extraction, Design Rule Verification. **Data Path Sub System Design:** Introduction, Addition, Subtraction, Comparators, Counters, Boolean logical operations, coding, shifters, Multiplication, Parallel Prefix computations	**10**	L1,L2, L3
3	**Array Subsystem Design:** SRAM, Special purpose RAMs, DRAM, Read only memory, Content Addressable memory, Programmable logic arrays. **Control Unit Design:** Finite State Machine (FSM) Design, Control Logic Implementation: PLA control implementation, ROM control implementation.	**10**	L1,L2, L3
4	**Special Purpose Subsystems:** Packaging, power distribution, I/O, Clock, Transconductance amplifier, follower integrated circuits. **Design Economics:** Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Person power, example	**10**	L1,L2, L3,L4
5	**VLSI System Testing & Verification:** Introduction, A walk through the Test Process, Reliability, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan **VLSI Applications: Case Study: RISC microcontroller, ATM Switch, etc.**	**10**	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Gain in-depth knowledge in VLSI design methodologies.
CO2	Develop the architectures for VLSI system design.

CO3	Design arithmetic blocks using the CMOS for ALU.
CO4	Evaluate the circuit design/fabrication cost.
CO5	Model the VLSI system using the State-Machine.
Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3
CO2	PO1,PO2,PO3,PO4
CO3	PO3,PO4,PO5,PO6
CO4	PO2,PO3,PO4,PO5
CO5	PO3,PO5,PO7

TEXT BOOKS:

1. Neil H.E. Weste, David Harris, "CMOS VLSI Design: A Circuits and System Perspectives" Addison Wesley - Pearson Education, 3rd Edition, 2004.

REFERENCE BOOKS/WEBLINKS:

1. Wayne, Wolf, "Modern VLSI Design: System on Silicon" Prentice Hall PTR/Pearson Education, Second Edition, 1998.
2. Douglas A Pucknell & Kamran Eshragian , "Basic VLSI Design" PHI 3rd Edition (original Edition – 1994).

Subject Title**:** **VLSI Design and Embedded Systems Lab-2**		
Subject Code**: 22LVSL26**	No. of Credits**: 02 = 0:0:2 (L:T:P)**	No. of lecture hours per week**: 04**
Exam Duration**: 3 Hours**	CIE + SEE = **50+50=100**	Total No. of lecture hours**: 48**

Course Learning Objectives: This course will enable the students to:

1. Objective of this lab is to learn the Virtuoso tool as well learn the flow of the Full Custom IC design cycle.
2. Usage of DRC, LVS and Parasitic Extraction on the various designs, like inverter, differential amplifier, operational amplifier, R-2R based DAC and Mixed signal design of SAR based ADC,
3. Timing analysis and power analysis of the circuits using CADENCE
4. Design a testing program for thread and process creation.
5. Design a testing program for specified conditions using multithreaded application.
6. Design a POSIX based message queue for communicating between two tasks.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
	PART A		
1	Design an INVERTER and analyze the following parameters using the cadence VIRTUSO *Schematic Entry* *Building the Inverter Test Design* *Analog Simulation* *Creating Layout View of Inverter* *Parasitic Extraction* *Creating the Configuration View* *Generating Stream Data*	**3**	L1,L2, L3,L4
2	Design an Diff_ Amplifier and analyze the following parameters using the cadence VIRTUSO *Schematic Entry* *Analog Simulation* *Creating a Layout View of Diff_ Amplifier* *Physical Verification*	**3**	L1,L2, L3,L4
3	Design an Common Source Amplifier and analyze the following parameters using the cadence VIRTUSO *Schematic Entry* *Symbol Creation* *Building the Common Source Amplifier Test Design* *Analog Simulation with Spectre* *Creating a layout view of Common Source Amplifier*	**3**	L1,L2, L3,L4
4	Design an Common Drain Amplifier and analyse the following parameters using the cadence VIRTUSO *Schematic Entry Symbol Creation* *Building the Common Drain Amplifier Test Design* *Analog Simulation with Spectre* *Creating a layout view of Common Drain Amplifier*	**3**	L1,L2, L3, L4

5	Design an Operational Amplifier and analyze the following parameters using the cadence VIRTUSO *Schematic Entry* *Symbol Creation* *Building the Operational Amplifier Test Design* *Analog Simulation with Spectre* *Creating a layout view of Operational Amplifier*	**3**	L1,L2, L3, L4
6	Design an R-2R DAC and analyze the following parameters using the cadence VIRTUSO *Schematic Entry Symbol Creation* *Building the R-2R DAC Test Design* *Analog Simulation with Spectre* *Creating a layout view of R-2R DAC*	**3**	L1,L2, L3,L4
7	Design an SAR BASED ADC and analyse the following parameters using the cadence VIRTUSO *Design Information* *Import the Verilog Module into ADE Using Verilog In.* *Schematic Entry* *Mixed Signal Simulation Using AMS in ADE*	**3**	L1,L2, L3,L4
	PART-B		
1	Creating a Thread and Process using POSIX Thread standard.	**3**	L1,L2, L3,L4
2	Creating two pipes for sending and receiving messages.	**3**	L1,L2, L3,L4
3	Creating 'n' number of child Threads.	**3**	L1,L2, L3,L4
4	Program to pass message through pipes.	**3**	L1,L2, L3,L4
5	Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes.	**3**	L1,L2, L3,L4

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Note:

- The internal assessment will be based on Record, Conduction, Question and Answer session.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Design analog circuits
CO2	Draw layouts of analog circuits
CO3	Analyze the analog circuits using CADENCE
CO4	Create test programs for thread and process.
CO5	Develop the Multithreaded application.
CO6	Create a POSIX based message queue for communicating between two tasks.

Course outcome and program outcome mapping

CO1	PO1,PO2
CO2	PO2,PO3,PO4
CO3	PO2,PO3,PO4
CO4	PO1,PO4,PO8
CO5	PO4,PO5,PO6,PO8

CO6	PO3,PO4,PO5,PO6,PO8,PO9

TEXT BOOKS:

1. Philip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, Third Edition, 2013.
2. Shibu K V, "Introduction to Embedded Systems", First Edition, Tata McGraw Hill Education Private Limited, 2009.

REFERENCE BOOKS/WEBLINKS:

1. https://www.buecher.de › ... › Mikroelektronik › Sonstige
2. https://www.cadence.com
3. https://www.cadence.com › Home › Tools
4. https://www.cadence.com › Home › Training › All Courses.

Subject Title**:** **Audit Course / Ability Enhancement Course**		
Subject Code**:** **22AUD27/22AEC27**	No. of Credits**: PP**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + SEE =	Total No. of lecture hours**: 40**

List of ONLINE Audit Course / Ability Enhancement Courses

Course Type	**Course Title**	**Duration**
MOOC - Swayam NPTEL	VLSI Design Flow: RTL to GDS	12 weeks
MOOC - Swayam NPTEL	Analog Electronics	12 weeks
MOOC - Swayam NPTEL	System Design using Verilog	12 weeks
MOOC - Swayam NPTEL	Computer Architecture And Organization	12 weeks
MOOC - Swayam NPTEL	Fabrication Techniques for MEMs-based sensors: clinical perspective	12 weeks

III Semester Syllabus

(2022 Batch)

Subject Title: **Low Power VLSI Design**		
Subject Code: **22LVS31**	No. of Credits: **04 = 3:0:0:2 (L:T:P:S)**	No. of lecture hours per week: **04**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **52**

Course Learning Objectives: This course will enable the students to:

6. Understand the basic knowledge of power dissipation in CMOS devices and analyse the Technology Impact on Low Power.
7. Study the Probabilistic power analysis and Simulation Power analysis.
8. Discuss the concepts of Low power Clock Distribution.
9. Illustrate the concepts of Low power Architecture & Systems
10. Discuss the various Algorithm & Architectural Level Methodologies.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction:** Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **Simulation power analysis:** SPICE circuit simulation gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. **TEXT-1**	**8**	L1,L2, L3
2	**Probabilistic power analysis**: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **Low Power Design Circuit level**: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. **TEXT-1 and TEXT-2**	**8**	L1,L2, L3
3	**Logic level:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. **TEXT-1 and TEXT-2**	**8**	L1,L2, L3
4	**Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design. **TEXT-1 and TEXT-2**	**8**	L1,L2, L3
5	**Algorithm & Architectural Level Methodologies:** Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis. **TEXT-1 and TEXT-2**	**8**	L1,L2, L3

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Analyze the Algorithm & Architectural Level Methodologies.
CO2	Apply the Different simulation tools for Power analysis.

CO3	Analyze Power & performance management with the concepts of gate level logic simulation and various concepts of Gate reorganization.
CO4	Discuss Power dissipation in clock distribution and the Sources of power dissipation on Digital Integrated circuits.
CO5	Illustrate the data correlation analysis in DSP systems.
Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Kaushik Roy, Sharat Prasad, "**Low-Power CMOS VLSI Circuit Design**" Wiley, 2000
2. Gary K. Yeap, "**Practical Low Power Digital VLSI Design**", KAP, 2002
3. Jan M. Rabaey , Massoud Pedram, "**Low Power Design Methodologies**" The Springer International Series in Engineering and Computer Science.

REFERENCE BOOKS/WEBLINKS:

1. A.P. Chandrasekaran and R.W. Broadersen, "**Low power digital CMOS design**", Kluwer Academic, 1995.
2. A Bellamour and M I Elmasri, "**Low power VLSI CMOS circuit design**", Kluwer Academic, 1995.
3. www.ntpel.com.

Professional Elective 3
Syllabus

Subject Title**:** **Advanced Computer Architecture**		
Subject Code**: 22LVS321**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Explain the concepts of parallel computing and hardware technologies
2. Compare and contrast the parallel architectures
3. Illustrate parallel programming concepts

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Parallel Computer Models:** The State of Computing, Multiprocessors and multicomputers, Multivector and SIMD computers. **Program and Network Properties:** Conditions of parallelism, Program Partitioning & Scheduling, Program Flow Mechanisms. **TEXT-1**	**8**	L1,L2, L3,L4
2	**Principles of Scalable Performance:** Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches. **TEXT-1** **Processors & Memory Hierarchy:** Advanced processor technology, Super Scalars & Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology. **TEXT-1**	**8**	L1,L2, L3,L4
3	**Bus, Cache and Shared Memory:** Bus Systems, Cache Memory Organizations, Shared Memory Organizations, Sequential & Weak Consistency Model. **TEXT-1** **Pipelining & Superscalar Technologies:** Linear Pipeline Processors, Nonlinear Pipeline Processors, Instruction Pipeline Design, Arithmetic Pipeline Design, Superscalar Pipeline Design. **TEXT-1**	**8**	L1,L2, L3,L4
4	**Multivector& SIMD Computers:**Vector Processing principles, Multivector Multiprocessors, Compound Vector Processing, SIMD Computer Organization. **TEXT-1** **Scalable, Multithreaded and Data Flow Computers:** Latency Hiding Techniques, Principles of Multithreading, Fine Grain Multi Computers, Scalable and Multithreaded Architectures, Data Flow and Hybrid Architectures. **TEXT-1**	**8**	L1,L2, L3,L4
5	**Parallel Models, Languages and Compilers**: Parallel Programming Models, Parallel Languages & Compilers, Dependence Analysis and Data Arrays, Code Optimization and Scheduling, Loop Parallelization and Pipelining. **TEXT-1** **Parallel Program Development and Environments:** Parallel Programming Environments, Synchronization and Multi Processor Modes, Shared Variable Program Structures. **TEXT-1**	**8**	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Understand the basic concepts for parallel processing

CO2	Analyze program partitioning and flow mechanisms
CO3	Apply pipelining concept for the performance evaluation
CO4	Learn the advanced processor architectures for suitable applications.
CO5	Understand parallel Programming
Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Kai Hwang & Narendra Jotwani, "Advanced Computer Architecture: Parallelism, Scalability, Programmability", McGraw Hill Education, ISBN:978-93-392-2092- I, 3" Edition, 2016.

REFERENCE BOOKS/WEBLINKS:

1. John L. Hennessy and David A. Patterson, Computer Architecture: A quantitative approach, 5th edition, Morgan Kaufmann Elseveir, 2013.
2. www.ntpel.com.

Subject Title: **CMOS RF CIRCUIT DESIGN**		
Subject Code: **22LVS322**	No. of Credits: **03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week: **03**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **40**

Course Learning Objectives: This course will enable the students to:

1. Learn basic concepts in RF and microwave design emphasizing the effects of nonlinearity and noise.
2. Able to appreciate communication system, multiple access and wireless standards necessary for RF circuit design.
3. Able to deal with transceiver architecture, various receiver and transmitter designs, their merits and demerits
4. Understand the design of RF building blocks such as Low Noise Amplifiers and Mixers.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction to RF Design and Wireless Technology:** **Basic concepts in RF design (I):** General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range.**[Text 1]**	8	L1,L2, L3,L4
2	**Basic concepts in RF design (II**): Passive impedancetransformation, scattering parameters, analysis of nonlineardynamic systems.**[Text 1]**	8	L1,L2, L3,L4
3	**Communication Concepts:** General concepts, analog modulation, digital modulation, spectral re-growth, Mobile RF communications, Multiple access techniques, Wireless standards.**[Text 1]**	8	L1,L2, L3,L4
4	**Transceiver Architecture (I):** General considerations, Receiver architecture.**[Text 1]**	8	L1,L2, L3,L4
5	**Transceiver Architecture (II):** Transmitter architectures **Low Noise Amplifiers:** LNA topologies: common-source stage withinductive load, common-source stage with resistive feedback. **Mixers:** General considerations, passive down conversion mixers. **[Text 1]**	8	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Analyze the effect of nonlinearity and noise in RF and microwave design.
CO2	Exemplify the approaches taken in actual RF products.
CO3	Minimize the number of off-chip components required to design mixers and Low-Noise Amplifiers.
CO4	Explain various receivers and transmitter topologies with their merits and drawbacks.

CO5	Demonstrate how the system requirements define the parameters of the circuits and how the performance of each circuit impacts that of the overall transceiver.
Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. B. Razavi, "**RF Microelectronics**," PHI, Second edition, 2004.

REFERENCE BOOKS/WEBLINKS:

1. R. Jacob Baker, H.W. Li, D.E. Boyce "CMOS Circuit Design, layout and Simulation", PHI 1998.
2. Thomas H. Lee "Design of CMOS RF Integrated Circuits" Cambridge University press 1998.
3. Y.P. Tsividis, "Mixed Analog and Digital Devices and Technology", TMH 1996.
4. www.ntpel.com.

Subject Title**:** **Embedded Linux System Design and Development**		
Subject Code**: 22LVS323**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction:** History of Embedded Linux, Why Embedded Linux, Embedded Linux Versus Desktop Linux, Frequently Asked Questions, Embedded Linux Distributions, Porting Roadmap. Getting Started: Architecture of Embedded Linux, Linux Kernel Architecture, User Space, Linux Start-Up Sequence, GNU CrossPlatform Tool chain.	**8**	L1,L2, L3,L4
2	**Board Support Package:** Inserting BSP in Kernel Build Procedure, Memory Map, Interrupt Management, The PCI Subsystem, Timers, UART, Power Management.	**8**	L1,L2, L3,L4
3	**Embedded Storage:** Flash Map, MTD—Memory Technology Device, MTD Architecture, Sample MTD Driver for NOR Flash, The Flash-Mapping Drivers, MTD Block and Character Devices,Mtdutils Package, Embedded File Systems, Optimizing Storage Space, Tuning Kernel Memory.	**8**	L1,L2, L3,L4
4	**Embedded Drivers:** Linux Serial Driver, Ethernet Driver , I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, Kernel Modules.	**8**	L1,L2, L3,L4
5	**Porting Applications:** Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver	**8**	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Understand the embedded Linux development environment.
CO2	Understand and create Linux BSP for a hardware platform.
CO3	Understand the Linux model for embedded storage and write drivers and applications for the same.
CO4	Understand various embedded Linux drivers such as serial, I2C, and so on.
CO5	Port applications to embedded Linux from a traditional RTOS.

Course outcome and program outcome mapping

CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10

CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. P.Raghavan, Amol Lad, Sriram Neelakandan, "Embedded Linux System Design And Development," Auerbach Publications, Taylor & Francis Group, 2006.

REFERENCE BOOKS/WEBLINKS:

1. Karim Yaghmour, Jon Masters, Gilad BenYossef, and Philippe Gerum "Building Embedded Linux Systems O'Reilly publications, 2nd edition.

Subject Title**:** **SoC Design**		
Subject Code**: 22LVS324**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. To Describe the organization and implementation of the 3- and 5-stage pipeline ARM processor cores
2. To Understand the needs high-level language (in this case, C) in application development
3. To Know the issues involved in debugging systems in embedded processor cores and in the production testing of board-level systems.
4. To learn different ARM integer cores, concept of memory hierarchy and management.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**ARM Organization and Implementation:** 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface. **The ARM Instruction Set:** Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL), Branch, Branch with Link and exchange (BX, BLX), Software Interrupt (SWI).	**8**	L1,L2, L3,L4
2	**The ARM Instruction Set (Continued)** Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture	**8**	L1,L2, L3,L4
3	**Architectural Support for High-Level Languages:** Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements ,Loops, Functions and procedures, Use of memory, Run-time environment.	**8**	L1,L2, L3,L4
4	**Architectural Support for System Development:** The ARM memory interface, The Advanced Microcontroller Bus Architecture(AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support	**8**	L1,L2, L3,L4
5	**ARM Processor Cores:** ARM7TDMI, ARM8, ARM9TDMI, ARM10TDMI, Discussion, Example and exercises. **Memory Hierarchy**: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.	**8**	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issue.
CO2	Use the concepts and methodologies employed in designing a System- on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.
CO3	Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.
CO4	Use integrated ARM CPU cores (including Strong ARM) that incorporate full support for memory management.
CO5	Analyze the requirements of a modern operating system and use the ARM architecture to address the same.

Course outcome and program outcome mapping

CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Steve Furber "**ARM System-On-Chip Architecture**" Addison Wesley, 2nd edition,2001.

REFERENCE BOOKS/WEBLINKS:

1. Joseph Yiu "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier) , 2nd edition, 2010.
2. Sudeep Pasricha and Nikil Dutt," On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
3. Michael Keating, Pierre Bricaud "Reuse Methodology Manual for System on Chip designs", Kluwer Academic Publishers, 2ndedition, 2008.

Subject Title: **FinFETs and Other Multi-Gate Transistors**		
Subject Code: **22LVS325**	No. of Credits: **03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week: **03**
Exam Duration: **3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours: **40**

Course Learning Objectives: This course will enable the students to:

1. To learn the evolution of SOI MOS transistor.
2. To have an insight into thin film formation techniques and advanced gate stack deposition.
3. To enable the students to analyse physics behind BSIM-CMG.
4. To analyse the electrostatics of the multi-gate MOS system.
5. To realise the interrelationship between the multi-gate FET device properties and digital and analog circuits.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**SOI MOSFET: From Th Single Gate to MultiGate:** A brief history of Multiple - Gate MOSFETs, MultiGate MOSFET physics.	8	L1,L2, L3,L4
2	**Multigate MOSFET Technology :** Introduction, Active Area:Fins, Gate Stack	8	L1,L2, L3,L4
3	**BSIM- CMG:** A Compact Model for Mult-Gate Transistors : Introduction, Framework for MultiGate FET Modeling, MultiGate Models, BSIM-CMG and BSIM-IMG, BSIM-CMG.	8	L1,L2, L3,L4
4	**Physics of the MultiGate MOS system :** Device electrostatics, Double gate MOS system, Two-dimensional confinement.	8	L1,L2, L3,L4
5	**Multi-Gate MOSFET circuit Design :** Introduction, Digital Circuit Design, Analog Circuit Design	8	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Understand the physics and bring out the advantages and challenges of Multi-gate FETs.
CO2	Describe thin film formation technique, gate stack deposition and issues related to fin crystal orientation and mobility enhancement.
CO3	Apply the compact models to describe physics beyond BSIMCMG to enable fast computer analysis of device/circuit behaviour.
CO4	Analyse electrostatics of multi-gate MOS system using quantum-mechanical concepts and describe the effects of tunnelling through thin gate dielectrics.
CO5	Correlate multigate FET device properties and elementary digital and analog circuits.

Course outcome and program outcome mapping

CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10

CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. J.P.Colinge, **FinFETs and other Multi-Gate Transistors,** Springer, Series on Integrated Circuits and Systems, 2008.
2. Samar Saha,, **Fin FET Devices for VLSI Circuits and Systems**, CRC Press, First Edition, 2020

REFERENCE BOOKS/WEBLINKS:

1. Weihua Han,Zhiming M. Wang, **Toward Quantum FinFET** , Springer Cham, First Edition 2021.
2. Yogesh singh Chauhan, Darsen D, et.al , **FinFET Modeling for IC Simulation and Design: using the BSIM-CMG standard**, Academic Press, 2015.

OPEN ELECTIVE-1
SYLLABUS

Subject Title**: Hardware modelling using VHDL**		
Subject Code**: 22LVS331**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Use the industry-standard hardware description language VHDL into the digital design process.
2. Design VHDL models ranging in complexity from a simple adder to more complex circuits.
3. Understand the synthesis and testing of the models.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**Review of Logic Design Fundamentals**: Combinational logic, Boolean Algebra and Algebraic Simplification, Karnaugh maps, Designing with NAND and NOR gates, Hazards in combinational Networks, Flipflop and Latches, Mealy Sequential Network Design, Design of Moore Sequential Network, Equivalent states and reduction of state Tables, Synchronous Design, Tristate Logic and Buses	**8**	L1,L2, L3,L4
2	**Introduction to VHDL**: VHDL Description of Combinational Networks, Modeling Flipflops using VHDL Processes, VHDL Models for a Multiplexer, Modeling a sequential Machine, Variables, signals, and constants, Arrays, VHDL operators, VHDL Functions, VHDL Procedures, Packages and Libraries.	**8**	L1,L2, L3,L4
3	**Styles of Descriptions**: VHDL Data types, VHDL Styles of Description Data flow Description: Highlights of Data flow Description, Structure of Data flow Description, Data type-vectors, Common VHDL programming Errors	**8**	L1,L2, L3,L4
4	**Designing with programmable Logic Devices**: Read only memories, Programmable Logic Arrays, Programmable Array Logic, Other sequential programmable Logic Devices (PLDs), Generics, Generate statements **Design of Networks for Arithmetic Operations**: Design of serial Adder with Accumulator, Design of Binary Multiplier, Multiplication of signed Binary Numbers, Design of Binary Divider	**8**	L1,L2, L3,L4
5	**Synthesis**: Highlights of synthesis, synthesis information from entity and module, Mapping process in the hardware domain- Mapping of signal assignment, variable L1, L2, L3 assignment, if statements, else-if statements, loop statement. **Hardware Testing and Design for Testability**: Testing Combinational Logic, Testing Sequential Logic.	**8**	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Understand the basic concepts of Digital Design

CO2	Implement various Combinational and sequential circuits using VHDL descriptions. Write simple VHDL programs in different styles.
CO3	Design and verify the functionality of digital circuits (PLA, PAL, PLD) and Arithmetic Operations.
CO4	Identify the suitable Abstraction level for a particular digital design.
CO5	Write the programs more effectively using Verilog tasks and directives. Perform timing and delay Simulation.
Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. "**Digital Systems Design using VHDL**", Charles H. Roth, Jr., The University of Texas at Austin. 2006 reprint, Thomson Asia Pte Ltd, Singapore
2. "**HDL Programming VHDL and Verilog**", Nazeih M. Botros, 2009 reprint, Dreamtech press

REFERENCE BOOKS/WEBLINKS:

1. "**VHDL for Programmable Logic**", Kevin Skahill, Pearson education, 2006

Subject Title**: Pattern Recognition & Machine Learning**		
Subject Code**: 22LVS332**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. To understand the model selection and different types of variables.
2. To study Supervised Learning Linear Regression Models.
3. To learn the various types of Supervised Learning Kernels.
4. To get familiar with Unsupervised Learning.
5. To learn the Probabilistic Graphical Models.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**Introduction:** Probability Theory, Model Selection, The Curse of Dimensionality, Decision Theory, Information **Theory Distributions:** Binary and Multinomial Variables, The Gaussian Distribution, The Exponential Family, Nonparametric Methods.	**8**	L1,L2, L3,L4
2	**Supervised Learning Linear Regression Models:** Linear Basis Function Models, The Bias-Variance Decomposition, Bayesian Linear Regression, Bayesian Model Comparison Classification & Linear Discriminant Analysis: Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Mode	**8**	L1,L2, L3,L4
3	**Supervised Learning Kernels:** Dual Representations, Constructing Kernels, Radial Basis Function Network, Gaussian Processes Support Vector Machines: Maximum Margin Classifiers, Relevance Vector Machines Neural Networks: Feed-forward Network, Network Training, Error Back propagation	**8**	L1,L2, L3,L4
4	**Unsupervised Learning:** Mixture Models: K-means Clustering, Mixtures of Gaussians, Maximum likelihood, EM for Gaussian mixtures, Alternative View of EM**.** **Dimensionality Reduction:** Principal Component Analysis, Factor/Component Analysis, Probabilistic PCA, Kernel PCA, Nonlinear Latent Variable Models	**8**	L1,L2, L3,L4
5	**Probabilistic Graphical Models:** Bayesian Networks, Conditional Independence, Markov Random Fields, Inference in Graphical Models, Markov Model, Hidden Markov Models	**8**	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Identify areas where Pattern Recognition and Machine Learning can offer a solution.
CO2	Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.
CO3	Describe and model data.
CO4	Solve problems in Regression and Classification.

CO5	Discuss main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems.
Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. "**Pattern Recognition and Machine Learning**", Christopher Bishop Springer 2006.

REFERENCE BOOKS/WEBLINKS:

1. Konstantinos Koutroumbas, Sergios Theodoridis, "**Pattern recognition**", Fourth Edition, Academic Press, 2009.
2. Tom M. Mitchell "**Machine Learning: An Artificial Intelligence Approach**", First Edition, Mc Graw Hill, Reprint 2017.

Subject Title**: Internet of Things**		
Subject Code**: 22LVS333**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

6. To understand the concepts of IOT and its applications in today's scenario.
7. To study the IoT network architecture and design.
8. To understand IOT content generation and transport through networks use cases of IoT.
9. To understand the devices employed for IOT data acquisition.

UNIT No.	Syllabus Content	No. of hours	*BTL
1	**What is IoT:**Genesis, Digitization, Impact, Connected Roadways, Buildings, Challenges **IoT Network Architecture and Design:** Drivers behind new network Architectures, Comparing IoT Architectures, M2M architecture, IoT world forum standard, IoT Reference Model, Simplified IoT Architecture.	**8**	L1,L2, L3,L4
2	**IoT Network Architecture and Design:** Core IoT Functional Stack, Layer1(Sensors and Actuators), Layer 2(Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer,IoT Network management. Layer 3(Applications and Analytics) – Analytics vs Control, Data vs Network Analytics, IoT Data Management and Compute Stack	**8**	L1,L2, L3,L4
3	**Engineering IoT Networks:** Things in IoT – Sensors, Actuators, MEMS and smart objects. Sensor networks, WSN, Communication protocols for WSN Communications Criteria, Range, Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks, IoT Access Technologies, IEEE 802.15.4 Competitive Technologies – Overview only of IEEE 802.15.4g, 4e, IEEE 1901.2a Standard Alliances – LTE Cat0, LTE-M, NB-IoT	**8**	L1,L2, L3,L4
4	**Engineering IoT Networks:** IP as IoT network layer, Key Advantages, Adoption, Optimization, Constrained Nodes, Constrained Networks, IP versions, Optimizing IP for IoT. Application Protocols for IoT – Transport Layer, Application Transport layer, Background only of SCADA, Generic web based protocols, IoT Application Layer Data and Analytics for IoT – Introduction, Structured and Unstructured data, IoT Data Analytics overview and Challenges.	**8**	L1,L2, L3,L4
5	**IoT in Industry (Three Use cases):** IoT Strategy for Connected manufacturing, Architecture for Connected Factory Utilities – Power utility, IT/OT divide, Grid blocks reference model, Reference Architecture, Primary substation grid block and automation. Smart and Connected cities –Strategy, Smart city network Architecture, Street layer, city layer, Data center layer, services layer, Smart city security architecture, Smart street lighting.	**8**	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.

- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Understand the basic concepts IoT Architecture and devices employed.
CO2	Analyze the sensor data generated and map it to IoT protocol stack for transport.
CO3	Apply communications knowledge to facilitate transport of IoT data over various available communications media.
CO4	Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.
CO5	Apply knowledge of Information technology to design the IoT applications.

Course outcome and program outcome mapping

CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

2. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry,"**IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things**", 1st Edition, Pearson Education (Cisco Press Indian Reprint), 2017 (ISBN: 978-9386873743)
3. Srinivasa K G, "**Internet of Things**", CENGAGE Leaning India, 2017

REFERENCE BOOKS/WEBLINKS:

3. Vijay Madisetti and ArshdeepBahga, "**Internet of Things (A Hands-on-Approach)**", 1st Edition, VPT, 2014. (ISBN: 978-8173719547)
4. Raj Kamal, "**Internet of Things: Architecture and Design Principles**", 1st Edition, McGraw Hill Education, 2017. (ISBN: 978-9352605224)

Subject Title**: High Frequency GaN Electronic Devices**		
Subject Code**: 22LVS334**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. To understand an integrated treatment of the state of the art in both conventional (i.e., HEMT) scaling as well as unconventional device architectures suitable for amplification and signal generation
2. To understand the both conventional scaled HEMTs (into the deep mm-wave) as well as unconventional approaches to address the mm-wave and THz regimes;
3. To know related physics, as well as numerical simulations and experimental realizations..

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	**Introduction and Overview**: **High Power High Frequency Transistors**: A Material's Perspective: Introduction, Johnson's Figure of Merit, Output Power Figure of Merit 2, Achieving Mobile Carriers for Wide Band Gap Semiconductors, Low Field Mobility Considerations, Channel Temperature Considerations, Heterojunction Advantages	**8**	L1,L2, L3,L4
2	**Isotope Engineering of GaN for Boosting Transistor Speeds**: Introduction, Current Saturation, The Effect of Non-equilibrium LO Phonons is Twofold, Derivation of the Electron-LO Phonon Interaction Hamiltonian, Evaluating the Probability of Scattering into the LO Phonon Mode q, Evaluation of the Phonon Population in Each Mode, Calculating Velocity vs. Field Dependence, Analysis, "Creative Disorder", Summary of the Theoretical Analysis, Experimental Feasibility of Introducing Isotopic Disorder in GaN HEMTs. **Linearity Aspects of High Power Amplification in GaN Transistors**: "Creative Disorder", Summary of the Theoretical Analysis, Experimental Feasibility of Introducing Isotopic Disorder in GaN HEMTs, Overview of Nonlinearity and Its Impacts, Trade-Offs Against Other Metrics, Origins of Non-linearity in GaN HEMTs, Transconductance, Capacitance, Self-heating, Trapping, Large-Signal Modelling, Special Concerns for GaN, Available Models, Physically Derived Models, Circuit Models, Device-Level Design for Linearity, Linearizing the Transconductance Profile, BRIDGE FET Technology.	**8**	L1,L2, L3,L4
3	**III-Nitride Tunneling Hot Electron Transfer Amplifier (THETA)**: Overview of the Chapter Analysis of Hot Electron Transport and Monte Carlo Simulation, Electron Transport Scattering Mechanisms, Monte Carlo Simulation Small Signal Models for High-Frequency Performance ,Effect of Base Thickness and Doping on β, gm, Delay Component, ft, and fmax, Effect of Emitter-Base Current Density on Delay Component, ft, and fmax , Unipolar Transport in III-Nitride Alloys, Polarization-Engineered Vertical Barriers, Leakage in Vertical AlGaN/GaN Heterojunctions, Polarization-Engineered Base-Collector Barriers, Design, Growth, Fabrication, and Characterization of THETA ,Generation I: Common-Emitter Current Gain , Ga Polar THETA with Current Gain >1, N Polar THETA Hot Electron Transport in Vertical	**8**	L1,L2, L3,L4

	AlGaN/GaN Heterostructures, Negative Differential Resistance in III-Nitride THETA, Generation II: Current Gain > 10 in III- Nitride HETs		
4	**Plasma-Wave Propagation in GaN and Its Applications**: Electron PlasmaWaves: Physical Origin, Drude Conductivity and Distributed Models for HEMTs, Hydrodynamic Transport Equations and Non-linear Effects, Electron PlasmaWaves in GaN Experimental Demonstration, Direct Electrical Probing, Quasi-Optical Excitation, Prospective Applications, RTD-Gated HEMT. **Numerical Simulation of Distributed Electromagnetic and Plasma Wave Effect Devices**: Hydrodynamic Modeling of the 2DEG Channel ,Electrodynamic Equations (or Maxwell's Equation), Finite Difference TimeDomain (FDTD) Solution, Time-Space Discretization of HD Equations, Time-Space Discretization of Maxwell'sEquation 4 Verification Using Analytical Models and Experimental Data , Model Validation Via Analytical Method , Model Validation Via Prior Measurements 5 HEMT-Based Terahertz Emitters Using PlasmaWaveInstability , Modeling of HEMT-Based Terahertz Emitters, Full-Wave Hydrodynamic Modeling of Terahertz Emissions from an Short Channel HEMT [24], Dyakonov-Shur Instability, Instability Mechanism , Instability inUngated InGaAs HEMT,	**8**	L1,L2, L3,L4
5	**Resonant Tunneling Transport in Polar III-Nitride**: Introduction, Background on Resonant Tunneling Devices, III-Nitride-Based Resonant Tunneling Devices, Polar Double-Barrier Heterostructures, Molecular Beam Epitaxy of III-Nitride RTDs, GaN/AlN Resonant Tunneling Diodes, Polar RTD Model,New Tunneling Features in Polar RTDs, Polar RTD at Resonance, Polarization- Induced Threshold Voltage,	**8**	L1,L2, L3,L4

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Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Describe the role and impact of nitrogen isotopic selection in material growth and its impact on carrier transport for increasing device speed and power.
CO2	Analyse two distinct perspectives on novel approaches for improving the linearity of GaN-based devices (a key metric for emerging high-speed communications applications) in terms of unconventional device concepts in the III-N material system.
CO3	Analyse hot-carrier injection-based devices, plasma-wave-based devices, and resonant tunneling diodes.
CO4	Understand the emergence of high-speed devices demands new techniques for characterization of devices and also new approaches to numerical simulation of devices.
CO5	Describe emerging noncontact fabrication and characterization techniques for ultrahigh-speed devices

Course outcome and program outcome mapping

CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Patrick Fay, Debdeep Jena, Paul Maki, "**High-Frequency GaN Electronic Device**", Springer International Publishing, 2020

REFERENCE BOOKS/WEBLINKS:

1. Farid Medjdoub, "**Gallium Nitride (GaN): Physics, Devices, and Technology**", 1st Edition, CRC press, 2015.

BOS Chairman Dean(Academics) Principal

Subject Title**: Advances in Image Processing**		
Subject Code**: 22LVS335**	No. of Credits**: 03 = 2:0:0:2 (L:T:P:S)**	No. of lecture hours per week**: 03**
Exam Duration**: 3 Hours**	CIE + (Assignment + Seminar) + SEE = **40+10+50 =100**	Total No. of lecture hours**: 40**

Course Learning Objectives: This course will enable the students to:

1. Acquire fundamental knowledge in understanding the representation of the digital image and its properties
2. Equip with some pre-processing techniques required to enhance the image for further analysis purpose.
3. Select the region of interest in the image using segmentation techniques.
4. Represent the image based on its shape and edge information.
5. Describe the objects present in the image based on its properties and structure.

UNIT No.	**Syllabus Content**	**No. of hours**	***BTL**
1	The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.	**8**	L1,L2, L3,L4
2	Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.	**8**	L1,L2, L3,L4
3	Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post processing.	**8**	L1,L2, L3,L4
4	Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.	**8**	L1,L2, L3,L4
5	Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and watersheds	**8**	L1,L2, L3,L4

*__BTL__: Blooms Taxonomy Level, **L:T:P** = Lecture: Tutorial : Practical

Note:

- Each Unit will have internal choice for SEE.
- The internal assessment will be based on CIE marks, Assignments, Seminar and Group Activities.

COURSE OUTCOMES:

After studying this course, students will be able to:

CO1	Understand the representation of the digital image and its properties
CO2	Apply pre-processing techniques required to enhance the image for its further analysis.
CO3	Use segmentation techniques to select the region of interest in the image for analysis
CO4	Represent the image based on its shape and edge information.
CO5	Describe the objects present in the image based on its properties and structure.

Course outcome and program outcome mapping	
CO1	PO1,PO2,PO3,PO8,PO9,PO10
CO2	PO1, PO2, PO8,PO9,PO10
CO3	PO1, PO2,PO8,PO9,PO10
CO4	PO1, PO8,PO9,PO10
CO5	PO1, PO8,PO9,PO10

TEXT BOOKS:

1. Milan Sonka, Vaclav Hlavac, Roger Boyle, "**Image Processing, Analysis, and Machine Vision**", Fourrth Edition, CENGAGE, 2008
2. Geoff Doughertry, **Digital Image Processing for Medical Applications**, Cambridge university Press, 2010 Cengage Learning, 2013, ISBN: 978-81-315-1883-0

REFERENCE BOOKS/WEBLINKS:

1. S.Jayaraman, S Esakkirajan, T.Veerakumar, **Digital Image Processing**, Tata McGraw Hill, 2011
2. Rafael C. Gonzalez and Richard E. Woods," **Digital Image Processing**", 3rd edition, Pearson Education, 2008.