Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY

(An Autonomous Institute affiliated to VTU, Accredited by NAAC with 'A' grade)

BDA Outer Ring Road, Mallathalli,Bengaluru-56

Board Of Studies 2022-23

Proposed UG
Scheme and Syllabus

For

Academic Year (AY) : 2022-23

Submitted by

Department of Electronics and Communication Engineering

To

DEAN (Academic)

For Seeking Approval from the Academic Council

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.
(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

Ref. No: AIT /EC /BOS / /2021-22 **Date**: 23-07-2022

To
Dean (Academic)
Dr. Ambedkar Institute of Technology
Bengaluru-56

Sir,

Sub: Regarding the details of the BOS meeting held on 23-07-2022

The BOS meeting of the department was held in the department of the Electronics and communication Engineering on Saturday, 23-07-2022.

The BOS committee has approved the following:

1. Approved the NEP based syllabus of Basic Electronics and Communication Engineering and for the I/II Semester of UG Courses for the academic year 2022-23 (Batch-2022).
2. Approved the NEP based Scheme for all the semesters (III to VIII semesters) of UG Course for the academic year 2022-23.
3. Approved the NEP based Syllabus for III and IV semesters of UG Course for the academic year 2022-23.
4. Approved the Scheme and Syllabus for V to VIII semesters of UG Course for the academic year 2022-23.
5. Approved the List of BOE members.
6. Approved the list of Valuers / Examiners.

Thanking you

CHAIRMAN BOS
Dept. of ECE

Enclosures:

1. List of Members of BOS.
2. Curriculum Design –UG
3. Minutes of the BOS Meeting.
4. NES based Scheme & Syllabus of I/II Semester Basic Electronics and Communication Engineering for the academic year 2022-23.
5. NEP based Scheme & Syllabus of 3rd and 4th Semesters for the academic year 2022-23.
6. Scheme & Syllabus of 5th and 6th Semesters for the academic year 2022-23.
7. Scheme & Syllabus of 7th and 8th Semesters for the academic year 2022-23.
8. List of BOE Members.
9. List of valuers / Examiners.

Members of BOS:

Sl No.	*CATEGORY*	*Nomination of the Committee*	*Name of the Person with Designation*
1	Head of the Department	**Chairperson**	Dr. Ramesh.S Professor and Head Department of ECE, Dr.AIT, Bengaluru-56
2	Faculty Members at Different Levels Bearing Different Specializations	**Member 1.**	Dr.Umadevi.H Professor, Department of ECE, Dr.AIT, Bengaluru-56
		Member 2.	Dr. Mahalinga V Mandi, Professor, Department of ECE, Dr.AIT, Bengaluru-56
		Member 3.	Smt. Sudha.B.S. Associate Professor, Department of ECE, Dr.AIT, Bengaluru-56
		Member 4.	Dr.Shivaputra Assistant Professor Department of ECE, Dr.AIT, Bengaluru-56
		Member 5.	Smt. Meenakshi.L.R. Assistant Professor, Department of ECE, Dr.AIT, Bengaluru-56
		Member 6.	Mr. Mohan Kumar V Assistant Professor, Department of ECE, Dr.AIT, Bengaluru-56
		Member 7.	Dr. Jambunath S Baligar Associate Professor Department of ECE, Dr.AIT, Bengaluru-56
		Member 8.	Dr. Chetan. S Assistant Professor, Department of ECE, Dr.AIT, Bengaluru-56

3	Subject Experts from outside the College Nominated by Academic Council	**Member 1.**	Dr. Devendra Jalihal Professor, EEE department IIT Madras, Chennai-600 036
		Member 2.	Prof. Santanu Mahapatra Professor, Department of Electronic Systems Engineering, Indian Institute of Science Bangalore, Bengaluru- 560012
		Member 3.	Dr. Mrityunjaya V Latte Former Principal JSS Academy of Technical Education, Dr. Vishnuvardhan Road, Uttarahalli – Kengeri Main Road, Bengaluru- 560 045
		Member 4.	Prof. P.Nagaraju Associate Professor, Dept. of TCE, RVCE, Bengaluru-560 059
4	Expert from IET Ayodhya	**Member 5.**	Prof. Ramapati Mishra Director, Former HOD, Dept. of ECE IET Ayodya, UP India
5	Expert from outside College, Nominated by Vice Chancellor (VTU)	**VTU Nominee**	Dr. Manjunaik N Professor, Department of ECE, UBDT, Davangere, Karnataka
	Representative from Industry /Corporate Sector/Allied area related to Placement Nominated by Academic council	**Member 1.**	Mr. Kubendra.K Senior Design Engineer VLSI Group, Samsung India,Outer ring Road, Near Marathahalli, Bengaluru

6		**Member 2.**	Dr. J. Krishna Kishore Senior Scientist, ISRO Satellite Centre, Bangalore – 560017
		Member 3.	Mr. Arun Chandrashekar Principal Scientist, INTEL Corporation, Bengaluru,
		Member 4.	Mr. Manjunath B Senior Manger HR, Wistron, India Bengaluru,
7	Post Graduate Meritorious alumnus nominated by Principal	**Member**	Mr. Premkumar M N Senior Manager, Intel, India Bengaluru

CHAIRMAN

BOS Dept. of ECE

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.
(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

MINUTES OF THE MEETING
OF THE
BOARD OF STUDIES 2022-23

DATED: Saturday, 23rd July 2022

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BEGALURU – 560056.
(An Autonomous Institution Affiliated to Visvesvaraya Technological University, Belgaum)

Department of Electronics & Communication Engineering

BOS Meeting Notice

Sub: Board of Studies Meeting is convened on 23-07-2022

With reference to the above subject, Board of Studies Meeting of the department is convened on Saturday, the 23rd July 2022 at 11:00 a.m. in Department of ECE for finalizing the scheme and syllabus of UG in B.E. (E & C) and PG in M.Tech in VLSI Design and Embedded Systems for the academic year 2022-23 with the following agenda.

Agenda:

1. Approval of the NEP Based Scheme of 1st to 8th Semesters B.E (E &C) for the Batch-2022
2. Approval of the NEP Based Scheme and Syllabus of 3rd & 4th Semesters B.E(E & C) for the Batch -2021
3. Approval of the Scheme and Syllabus of 5th to 8th Semester B.E(E & C) for the Batch-2020
4. Approval of the Scheme and Syllabus of 7th to 8th Semester B.E(E & C) for the Batch-2019
5. Approval of Syllabus of Basic Electronics and Communication Engineering (21ECT104/204) for 1st /2nd Semester for the Batch 2022.
6. Approval of Scheme and Syllabus for III & IV Semesters for the Batch 2021.
7. Approval of the Scheme and Syllabus for the 1st and 2nd Semester PG for the Batch-2022
8. Approval of the Scheme and Syllabus for the 3rd and 4th Semester PG for the Batch-2021.
9. Approval of the courses for the Minor Degree
10. Approval of List of Examiners

Minutes of Board of Studies (BOS) Meeting:

The Meeting of Board of Studies (BOS) of department Electronics and Communication Engineering was held on 23-07-2022 at 11:00 a.m. under the Chairmanship of the Dr. Ramesh S, Professor and Head, Department of Electronics and Communication Engineering in the department of Electronics and Communication Engineering.

At the very outset, the Chairman welcomed all the Internal and External members of BOS to the meeting and gave a preliminary presentation on the agenda items with reference to the scheme and syllabus of UG for the academic year 2022-23

The chairman along with academic coordinator(s) gave a detailed presentation of the courses to be offered to the students in both Core and Elective subjects in semester wise at the Under Graduate level and also briefed the members about the Curriculum Design of the Department for the UG Course.

PROCEEDINGS/RESOLUTIONS:

The following are the Suggestions of the members of BOS with reference to the presentations:

- In Basic Electronics and Communication Engineering, advanced topics like, BJT FET are added as self-study topics.
- In Basic Electronics and Communication Engineering, AM, FM and PM are too much advanced topics for non-electronics students.
- In Basic Electronics and Communication Engineering, Simplification of Boolean Expressions concepts needs to be added.
- Information Theory Coding and Machine Learning subjects may be made core subjects instead of offering them as elective subjects.
- Committee discussed and finalized the following two courses to be offered for Inter/Intra Department Internship for students studying in II semester:

1.Microcontroller and its applications

2. MATLAB and its applications

Finally, the BOS members approved the following after incorporating the suggested modifications

- Approved the Curriculum Design for the semesters I to VIII of UG Course for the students of the Batch 2022
- Approved the NEP Based Syllabus of Basic Electronics and Communication Engineering for the semesters I/II of UG Course for the academic year 2022-23.
- Approved the NEP Based Scheme and syllabus for the semesters III and IV of UG Course for the academic year 2022-23.
- Approved the Scheme and syllabus for all the semesters V to VIII of UG Course for the academic year 2022-23.
- Approved the courses for the Minor Degree
- Approved the List of BOE members.
- Approved the list of Valuers / Examiners.

CHAIRMAN

BOS Dept. of ECE

BOS Coordinators	**Signatures**
1. Prof. B. S. Sudha	
2. Mr. Anand H D	

List of BOE Members:

SL. NO.	NAME AND ADDRESS
1.	Dr. Ramesh S. Professor and Head, Department of ECE
External BOE members:	
1.	Dr. Dinesh P., Professor and Dean, Department of ECE, DSCE, Bengaluru
2.	Prof. Nagraju P, Associate Professor, Department of TCE, RVCE, Bengaluru
3.	Dr. Rajeshwari Hegde, Professor and Head, Department of TCE, BMSCE, Bengaluru-19
4.	Dr. Revanna, Associate Professor, Department of ECE, Govt. Engineering College, Ramanagara
Internal BOE Members:	
1.	Dr. Umadevi H., Professor
2.	Smt. Sudha B. S., Associate Professor
3.	Dr. Shivaputra, Assistant Professor
4.	Smt. Meenakshi L. Rathod, Assistant Professor
5.	Mr. Mohankumar V., Assistant Professor
6.	Smt. Girija S., Assistant Professor

CHAIRMAN

BOS Dept. of ECE

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

Typical Curriculum framework for B.E. Degree Programme.

SN	Subject Area and Code	AICTE Breakup of Credits	Average No. of Credits
1	Humanities and Social Science including Management Courses	12*	10
2	Basic Science Courses (Physics, Chemistry and Mathematics)	25*	23
3	Engineering Science Courses including, Engineering Graphics and Design, Basics of Electrical / Electronics / Mechanical / Computer / Civil, Problem Solving etc.	24*	20
4	Professional Core Courses	48*	43
5	Professional Elective Courses relevant to chosen Specialization / Branch	18*	14
6	Open Subjects – Electives from other technical, emerging, arts, commerce and NCC / NSS subjects / Ability Enhancement Courses	18*	14
7	Mini and Major Project work / Seminar / Summer Internship and Research / Industrial Internship	15*	32
8	Mandatory Courses such as Environmental Sciences, Induction Program, Indian Constitution, Universal Human Values, Kannada.	No Credits	04
	Total	**160***	**160**

Credit break down/distribution for all semesters BE programme	
Semester	Credits
I & II	20 + 20 = 40
III	18
IV	22
V	18
VI	22
VII	24
VIII	16
Total	**160**

***Minor variation is allowed as per need of the respective discipline.**

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BENGALURU-560 056

(An Autonomous Institution Affiliated To VTU, Belagavi)

Department Of Electronics & Communication Engineering

DETAILS OF CURRICULUM DESIGN UNDER AUTONOMY (Batch - 2020)

Sl. N0.	Category	No. of credits								Credit range as per VTU guidelines (175 credits)	Average number of credits (Typical)	Actual credit allocation
		Sem I	Sem II	Sem III	Sem IV	Sem V	Sem VI	Sem VII	Sem VIII	Min-Max		
A	**Humanities, Social Sciences and Management (HSMC)**									05-10	**10**	**14**
1.	English		01									
2.	Kannada	01										
3.	Constitution of India and Professional Ethics			01								
4.	Management and Entrepreneurship						03					
5.	Environmental Studies				01							
6.	Intellectual Property Rights					03						
7.	Cost Management and Engineering Projects (CMEP)/Occupational and safety and Health Administration (OSHA)							02	02			

Sl. N0.	Category	No. of credits								Credit range as per VTU guidelines (175 credits)	Average number of credits (Typical)	Actual credit allocation
B	**Basic Sciences (BSC)**									10-20	**28**	**24**
1.	Engineering Physics	04										
2.	Physics Lab	01										
3.	Engineering Chemistry		04									
4.	Chemistry Lab		01									
5.	Differential Equations & Complex Variables	04										
6.	Calculus and Linear Algebra		04									
7.	Transform Calculus and Boundary Value Problems			03								
8.	Numerical Methods and Statistical Techniques				03							
C	**Engineering Sciences (ESC)**									15-20	**20**	**20**
1.	Basic Electrical Engineering	03										
2.	Basic Electrical Engineering Lab	01										
3.	Civil Engineering and Mechanics	03										
4.	C Programming for Problem Solving		03									
5.	Programming for Problem Solving Lab		01									
6.	Elements of Mechanical Engineering		03									
7.	Engineering Graphics and Design	03										

Sl. N0.	Category	No. of credits								Credit range as per VTU guidelines (175 credits)	Average number of credits (Typical)	Actual credit allocation
8.	Basic Electronics		03									
D	**Professional Course-Core (PCC)**									30-40	**64**	**79**
1.	Electronic Devices			03								
2.	Digital Electronics			04								
3.	Network Theory			04								
4.	Signals and Systems			04								
5.	Power Electronics & Instrumentation			03								
6.	Electronic Devices and Instrumentation Laboratory			01								
7.	Digital Electronics Laboratory			01								
8.	Analog Circuits				03							
9.	Principles of Communication Systems				04							
10.	Electromagnetic Waves				03							
11.	Verilog HDL				04							
12.	Control Systems				04							
13.	Analog Circuits and Communication Laboratory				01							
14.	HDL Laboratory				01							

Sl. N0.	Category	No. of credits								Credit range as per VTU guidelines (175 credits)	Average number of credits (Typical)	Actual credit allocation
15.	Microprocessor and Microcontroller					03						
16.	Digital Signal Processing					04						
17.	Digital Communication					04						
18.	Object Oriented Programming C++					03						
19.	Digital Signal Processing Lab					01						
20.	Microcontroller Lab					01						
21.	Embedded Systems						03					
22.	Computer Communication Network						04					
23.	CMOS VLSI Design						04					
24.	Embedded systems Lab						01					
25.	VLSI Lab						01					
26.	Wireless Communication							04				
27.	Microwave and Antenna							04				
28.	Advance Communication Lab							01				
29.	Computer Communication Network Lab							01				
E	**Professional Course Elective (PEC)**									10-15	**20**	**12**
1.	Elective – 1 (PECEL 1)					03						
2.	Elective – 2 (PECEL 2)						03					
3.	Elective – 3 (PECEL 3)							03				
4.	Elective – 4 (PECEL 4)							03				

Sl. N0.	Category	No. of credits								Credit range as per VTU guidelines (175 credits)	Average number of credits (Typical)	Actual credit allocation
F	**Other Open Elective Course (OEC)**									05-10	**08**	**09**
1.	Open Elective-A (OE-A)					03						
2.	Open Elective-B (OE-B)						03					
3.	Open Elective-C (OE-C)							03				
G	**Project Work (PROJ)**									10-15	**25**	**17**
1.	Mini Project						02					
2.	Project Work-I							02				
3.	Project Work-II								10			
4.	Seminar								01			
5.	Internship								02			
	Total No. of Credits	**20**	**20**	**24**	**24**	**25**	**24**	**23**	**15**		**175**	**175**

Chairman BOS

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BENGALURU-560 056

(An Autonomous Institution Affiliated To VTU, Belagavi)

Department Of Electronics & Communication Engineering

DETAILS OF CURRICULUM DESIGN UNDER AUTONOMY (Batch - 2019)

Sl. N0.	Category	No. of credits								Credit range as per VTU guidelines (175 credits)	Average number of credits (Typical)	Actual credit allocation
		Sem I	Sem II	Sem III	Sem IV	Sem V	Sem VI	Sem VII	Sem VIII	Min-Max		
A	**Humanities, Social Sciences and Management (HSMC)**									05-10	**10**	**14**
1.	English		01									
2.	Kannada	01										
3.	Constitution of India and Professional Ethics			01								
4.	Management and Entrepreneurship						03					
5.	Environmental Studies				01							
6.	Intellectual Property Rights					03						
7.	Cost Management and Engineering Projects (CMEP)/Occupational and safety and Health Administration (OSHA)							02	02			

Sl. N0.	Category	No. of credits								Credit range as per VTU guidelines (175 credits)	Average number of credits (Typical)	Actual credit allocation
B	**Basic Sciences (BSC)**									10-20	**28**	**24**
1.	Engineering Physics	04										
2.	Physics Lab	01										
3.	Engineering Chemistry		04									
4.	Chemistry Lab		01									
5.	Differential Equations & Complex Variables	04										
6.	Calculus and Linear Algebra		04									
7.	Transform Calculus and Boundary Value Problems			03								
8.	Numerical Methods and Statistical Techniques				03							
C	**Engineering Sciences (ESC)**									15-20	**20**	**20**
1.	Basic Electrical Engineering	03										
2.	Basic Electrical Engineering Lab	01										
3.	Civil Engineering and Mechanics	03										
4.	C Programming for Problem Solving		03									
5.	Programming for Problem Solving Lab		01									
6.	Elements of Mechanical Engineering		03									
7.	Engineering Graphics and Design	03										

Sl. N0.	Category	No. of credits								Credit range as per VTU guidelines (175 credits)	Average number of credits (Typical)	Actual credit allocation
8.	Basic Electronics		03									
D	**Professional Course-Core (PCC)**									30-40	**64**	**79**
1.	Electronic Devices			03								
2.	Digital Electronics			04								
3.	Network Theory			04								
4.	Signals and Systems			04								
5.	Power Electronics & Instrumentation			03								
6.	Electronic Devices and Instrumentation Laboratory			01								
7.	Digital Electronics Laboratory			01								
8.	Analog Circuits				03							
9.	Principles of Communication Systems				04							
10.	Electromagnetic Waves				03							
11.	Verilog HDL				04							
12.	Control Systems				04							
13.	Analog Circuits and Communication Laboratory				01							
14.	HDL Laboratory				01							

Sl. N0.	Category	No. of credits								Credit range as per VTU guidelines (175 credits)	Average number of credits (Typical)	Actual credit allocation
15.	Microprocessor and Microcontroller					03						
16.	Digital Signal Processing					04						
17.	Digital Communication					04						
18.	Object Oriented Programming C++					03						
19.	Digital Signal Processing Lab					01						
20.	Microcontroller Lab					01						
21.	Embedded Systems						03					
22.	Computer Communication Network						04					
23.	CMOS VLSI Design						04					
24.	Embedded systems Lab						01					
25.	VLSI Lab						01					
26.	Wireless Communication							04				
27.	Microwave and Antenna							04				
28.	Advance Communication Lab							01				
29.	Computer Communication Network Lab							01				
E	**Professional Course Elective (PEC)**									10-15	**20**	**12**
1.	Elective – 1 (PECEL 1)					03						
2.	Elective – 2 (PECEL 2)						03					
3.	Elective – 3 (PECEL 3)							03				
4.	Elective – 4 (PECEL 4)							03				

Sl. N0.	Category	No. of credits								Credit range as per VTU guidelines (175 credits)	Average number of credits (Typical)	Actual credit allocation
F	**Other Open Elective Course (OEC)**									05-10	**08**	**09**
1.	Open Elective-A (OE-A)					03						
2.	Open Elective-B (OE-B)						03					
3.	Open Elective-C (OE-C)							03				
G	**Project Work (PROJ)**									10-15	**25**	**17**
1.	Mini Project						02					
2.	Project Work-I							02				
3.	Project Work-II								10			
4.	Seminar								01			
5.	Internship								02			
	Total No. of Credits	**20**	**20**	**24**	**24**	**25**	**24**	**23**	**15**		**175**	**175**

Chairman BOS

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

(Applicable to 2022 batch)

Scheme of Teaching and Examination for I /II Semester B.E., (Common to all B.E. Programmes) Academic Year:2022-23

Physics Cycle : I/II Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hours/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BS	21MAT101	Calculus and Linear Algebra	Mathematics	3	2	0	0	5	3	50	50	100	4
		21MAT201	Advanced Calculus and Numerical methods											
2	BS	21PHT102/ 21PHT202	Engineering Physics	Physics	3	0	0	0	3	3	50	50	100	3
3	ES	21EET103/ 21EET203	Basic Electrical Engineering	Electrical	2	2	0	0	4	3	50	50	100	3
4	ES	21CVT104/ 21CVT204	Elements of Civil Engineering & Mechanics	Civil	3	0	0	0	3	3	50	50	100	3
5	ES	21MED105/ 21MED205	Computer aided Engineering Drawing	Mechanical	2	0	2	0	4	3	50	50	100	3
6	BS	21PHL106/ 21PHL206	Engineering Physics Lab	Physics	0	0	2	0	2	3	50	50	100	1
7	ES	21EEL107/ 21EEL207	Basic Electrical lab	Electrical	0	0	2	0	2	3	50	50	100	1
8	HS	21HST108	Communicative English	Humanities	1	0	1*	0	2	2	50	50	100	1
		21HST208	Professional writing skills in English											
9	AE	21HST109	Health and Wellness	Humanities	1	0	1*	0	2	2	50	50	100	1
		21CVT209	Rural Development	Civil										
10	MC	21HSN110	Career Development skill-I	Humanities	1	0	1*	0	2	--	50	-	PP/NP	0
		21HSN210	Career Development skill-II											
									Total	29		500	450	900	20

Note: BS: Basic Science Course, ES: Engineering Science Course, HS: Humanities & Social Science Course,
AE: Ability Enhancement Course, MC: Mandatory Course, * No practical evaluation,
L: Lecture, T:Titorial, P:Practical/drawing, S:Self study, CIE: Continuous Internal Evaluation, SEE: Semester End Examination

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

Scheme of Teaching and Examination for I /II Semester B.E., (Common to all B.E. Programmes) Academic Year:2022-23

Chemistry Cycle: I/II Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BS	21MAT101	Calculus and Linear Algebra	Mathematics	3	2	0	0	5	3	50	50	100	4
		21MAT201	Advanced Calculus and Numerical methods											
2	BS	21CHT102/ 21CHT202	Engineering Chemistry	Chemistry	3	0	0	0	3	3	50	50	100	3
3	ES	21CST103/ 21CST203	Problem solving through Programming	Computer Science	2	2	0	0	4	3	50	50	100	3
4	ES	21ECT104/ 21ECT204	Basic Electronics and Communication Engineering	Electronics	3	0	0	0	3	3	50	50	100	3
5	ES	21MET105/ 21MET205	Elements of Mechanical Engineering	Mechanical	2	2	0	0	4	3	50	50	100	3
6	BS	21CHL106/ 21CHL206	Engineering Chemistry Laboratory	Chemistry	0	0	2	0	2	3	50	50	100	1
7	ES	21CSL107/ 21CSL207	Computer Programming Laboratory	Computer Science	0	0	2	0	2	3	50	50	100	1
8	HS	21HST108	Communicative English	Humanities	1	0	1*	0	2	2	50	50	100	1
		21HST208	Professional writing skills in English											
9	AE	21CVT109	Rural Development	Civil	1	0	1*	0	2	2	50	50	100	1
		21HST209	Health and Wellness	Humanities										
10	MC	21HSN110	Career Development skill-I	Humanities	1	0	1*	0	2	----	50	--	PP/NP	0
		21HSN210	Career Development skill-II											
								Total	30		500	450	900	20

Note: BS: Basic Science Course, ES: Engineering Science Course, HS: Humanities & Social Science Course, AE: Ability Enhancement Course, MC: Mandatory Course, * No practical evaluation,
L: Lecture, T:Titorial, P:Practical/drawing, S:Self study, CIE: Continuous Internal Evaluation, SEE: Semester End Examination

Note –At the end of the second-semester summer internship shall be carried out – based on inter/intra institutional activities credited in the third semester. University /Institutions may swap few courses between a FIRST and SECOND semester to balance the workload teaching and laboratory schedule

Summer Internship - I: All the students admitted shall have to undergo a mandatory summer internship of 03 weeks during the vacation of II semesters. Summer Internship shall include Inter / Intra Institutional activities. Internship A University Viva-voce examination shall be conducted during III semesters and the prescribed credit shall be included in III semesters. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Scheme of Teaching and Examination effective from the Academic Year 2022-23

III Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BSC	21MAT301	Transform Calculus, Fourier Series and Numerical Techniques	Mathematics	2	2	0	0		03	50	50	100	3
2	IPCC	21ECT302	Digital System Design Using Verilog	ECE	3	0	2			03	50	50	100	4
3	IPCC	21ECT303	Basic Signal Processing	ECE	3	0	2			03	50	50	100	4
4	PCC	21ECT304	Analog Electronic Circuits	ECE	3	0	0	1		03	50	50	100	3
5	PCC	21ECL305	Analog & Digital Electronics Lab	ECE	0	0	2			03	50	50	100	1
6	UHV	21HST306	Social Connect and Responsibility		0	0	1			01	50	50	100	1
7	HSS	21HST307	Samskrutika Kannada		1	0	0			01	50	50	100	1
		21HST307	Balake Kannada											
		OR												
		21HST308	Constitution of India and Professional Ethics											
8	AEC	21ECT309X	Ability Enhancement Course - III							01	50	50	100	1
9	HSSC	21HSN310	Professional Skills		1	0	0	1		02	50	----	PP/NP	0
Total											400	400	800	18
10	Scheduled activities from III to VIII semesters	21HSHS803	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE)(Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester. The activities shall be carried out between III semester to VIII semester (for 5 semesters). SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE and Yoga activities.									
		21HSN803	Physical Education (PE) (Sport and activities)	PE										
		21HSN803	Yoga	Yoga										
Course Prescribed to Lateral Entry Diploma Holders Admitted to III Semester B.E. Program														
11		21MAN311	Additional Mathematics-I	Maths	1	0	0	1		02	50	----	PP/NP	0

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course. **L** –Lecture, **T** – Tutorial, **P**- Practical/ Drawing, **S** – Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD** Teaching Department, **PSB:** Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and 21KBK37/47 **Balake Kannada** is for non-Kannada speaking, reading, and writing students

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

21INT49Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internship of 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) Placement Training: These courses are prescribed for I to IV semesters respectively to the students of BE programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case any student fails to register for the said course/fails to secure the minimum 40% of the prescribed CIE marks, he/she shall be deemed to have secured an **NP (not pass)** grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.			
Ability Enhancement Course - III			
21ECT3091	LD Lab using Pspice / MultiSIM	**21ECT3093**	LIC Lab using Pspice / MultiSIM
21ECT3092	AEC Lab using Pspice / MultiSIM	**21ECT3094**	LabVIEW Programming Basics

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Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Scheme of Teaching and Examination effective from the Academic Year 2022-23

IV Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BSC	21MAT401	Maths for Communication Engineers	Mathematics						03	50	50	100	3
2	IPCC	21ECT402	Digital Signal Processing	ECE	3	0	2			03	50	50	100	4
3	IPCC	21ECT403	Circuit analysis and control systems	ECE	3	0	2			03	50	50	100	4
4	PCC	21ECT404	Communication Theory	ECE	3	0	0	1		03	50	50	100	3
5	PCC	21ECL405	Communication Laboratory I	ECE	0	0	2			03	50	50	100	1
6	AEC	21ECT406	Biology For Engineers		0	0	1			02	50	50	100	2
7	HSSC	21HST407	Samskrutika Kannada		1	0	0			01	50	50	100	1
		21HST407	Balake Kannada											
		OR												
		21HST408	Constitution of India and Professional Ethics											
8	AEC	21ECT409X	Ability Enhancement Course - IV							01	50	50	100	1
9	HSSC	21HSN410	Professional Skills	HSS	1	0	1	0		02	50	----	PP/NP	0
10	UHV	21HSN412	Universal Human Values	Any Department	1	0	0	1		01	50	50	100	1
11	INT	21ECI413	Inter/Intra Institutional Internship	Evaluation By the appropriate authorities	Completed during the intervening period ofII and III semesters by students admitted to first year of BE./B.Tech and during the intervening period of III and IV semesters by Lateral entry students admitted to III semester.					03	100		100	2
									Total		550	450	1000	22
Course Prescribed to Lateral Entry Diploma Holders Admitted to III Semester B.E. Program														
12		21MAN411	Additional Mathematics-II	Maths	1	0	0	1		02	50	----	PP/NP	0

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course. **L** –Lecture, **T** – Tutorial, **P**- Practical/ Drawing, **S** – Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD** Teaching Department, **PSB:** Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and 21KBK37/47 **Balake Kannada** is for non-Kannada speaking, reading, and writing students

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

Internship of 04 weeks during the intervening period of IV and V semesters; 21INT68Innovation/ Entrepreneurship/ Societal based Internship.

(1) All the students shall have to undergo a mandatory internship of 04 weeks during the intervening period of IV and V semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the VI semester grade card.The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be considered under F (fail) grade and shall have to complete during subsequently after satisfying the internship requirements.

(2) Innovation/ Entrepreneurship Internship shall be carried out at industry, State and Central Government /Non-government organizations (NGOs), micro, small and medium enterprise (MSME), Innovation centres or Incubation centres. Innovation need not be a single major breakthrough; it can also be a series of small or incremental changes. Innovation of any kind can also happen outside of the business world. Entrepreneurship internships offers a chance to gain hands on experience in the world of entrepreneurship and helps to learn what it takes to run a

small entrepreneurial business by performing intern duties with an established company. This experience can then be applied to future business endeavours. Start-ups and small companies are a preferred place to learn the business tack ticks for future entrepreneurs as learning how a small business operates will serve the intern well when he/she manages his/her own company. Entrepreneurship acts as a catalyst to open the minds to creativity and innovation. Entrepreneurship internship can be from several sectors, including technology, small and medium-sized, and the service sector.

(3) Societal or social internship. Urbanization is increasing on a global scale; and yet, half the world's population still resides in rural areas and is devoid of many things that urban population enjoy. Rural internship is a work-based activity in which students will have a chance to solve/reduce the problems of the rural place for better living. As proposed under the AICTE rural internship programme, activities under Societal or social internship, particularly in rural areas, shall be considered for 40 points under AICTE activity point programme.

Ability Enhancement Course - IV

21ECT4091	Embedded C Basics	**21ECT4093**	Octave / Scilab for signals
21ECT4092	C++ Basics	**21ECT4094**	DAQ using LabVIEW

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Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

V Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	PCC	21ECT501	Digital Communication	ECE	3	0	0			3	50	50	100	3
2	IPCC	21ECT502	Object Oriented Programming with Java & Data Structures	ECE	3	0	2		3	3	50	50	100	4
3	PCC	21ECT503	Computer Communication Networks	ECE	3	0	0		3	3	50	50	100	3
4	PCC	21ECT504	Microwave Theory & Antennas	ECE	3	0	0		3	3	50	50	100	3
5	PCC	21ECL505	Communication Lab II	ECE	0	0	2		3	3	50	50	100	1
6	AEC	21ECT506	Research Methodology & Intellectual Property Rights	Any Department	2	0	0		2	2	50	50	100	2
7	HSSC	21CV507	Environmental Studies	Civil/Chemistry	1	0	0			1	50	50	100	1
8	AEC	21ECT508	Ability Enhancement Course-V	ECE						1/2	50	50	100	1
9	HSSC	21HSN509	Aptitude and Verbal ability skills		1	0	1	0		2	50	--	PP/NP	0
										Total	450	400	800	18

Ability Enhancement Course - V

21ECT5081	IoT Lab	**21ECT5083**	Antenna Design & Testing
21ECT5082	Communication Simulink Toolbox	**21ECT5084**	Microwaves toolbox

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Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

VI Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	HSSC	21ECT601	Technological Innovation Management and Entrepreneurship								50	50	100	03
2	IPPC	21ECT602	Computer Organization & ARM Microcontrollers	ECE	2	2			4	3	50	50	100	04
3	PCC	21ECT603	VLSI Design & Testing	ECE	3				3	3	50	50	100	03
4	PEC	21ECE604X	Professional Elective -I	ECE	3				3	3	50	50	100	03
5	OEC	21ECE605X	OpenElective-I	ECE	3				3	3	50	50	100	03
6	PCC	21ECL606	VLSI Laboratory	ECE			2		2		50	50	100	01
7	MP	21ECM607	Mini Project	ECE			2		2		50	50	100	03
8	INT	21ECI608	Innovation/Entrepreneurship /Societal Internship								50	50	100	03
9	HSSC	21HSN609	Analytical & Reasoning skills	Placement Cells	2	0	0-		02	--	50	--	PP/NP	00
								Total			500	450	900	22

Research/Industrial Internship - At the End of the sixth / Seventh semester (in two cycles to accommodate all the students of the University) Research/Industrial Internship shall be carried out – Based on industrial/Govt./NGO/MSME/Rural Internship/Innovation/Entrepreneurship. All the students admitted shall have to undergo a mandatory internship of 24 weeks during the vacation of VI/VII semesters. A University Viva-Voce examination shall be conducted during VII/VIII semester and the prescribed credit shall be included in VII/VIII semester. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements. Research internship Students have to take up research internships at Centers of Excellence (CoE) / Study Centers established in the same institute and /or out of the institute at reputed

research organizations / Institutes. A research internship is intended to give you the flavour of current research going on on a particular topic/s. The internships serve this purpose. They help students get familiarized with the field, the skill needed the effort amount and kind of effort required for carrying out research in that field.

Industry internships: This is an extended period of work experience undertaken by university/Institute students looking to supplement their degree with professional development. The students are allowed to prepare themselves for the workplace and develop practical skills as well as academic ones. It also helps them learn to overcome unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with "unexpected contingencies" helps students recognize, appreciate, and adapt to organization realities by tempering knowledge with practical constraints.

Mini-project work: Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini-project can be assigned to an individual student or a group having not more than 4 students. (or Mini Project is a laboratory-oriented course which will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications) CIE procedure for
Mini-project: (i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide. The CIE marks awarded for the Mini-project work, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the college. The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates. SEE for Mini-project: (i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester-end examination (SEE) conducted at the department. (ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester-end examination (SEE) conducted separately at the departments to which the student/s belongs
Open Elective Courses: Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives). Selection of an open elective shall not be allowed if, • The candidate has studied the same course during the previous semesters of the program. • The syllabus content of open electives is similar to that of the Departmental core courses or professional electives. • A similar course, under any category, is prescribed in the higher semesters of the program. • Registration to electives shall be documented under the guidance of the Programme Coordinator/ Advisor/Mentor

Professional Elective Courses-I		**Open Elective Courses-I**	
Subject Code	**Title**	**Subject Code**	**Title**
21ECE6041	Artificial Neural Networks (L:T:P :: 2:2:0)	**21ECE6051**	Communication Engineering (L:T:P :: 3:0:0)
21ECE6042	Cryptography (L:T:P :: 2:2:0)	**21ECE6052**	Microcontrollers (L:T:P :: 3:0:0)
21ECE6043	Python Programming (L:T:P :: 2:0:2)	**21ECE6053**	Basic VLSI Design (L:T:P :: 3:0:0)
21ECE6044	Micro Electro Mechanical Systems (L:T:P :: 3:0:0)	**21ECE6054**	Electronic Circuits with Verilog (L:T:P :: 2:0:2)
		21ECE6055	Sensors & Actuators (L:T:P :: 3:0:0)

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Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

VII Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	PCC	21ECE701	Advanced VLSI	ECE	3	0	0		3	3	50	50	100	3
2	PCC	21ECE702	Optical & Wireless Communication	ECE	2	0	0		3	3	50	50	100	2
3	PEC	21ECE703X	Professional elective Course-II	ECE	3	0	0		3	3	50	50	100	3
4	PEC	21ECE704X	Professional elective Course-III	ECE	3	0	0		3	3	50	50	100	3
5	OEC	21ECE705X	Open elective Course-II		3	0	0		3	3	50		100	3
6	Project	21ECP706	Project work	ECE						3	100	50	200	10
								Total			350	450	700	24

Professional Elective Courses-II		Professional Elective Courses-III		Open Elective Courses-II	
Subject Code	Title	Subject Code	Title	Subject Code	Title
21ECE7031	Advanced Design Tools for VLSI (L:T:P :: 2:0:2)	21ECE7041	IoT & Wireless Sensor Networks (L:T:P :: 3:0:0)	21ECE7051	Optical & Satellite Communication (L:T:P :: 3:0:0)
21ECE7032	Digital Image Processing (L:T:P :: 2:0:2)	21ECE7042	Network Security (L:T:P :: 3:0:0)	21ECE7052	ARM Embedded Systems (L:T:P :: 3:0:0)
21ECE7033	DSP Algorithms & Architecture (L:T:P :: 3:0:0)	21ECE7043	Fabrication technology (L:T:P :: 3:0:0)	21ECE7053	Basic Digital Image Processing (L:T:P :: 2:0:2)
21ECE7034	Biomedical Signal Processing (L:T:P :: 3:0:0)	21ECE7044	Machine Learning with Python (L:T:P :: 2:0:2)	21ECE7054	Basic Digital Signal Processing (L:T:P :: 2:0:2)
21ECE7035	Speech Signal Processing (L:T:P :: 3:0:0)	21ECE7045	Multimedia Communication (L:T:P :: 2:0:2)	21ECE7055	E-waste Management (L:T:P :: 3:0:0)

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Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

VIII Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week				Examination				Credits
					L	T	P	S	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	Seminar	21ECS801	Technical Seminar		One contact hour /week for interaction between the faculty and students				--	100	---	100	01
2	Research Internship/ Industry Internship	21ECI802	Research/Industry Internship*		Two contact hours /week for interaction between the faculty and students.				3 (Batch wise)	100	100	200	15
3	NCMC	21EC803	National Service Scheme (NSS)	NSS	Completed during the intervening period of III semester to VIII semester.				--	50	50	100	--
		21EC803	Physical Education (PE) (Sports & Athletics)	PE									
		21EC803	Yoga	Yoga									
									Total	250	150	400	16

Note: (1) University /Institutions may swap 7th and 8th Semester Course work to accommodate industry/research internship at the end of sixth semester /at the end of seventh semester to balance the workload. (2) Credits earned for the course prescribed will be accounted in 8th semester

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

(Applicable to 2021 batch)

Scheme of Teaching and Examination for I /II Semester B.E., (Common to all B.E. Programmes) Academic Year:2022-23

Physics Cycle : I/II Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hours/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BS	21MAT101	Calculus and Linear Algebra	Mathematics	3	2	0	0	5	3	50	50	100	4
		21MAT201	Advanced Calculus and Numerical methods											
2	BS	21PHT102/ 21PHT202	Engineering Physics	Physics	3	0	0	0	3	3	50	50	100	3
3	ES	21EET103/ 21EET203	Basic Electrical Engineering	Electrical	2	2	0	0	4	3	50	50	100	3
4	ES	21CVT104/ 21CVT204	Elements of Civil Engineering & Mechanics	Civil	3	0	0	0	3	3	50	50	100	3
5	ES	21MED105/ 21MED205	Computer aided Engineering Drawing	Mechanical	2	0	2	0	4	3	50	50	100	3
6	BS	21PHL106/ 21PHL206	Engineering Physics Lab	Physics	0	0	2	0	2	3	50	50	100	1
7	ES	21EEL107/ 21EEL207	Basic Electrical lab	Electrical	0	0	2	0	2	3	50	50	100	1
8	HS	21HST108	Communicative English	Humanities	1	0	1*	0	2	2	50	50	100	1
		21HST208	Professional writing skills in English											
9	AE	21HST109	Health and Wellness	Humanities	1	0	1*	0	2	2	50	50	100	1
		21CVT209	Rural Development	Civil										
10	MC	21HSN110	Career Development skill-I	Humanities	1	0	1*	0	2	--	50	-	PP/NP	0
		21HSN210	Career Development skill-II											
									Total	29		500	450	900	20

Note: BS: Basic Science Course, ES: Engineering Science Course, HS: Humanities & Social Science Course,
AE: Ability Enhancement Course, MC: Mandatory Course, * No practical evaluation,
L: Lecture, T:Titorial, P:Practical/drawing, S:Self study, CIE: Continuous Internal Evaluation, SEE: Semester End Examination

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

Scheme of Teaching and Examination for I /II Semester B.E., (Common to all B.E. Programmes) Academic Year:2022-23

Chemistry Cycle: I/II Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BS	21MAT101	Calculus and Linear Algebra	Mathematics	3	2	0	0	5	3	50	50	100	4
		21MAT201	Advanced Calculus and Numerical methods											
2	BS	21CHT102/ 21CHT202	Engineering Chemistry	Chemistry	3	0	0	0	3	3	50	50	100	3
3	ES	21CST103/ 21CST203	Problem solving through Programming	Computer Science	2	2	0	0	4	3	50	50	100	3
4	ES	21ECT104/ 21ECT204	Basic Electronics and Communication Engineering	Electronics	3	0	0	0	3	3	50	50	100	3
5	ES	21MET105/ 21MET205	Elements of Mechanical Engineering	Mechanical	2	2	0	0	4	3	50	50	100	3
6	BS	21CHL106/ 21CHL206	Engineering Chemistry Laboratory	Chemistry	0	0	2	0	2	3	50	50	100	1
7	ES	21CSL107/ 21CSL207	Computer Programming Laboratory	Computer Science	0	0	2	0	2	3	50	50	100	1
8	HS	21HST108	Communicative English	Humanities	1	0	1*	0	2	2	50	50	100	1
		21HST208	Professional writing skills in English											
9	AE	21CVT109	Rural Development	Civil	1	0	1*	0	2	2	50	50	100	1
		21HST209	Health and Wellness	Humanities										
10	MC	21HSN110	Career Development skill-I	Humanities	1	0	1*	0	2	----	50	--	PP/NP	0
		21HSN210	Career Development skill-II											
								Total	30		500	450	900	20

Note: BS: Basic Science Course, ES: Engineering Science Course, HS: Humanities & Social Science Course, AE: Ability Enhancement Course, MC: Mandatory Course, * No practical evaluation,
L: Lecture, T:Titorial, P:Practical/drawing, S:Self study, CIE: Continuous Internal Evaluation, SEE: Semester End Examination

Note –At the end of the second-semester summer internship shall be carried out – based on inter/intra institutional activities credited in the third semester. University /Institutions may swap few courses between a FIRST and SECOND semester to balance the workload teaching and laboratory schedule

Summer Internship - I: All the students admitted shall have to undergo a mandatory summer internship of 03 weeks during the vacation of II semesters. Summer Internship shall include Inter / Intra Institutional activities. Internship A University Viva-voce examination shall be conducted during III semesters and the prescribed credit shall be included in III semesters. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Scheme of Teaching and Examination effective from the Academic Year 2022-23

III Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BSC	21MAT301	Transform Calculus, Fourier Series and Numerical Techniques	Mathematics	2	2	0	0		03	50	50	100	3
2	IPCC	21ECT302	Digital System Design Using Verilog	ECE	3	0	2			03	50	50	100	4
3	IPCC	21ECT303	Basic Signal Processing	ECE	3	0	2			03	50	50	100	4
4	PCC	21ECT304	Analog Electronic Circuits	ECE	3	0	0	1		03	50	50	100	3
5	PCC	21ECL305	Analog & Digital Electronics Lab	ECE	0	0	2			03	50	50	100	1
6	UHV	21HST306	Social Connect and Responsibility		0	0	1			01	50	50	100	1
7	HSSC	21HST307	Samskrutika Kannada		1	0	0			01	50	50	100	1
		21HST307	Balake Kannada											
		OR												
		21HST308	Constitution of India and Professional Ethics											
8	AEC	21ECT309X	Ability Enhancement Course - III							01	50	50	100	1
9	HSSC	21HSN310	Professional Skills		1	0	0	1		02	50	----	PP/NP	0
Total											400	400	800	18
10	Scheduled activities from III to VIII semesters	21HSHS803	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE)(Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester. The activities shall be carried out between III semester to VIII semester (for 5 semesters). SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE and Yoga activities.									
		21HSN803	Physical Education (PE) (Sport and activities)	PE										
		21HSN803	Yoga	Yoga										
Course Prescribed to Lateral Entry Diploma Holders Admitted to III Semester B.E. Program														
11		21MAN311	Additional Mathematics-I	Maths	1	0	0	1		02	50	----	PP/NP	0

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course. **L** –Lecture, **T** – Tutorial, **P**- Practical/ Drawing, **S** – Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD** Teaching Department, **PSB:** Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and 21KBK37/47 **Balake Kannada** is for non-Kannada speaking, reading, and writing students

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

21INT49Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internship of 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) Placement Training: These courses are prescribed for I to IV semesters respectively to the students of BE programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case any student fails to register for the said course/fails to secure the minimum 40% of the prescribed CIE marks, he/she shall be deemed to have secured an **NP (not pass)** grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.			
Ability Enhancement Course - III			
21ECT3091	LD Lab using Pspice / MultiSIM	**21ECT3093**	LIC Lab using Pspice / MultiSIM
21ECT3092	AEC Lab using Pspice / MultiSIM	**21ECT3094**	LabVIEW Programming Basics

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Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Scheme of Teaching and Examination effective from the Academic Year 2022-23

IV Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BSC	21MAT401	Maths for Communication Engineers	Mathematics						03	50	50	100	3
2	IPCC	21ECT402	Digital Signal Processing	ECE	3	0	2			03	50	50	100	4
3	IPCC	21ECT403	Circuit analysis and control systems	ECE	3	0	2			03	50	50	100	4
4	PCC	21ECT404	Communication Theory	ECE	3	0	0	1		03	50	50	100	3
5	PCC	21ECL405	Communication Laboratory I	ECE	0	0	2			03	50	50	100	1
6	AEC	21ECT406	Biology For Engineers		0	0	1			02	50	50	100	2
7	HSSC	21HST407	Samskrutika Kannada		1	0	0			01	50	50	100	1
		21HST407	Balake Kannada											
		OR												
		21HST408	Constitution of India and Professional Ethics											
8	AEC	21ECT409X	Ability Enhancement Course - IV							01	50	50	100	1
9	HSSC	21HSN410	Professional Skills	HSS	1	0	1	0		02	50	----	PP/NP	0
10	UHV	21HSN412	Universal Human Values	Any Department	1	0	0	1		01	50	50	100	1
11	INT	21ECI413	Inter/Intra Institutional Internship	Evaluation By the appropriate authorities	Completed during the intervening period ofII and III semesters by students admitted to first year of BE./B.Tech and during the intervening period of III and IV semesters by Lateral entry students admitted to III semester.					03	100		100	2
									Total		550	450	1000	22
Course Prescribed to Lateral Entry Diploma Holders Admitted to III Semester B.E. Program														
12		21MAN411	Additional Mathematics-II	Maths	1	0	0	1		02	50	----	PP/NP	0

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course. **L** –Lecture, **T** – Tutorial, **P**- Practical/ Drawing, **S** – Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD** Teaching Department, **PSB:** Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and 21KBK37/47 **Balake Kannada** is for non-Kannada speaking, reading, and writing students

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

Internship of 04 weeks during the intervening period of IV and V semesters; 21INT68Innovation/ Entrepreneurship/ Societal based Internship.

(1) All the students shall have to undergo a mandatory internship of 04 weeks during the intervening period of IV and V semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the VI semester grade card.The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be considered under F (fail) grade and shall have to complete during subsequently after satisfying the internship requirements.

(2) Innovation/ Entrepreneurship Internship shall be carried out at industry, State and Central Government /Non-government organizations (NGOs), micro, small and medium enterprise (MSME), Innovation centres or Incubation centres. Innovation need not be a single major breakthrough; it can also be a series of small or incremental changes. Innovation of any kind can also happen outside of the business world. Entrepreneurship internships offers a chance to gain hands on experience in the world of entrepreneurship and helps to learn what it takes to run a

small entrepreneurial business by performing intern duties with an established company. This experience can then be applied to future business endeavours. Start-ups and small companies are a preferred place to learn the business tack ticks for future entrepreneurs as learning how a small business operates will serve the intern well when he/she manages his/her own company. Entrepreneurship acts as a catalyst to open the minds to creativity and innovation. Entrepreneurship internship can be from several sectors, including technology, small and medium-sized, and the service sector.

(3) Societal or social internship. Urbanization is increasing on a global scale; and yet, half the world's population still resides in rural areas and is devoid of many things that urban population enjoy. Rural internship is a work-based activity in which students will have a chance to solve/reduce the problems of the rural place for better living. As proposed under the AICTE rural internship programme, activities under Societal or social internship, particularly in rural areas, shall be considered for 40 points under AICTE activity point programme.

Ability Enhancement Course - IV

21ECT4091	Embedded C Basics	**21ECT4093**	Octave / Scilab for signals
21ECT4092	C++ Basics	**21ECT4094**	DAQ using LabVIEW

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B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

V Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	PCC	21ECT501	Digital Communication	ECE	3	0	0			3	50	50	100	3
2	IPCC	21ECT502	Object Oriented Programming with Java & Data Structures	ECE	3	0	2		3	3	50	50	100	4
3	PCC	21ECT503	Computer Communication Networks	ECE	3	0	0		3	3	50	50	100	3
4	PCC	21ECT504	Microwave Theory & Antennas	ECE	3	0	0		3	3	50	50	100	3
5	PCC	21ECL505	Communication Lab II	ECE	0	0	2		3	3	50	50	100	1
6	AEC	21ECT506	Research Methodology & Intellectual Property Rights	Any Department	2	0	0		2	2	50	50	100	2
7	HSSC	21CV507	Environmental Studies	Civil/Chemistry	1	0	0			1	50	50	100	1
8	AEC	21ECT508	Ability Enhancement Course-V	ECE						1/2	50	50	100	1
9	HSSC	21HSN509	Aptitude and Verbal ability skills		1	0	1	0		2	50	--	PP/NP	0
										Total	450	400	800	18

Ability Enhancement Course - V

21ECT5081	IoT Lab	**21ECT5083**	Antenna Design & Testing
21ECT5082	Communication Simulink Toolbox	**21ECT5084**	Microwaves toolbox

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B.E. Electronics & Communication Engineering

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VI Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	HSSC	21ECT601	Technological Innovation Management and Entrepreneurship								50	50	100	03
2	IPPC	21ECT602	Computer Organization & ARM Microcontrollers	ECE	2	2			4	3	50	50	100	04
3	PCC	21ECT603	VLSI Design & Testing	ECE	3				3	3	50	50	100	03
4	PEC	21ECE604X	Professional Elective -I	ECE	3				3	3	50	50	100	03
5	OEC	21ECE605X	OpenElective-I	ECE	3				3	3	50	50	100	03
6	PCC	21ECL606	VLSI Laboratory	ECE			2		2		50	50	100	01
7	MP	21ECM607	Mini Project	ECE			2		2		50	50	100	03
8	INT	21ECI608	Innovation/Entrepreneurship /Societal Internship								50	50	100	03
9	HSSC	21HSN609	Analytical & Reasoning skills	Placement Cells	2	0	0-		02	--	50	--	PP/NP	00
								Total			500	450	900	22

Research/Industrial Internship - At the End of the sixth / Seventh semester (in two cycles to accommodate all the students of the University) Research/Industrial Internship shall be carried out – Based on industrial/Govt./NGO/MSME/Rural Internship/Innovation/Entrepreneurship. All the students admitted shall have to undergo a mandatory internship of 24 weeks during the vacation of VI/VII semesters. A University Viva-Voce examination shall be conducted during VII/VIII semester and the prescribed credit shall be included in VII/VIII semester. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements. Research internship Students have to take up research internships at Centers of Excellence (CoE) / Study Centers established in the same institute and /or out of the institute at reputed

research organizations / Institutes. A research internship is intended to give you the flavour of current research going on on a particular topic/s. The internships serve this purpose. They help students get familiarized with the field, the skill needed the effort amount and kind of effort required for carrying out research in that field.

Industry internships: This is an extended period of work experience undertaken by university/Institute students looking to supplement their degree with professional development. The students are allowed to prepare themselves for the workplace and develop practical skills as well as academic ones. It also helps them learn to overcome unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with "unexpected contingencies" helps students recognize, appreciate, and adapt to organization realities by tempering knowledge with practical constraints.

Mini-project work: Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini-project can be assigned to an individual student or a group having not more than 4 students. (or Mini Project is a laboratory-oriented course which will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications) CIE procedure for
Mini-project: (i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide. The CIE marks awarded for the Mini-project work, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the college. The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates. SEE for Mini-project: (i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester-end examination (SEE) conducted at the department. (ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester-end examination (SEE) conducted separately at the departments to which the student/s belongs
Open Elective Courses: Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives). Selection of an open elective shall not be allowed if, • The candidate has studied the same course during the previous semesters of the program. • The syllabus content of open electives is similar to that of the Departmental core courses or professional electives. • A similar course, under any category, is prescribed in the higher semesters of the program. • Registration to electives shall be documented under the guidance of the Programme Coordinator/ Advisor/Mentor

Professional Elective Courses-I		**Open Elective Courses-I**	
Subject Code	**Title**	**Subject Code**	**Title**
21ECE6041	Artificial Neural Networks (L:T:P :: 2:2:0)	**21ECE6051**	Communication Engineering (L:T:P :: 3:0:0)
21ECE6042	Cryptography (L:T:P :: 2:2:0)	**21ECE6052**	Microcontrollers (L:T:P :: 3:0:0)
21ECE6043	Python Programming (L:T:P :: 2:0:2)	**21ECE6053**	Basic VLSI Design (L:T:P :: 3:0:0)
21ECE6044	Micro Electro Mechanical Systems (L:T:P :: 3:0:0)	**21ECE6054**	Electronic Circuits with Verilog (L:T:P :: 2:0:2)
		21ECE6055	Sensors & Actuators (L:T:P :: 3:0:0)

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B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

VII Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	PCC	21ECE701	Advanced VLSI	ECE	3	0	0		3	3	50	50	100	3
2	PCC	21ECE702	Optical & Wireless Communication	ECE	2	0	0		3	3	50	50	100	2
3	PEC	21ECE703X	Professional elective Course-II	ECE	3	0	0		3	3	50	50	100	3
4	PEC	21ECE704X	Professional elective Course-III	ECE	3	0	0		3	3	50	50	100	3
5	OEC	21ECE705X	Open elective Course-II		3	0	0		3	3	50		100	3
6	Project	21ECP706	Project work	ECE						3	100	50	200	10
								Total			350	450	700	24

Professional Elective Courses-II		Professional Elective Courses-III		Open Elective Courses-II	
Subject Code	Title	Subject Code	Title	Subject Code	Title
21ECE7031	Advanced Design Tools for VLSI (L:T:P :: 2:0:2)	21ECE7041	IoT & Wireless Sensor Networks (L:T:P :: 3:0:0)	21ECE7051	Optical & Satellite Communication (L:T:P :: 3:0:0)
21ECE7032	Digital Image Processing (L:T:P :: 2:0:2)	21ECE7042	Network Security (L:T:P :: 3:0:0)	21ECE7052	ARM Embedded Systems (L:T:P :: 3:0:0)
21ECE7033	DSP Algorithms & Architecture (L:T:P :: 3:0:0)	21ECE7043	Fabrication technology (L:T:P :: 3:0:0)	21ECE7053	Basic Digital Image Processing (L:T:P :: 2:0:2)
21ECE7034	Biomedical Signal Processing (L:T:P :: 3:0:0)	21ECE7044	Machine Learning with Python (L:T:P :: 2:0:2)	21ECE7054	Basic Digital Signal Processing (L:T:P :: 2:0:2)
21ECE7035	Speech Signal Processing (L:T:P :: 3:0:0)	21ECE7045	Multimedia Communication (L:T:P :: 2:0:2)	21ECE7055	E-waste Management (L:T:P :: 3:0:0)

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B.E. Electronics & Communication Engineering

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VIII Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week				Examination				Credits
					L	T	P	S	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	Seminar	21ECS801	Technical Seminar		One contact hour /week for interaction between the faculty and students				--	100	---	100	01
2	Research Internship/ Industry Internship	21ECI802	Research/Industry Internship*		Two contact hours /week for interaction between the faculty and students.				3 (Batch wise)	100	100	200	15
3	NCMC	21EC803	National Service Scheme (NSS)	NSS	Completed during the intervening period of III semester to VIII semester.				--	50	50	100	--
		21EC803	Physical Education (PE) (Sports & Athletics)	PE									
		21EC803	Yoga	Yoga									
									Total	250	150	400	16

Note: (1) University /Institutions may swap 7th and 8th Semester Course work to accommodate industry/research internship at the end of sixth semester /at the end of seventh semester to balance the workload. (2) Credits earned for the course prescribed will be accounted in 8th semester

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2020 Batch)

I Semester (Physics Group)

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Board Paper Setting	Teaching Hours / Week			Examination				Credits
						Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	BC	18MA11	Calculus and Linear Algebra	MAT	Science	03	02	--	03	050	050	100	04
2	BC	18PH12	Engineering Physics	PHY	Science	03	02	--	03	050	050	100	04
3	ES	18EE13	Basic Electrical Engineering	EE	EE	02	02	--	03	050	050	100	03
4	ES	18CV14	Civil Engineering and Mechanics	EC/EI/TC	CIV	02	02	--	03	050	050	100	03
5	ES	18MEL15	Engineering Graphics and Design	ME,IEM	ME	02	--	02	03	050	050	100	03
6	BC	18PHL16	Engineering Physics Laboratory	PHY	Science	--	--	02	03	050	050	100	01
7	ES	18EEL17	Basic Electrical Engineering Laboratory	EE	EE	--	--	02	03	050	050	100	01
8	HS	18HS11/ 18HS12	English/Kannada	HS	HS	01	--	02	02	050	050	100	01
			Total			**13**	**08**	**08**	**23**	**400**	**400**	**800**	**20**

Note: BC: Basic Course, ES: Engineering Science. HS: Humanities, EE: Electrical & Electronics Engineering, ME: Mechanical Engineering, CS: Computer Science and Engineering, PHY: Physics, CIV: Civil Engineering

BOS Chairman Dean(Academics) Principal

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2020 Batch)

II Semester(Chemistry Cycle)

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Board Paper Setting	Teaching Hours / Week			Examination				Credits
						Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	BC	18MA21	Differential Equations & Complex Variables	MAT	Science	03	02	--	03	050	050	100	04
2	BC	18CH22	Engineering Chemistry	CHE	Science	03	02	--	03	050	050	100	04
3	ES	18CS23	Programming for Problem Solving	CS	CS	02	02	--	03	050	050	100	03
4	ES	18EC24	Basic Electronics	EC/EI/TC	ECE	02	02	--	03	050	050	100	03
5	ES	18ME25	Elements of Mechanical Engineering	ME,IEM	ME	02	02	--	03	050	050	100	03
6	BC	18CHL26	Engineering Chemistry Laboratory	CHE	Science	--	--	02	03	050	050	100	01
7	ES	18CSL27	Computer Programming Laboratory	CS	CS	--	--	02	03	050	050	100	01
8	HS	18HS21/ 18HS22	English/Kannada	HS	HS	01	--	02	02	050	050	100	01
			Total			**13**	**10**	**06**	**23**	**400**	**400**	**800**	**20**

Note: BC: Basic Course, ES: Engineering Science. HS: Humanities, ECE: Electronics and Communication Engineering, EI: Electronics and Instrumentation, TC: Telecommunication Engineering, ME: Mechanical Engineering, CS: Computer Science and Engineering, CHE: Chemistry, MAT: Mathematics

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2020 Batch)

III Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing/ Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	BC	18MA31	Transforms & Applications	MAT	02	02	--	04	050	050	100	03
2	PC	18EC31	Electronics devices	EC	03	--	--	04	050	050	100	03
3	PC	18EC32	Digital Electronics	EC	04	--	--	04	050	050	100	04
4	PC	18EC33	Network Theory	EC	04	--	--	04	050	050	100	04
5	PC	18EC34	Signals and Systems	EC	03	02	--	05	050	050	100	04
6	PC	18EC35	Power Electronics & Instrumentation	EC	03	--	--	03	050	050	100	03
7	PC	18ECL36	Electronic Devices & Instrumentation Laboratory	EC	--	--	02	02	050	050	100	01
8	PC	18ECL37	Digital Electronics Laboratory	EC	--	--	02	02	050	050	100	01
9	HS	18HS31/32	Constitution of India Professional Ethics and Cyber law /Environmental Studies	HS	01	--	--	02	050	050	100	01
10	MC	18HS33	Soft skills (MC)	HS	04	--	--	03	050	---	050	00
Total					**25**	**02**	**04**	**31**	**500**	**450**	**950**	**24**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

11.	MC	18MAD41	Advance Mathematics - I	MAT	02	02	--	03	50	--	--	00

a.) The mandatory non – credit courses Advance Mathematics I and II prescribed at III and IV semesters respectively, to lateral entry Diploma holders admitted to III semester of BE programs shall compulsorily be registered during respective semesters to complete all the formalities of the course and appear for SEE examination.

b.) The mandatory non – credit courses Basic Engineering Mathematics I and II, prescribed to lateral entrant Diploma holders admitted to III and IV semester of BE programs, are to be completed to secure eligibility to VII semester. However, they are not considered for vertical progression from II year to III year of the programme but considered as head of passing along with credit courses of the programme to eligibility to VII semester.

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SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2020 Batch)

IV Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1.	BC	18MA41	Probability, Numerical and Optimization Technique	MAT	02	02	--	04	050	050	100	03
2.	PC	18EC41	Analog Circuits	EC	03	--	--	04	050	050	100	03
3.	PC	18EC42	Principles of Communication Systems	EC	04	--	--	03	050	050	100	04
4.	PC	18EC43	Electromagnetic Waves	EC	03	--	--	04	050	050	100	03
5.	PC	18EC44	Verilog HDL	EC	04	--	--	04	050	050	100	04
6.	PC	18EC45	Control Systems	EC	04	--	--	04	050	050	100	04
7.	PC	18ECL46	Analog Circuits and Communication Laboratory	EC	--	--	02	02	050	050	100	01
8.	PC	18ECL47	HDL Lab	EC	--	--	02	02	050	050	100	01
9.	CIV	18HS41/42	Constitution of India Professional Ethics and Cyber law/ Environmental Studies	HS/CIV	01	--	--	01	050	050	100	01
10.	MC	18HS43	Soft skills (NCMC)	HS	04	--	--	04	050	--	050	00
			Total		**26**	**02**	**04**	**32**	**500**	**450**	**950**	**24**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

11.	MC	19MAD41	Advance Mathematics – II	MAT	02	02	--	03	50	--	--	00

a.) The mandatory non – credit courses Advance Mathematics I and II prescribed at III and IV semesters respectively, to lateral entry Diploma holders admitted to III semester of BE programs shall compulsorily be registered during respective semesters to complete all the formalities of the course and appear for SEE examination.

b.) The mandatory non – credit courses Basic Engineering Mathematics I and II, prescribed to lateral entrant Diploma holders admitted to III and IV semester of BE programs, are to be completed to secure eligibility to VII semester. However, they are not considered for vertical progression from II year to III year of the programme but considered as head of passing along with credit courses of the programme to eligibility to VII semester.

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2020 Batch)

V Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	PC	18HS51	IPR	HS	03	--	--	03	050	050	100	03
2	PC	18EC51	Microprocessor and Microcontrollers	EC	04	--	--	04	050	050	100	03
3	PC	18EC52	Digital Signal Processing	EC	04	--	--	04	050	050	100	04
4	PC	18EC53	Digital Communication	EC	04	--	--	04	050	050	100	04
5	PC	18EC54	Object Oriented Programming with C++	EC	03	--	--	04	050	050	100	03
6	PE	18EC55X	Professional Elective-1	EC	03	--	--	03	050	050	100	03
7	OE	18EC56X	Open Elective A		03	--	--	03	050	050	100	03
8	PC	18ECL57	Microcontroller Laboratory	EC	--	--	02	02	050	050	100	01
9	PC	18ECL58	Digital Signal Processing Laboratory	EC	--	--	02	02	050	050	100	01
				Total	**24**	**00**	**04**	**29**	**450**	**400**	**900**	**25**

18EC55x_Professional Elective – 1		
Sl. No.	**Course Code**	**Course Title**
1	18EC551	Digital Switching System
2	18EC552	Python Programming
3	18EC553	Artificial Neural Networks
4	18EC554	Nanoelectronics
5	18EC555	Computer Organization and Architecture

Open Elective-A(OE-A)		
Sl. No.	**Course Code**	**Course Title**
1	18EC561	Real Time Operating System(CS,IS, EI, ML)
2	18EC562	Mechatronics (CS,IS, EI, ML, ME, IEM, EEE)
3	18EC563	Television Engineering (TE, EI, ML)
4	18EC564	Sensors (CS, IS, ML, TC)

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SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2020 Batch)

VI Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing/ Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	PC	18HS61	Management and Entrepreneurship	EC	03	--	--	03	050	050	100	03
2	PC	18EC61	CMOS VLSI Design	EC	04	--	--	04	050	050	100	04
3	PC	18EC62	Embedded Systems	EC	03	--	--	03	050	050	100	03
4	PC	18EC63	Computer Communication Network	EC	04	--	--	04	050	050	100	04
5	PC	18EC64x	Professional Elective – 2	EC	03	--	--	03	050	050	100	03
6	OE	18EC65x	Open Elective –B	EC	03	--	--	03	050	050	100	03
7	PC	18ECL66	Embedded System Laboratory	EC	--	--	02	02	050	050	100	01
8	PC	18ECL67	VLSI Laboratory	EC	--	--	02	02	050	050	100	01
9	M	18ECM68	Mini Project					03	050	050	100	02
10	INT	18ECI69	Industry Internship	To be carried out during the intervening vacations of VI an VII semesters				--	--	--	--	--
			Total		**20**	**00**	**04**	**27**	**450**	**450**	**900**	**24**

18EC65x_Professional Elective – 2 (PECEL 2)		
Sl. No.	**Course Code**	**Course Title**
1	18EC641	Semiconductor Fabrication
2	18EC642	Cryptography
3	18EC643	Information Theory & Coding
4	18EC644	System Verilog for verification
5	18EC645	Internet of Things
6	18EC646	Autotronics and Vehicle Intelligence

Open Elective-B(OE-B)		
Sl. No.	**Course Code**	**Course Title**
1	18EC651	Automotive Electronics Engineering (CS, IS, EI, ET, ML, ME, IEM, EEE)
2	18EC652	Nano Electronics (CS,IS,ML,TC, ME)
3	18EC653	Wireless Sensor Networks(EE,ML,EI)
4	18EC654	Robotics and Machine vision systems(ME,EI,EE,ML,IEM)

BOS Chairman Dean(Academics) Principal

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SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2020 Batch)

VII Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	MC	18HS71	Cost Management of Engg Projects	HS	02	--	--	02	050	050	100	02
2	PC	18EC71	Wireless Communication	EC	04	--	--	04	050	050	100	04
3	PC	18EC72	Microwave and Antenna	EC	03	--	--	03	050	050	100	04
4	PE	18EC73X	Professional Elective-3	EC	03	--	--	03	050	050	100	03
5	PE	18EC74X	Professional Elective-4	EC	03	--	--	03	050	050	100	03
6	OE	18EC75X	Open Elective-C	EC	03	--	--	03	050	050	100	03
7	PC	18ECL76	Advance Communication Lab	EC	--	--	02	02	050	050	100	01
8	PC	18ECL77	CCN Lab	EC	--	--	02	02	050	050	100	01
9	Project	18ECP78	Project work phase-1	EC	--	--	02	02	050	050	100	02
10	INT	18ECI79	Internship	--	--	--	--	---	---	---	--	--
			Total		**18**	**--**	**06**	**24**	**400**	**400**	**800**	**23**

Internship: All the students admitted to III year of BE have to undergo mandatory internship of 4 weeks during the vacations of VI and VII semesters and /or VII and VIII semesters. A University examination will be conducted during VIII semester and prescribed credit are added to VIII semester. Internship is considered as a head of passing and is considered for the award of degree. Those, who do not take-up/complete the internship will be declared as failed and have to complete during subsequent University examination after satisfy the internship requirements

Note: : PC: Professional Core. PE: Professional Elective, OE: Open Elective. MC: Mandatory Course, PRJ: Project work, INT: Internship

Select **ANY ONE** of the Professional Elective. Open Elective-A: Students can select any one of the open electives (Please refer to consolidated list of Dr AIT for open electives) offered by any Department

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2020 Batch)

Professional Elective-3(PE-3)		
Sl. No.	**Course Code**	**Course Title**
1	18EC731	5G Technology
2	18EC732	Speech and Audio Processing
3	18EC733	Real Time Operating systems
4	18EC734	DSP Algorithm and architecture
5	18EC735	Network Security

Professional Elective-4(PE-4)		
Sl. No.	**Course Code**	**Course Title**
1	18EC741	Analog and Mixed Mode VLSI
2	18EC742	Operating systems
3	18EC743	Satellite Communication
4	18EC744	ASIC Design
5	18EC745	Operational Research

Open Elective-B(OE-B)		
Sl. No	**Course Code**	**Course Title**
1	18EC751	Internet of Things (CS,IS,EI,ML)
2	18EC752	Cryptography and Network Security(CS,IS,ML,TC)
3	18EC753	Mobile Communication(EI,EE,ML)
4	18EC754	High Speed Electronics(EE,EI,ML,TC)

BOS Chairman Dean(Academics) Principal

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SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2020 Batch)

VIII Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
2	MC	18CV81	Occupational and Safety and Health administration	CV	02	--	--	03	050	050	100	02
4	Project	18ECP81	Project Work Phase-2	EC	--	--	02	03	050	050	100	10
5	Seminar	18ECS82	Technical Seminar	EC	--	--	02	03	050	050	100	01
	INT	18ECI83	Industry Internship	EC	--	--	--	03	050	050	100	02
			Total		**05**	**--**	**04**	**15**	**250**	**250**	**500**	**15**

Internship: Those, who have not pursued /completed the internship will be declared as failed and have to complete during subsequent SEE examination after they satisfy the internship requirements.

Note: : PC: Professional Core. PE: Professional Elective, OE: Open Elective. MC: Mandatory Course, PRJ: Project work, INT: Internship

Select **ANY ONE** of the Professional Elective and Open Elective subject

Students can select any one of the open electives (Please refer to consolidated list of Dr. AIT open electives) offered by any Department.
Selection of an open elective is not allowed provided,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of Departmental core courses or professional electives. Registration to electives shall be documented under the guidance of Programme Coordinator/ Mentor.

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SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

I Semester (Physics Group)

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Board Paper Setting	Teaching Hours / Week			Examination				Credits
						Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	BC	18MA11	Differential Equations & Complex Variables	MAT	Science	03	02	--	03	050	050	100	04
2	BC	18PH12	Engineering Physics	PHY	Science	03	02	--	03	050	050	100	04
3	ES	18EE13	Basic Electrical Engineering	EE	EE	02	02	--	03	050	050	100	03
4	ES	18CV14	Civil Engineering and Mechanics	EC/EI/TC	CIV	02	02	--	03	050	050	100	03
5	ES	18MEL15	Engineering Graphics and Design	ME,IEM	ME	02	--	02	03	050	050	100	03
6	BC	18PHL16	Engineering Physics Laboratory	PHY	Science	--	--	02	03	050	050	100	01
7	ES	18EEL17	Basic Electrical Engineering Laboratory	EE	EE	--	--	02	03	050	050	100	01
8	HS	18HS11/ 18HS12	English/Kannada	HS	HS	01	--	02	02	050	050	100	01
			Total			**13**	**08**	**08**	**23**	**400**	**400**	**800**	**20**

Note: BC: Basic Course, ES: Engineering Science. HS: Humanities, EE: Electrical & Electronics Engineering, ME: Mechanical Engineering, CS: Computer Science and Engineering, PHY: Physics, CIV: Civil Engineering

BOS Chairman Dean(Academics) Principal

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

II Semester(Chemistry Cycle)

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Board Paper Setting	Teaching Hours / Week			Examination				Credits
						Theory Lecture (L)	Tutorial (T)	Drawing/ Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	BC	18MA21	Calculus and Linear Algebra	MAT	Science	03	02	--	03	050	050	100	04
2	BC	18CH22	Engineering Chemistry	CHE	Science	03	02	--	03	050	050	100	04
3	ES	18CS23	Programming for Problem Solving	CS	CS	02	02	--	03	050	050	100	03
4	ES	18EC24	Basic Electronics	EC/EI/TC	ECE	02	02	--	03	050	050	100	03
5	ES	18ME25	Elements of Mechanical Engineering	ME,IEM	ME	02	02	--	03	050	050	100	03
6	BC	18CHL26	Engineering Chemistry Laboratory	CHE	Science	--	--	02	03	050	050	100	01
7	ES	18CSL27	Computer Programming Laboratory	CS	CS	--	--	02	03	050	050	100	01
8	HS	18HS21/ 18HS22	English/Kannada	HS	HS	01	--	02	02	050	050	100	01
			Total			**13**	**10**	**06**	**23**	**400**	**400**	**800**	**20**

Note: BC: Basic Course, ES: Engineering Science. HS: Humanities, ECE: Electronics and Communication Engineering, EI: Electronics and Instrumentation, TC: Telecommunication Engineering, ME: Mechanical Engineering, CS: Computer Science and Engineering, CHE: Chemistry, MAT: Mathematics

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SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

III Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing/ Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	BC	18MA31	Transforms & Applications	MAT	02	02	--	03	050	050	100	03
2	PC	18EC31	Electronics devices	EC	04	--	--	03	050	050	100	04
3	PC	18EC32	Digital System Design	EC	04	--	--	03	050	050	100	04
4	PC	18EC33	Network Theory	EC	04	--	--	03	050	050	100	04
5	PC	18EC34	Engineering Statistics	EC	03	--	--	03	050	050	100	03
6	PC	18EC35	Power Electronics & Instrumentation	EC	03	--	--	03	050	050	100	03
7	PC	18ECL36	Electronic Devices & Instrumentation Laboratory	EC	--	--	02	03	050	050	100	01
8	PC	18ECL37	Digital System Design Laboratory	EC	--	--	02	03	050	050	100	01
9	HS	18HS31/32	Constitution of India Professional Ethics and Cyber law /Environmental Studies	HS	01	--	--	02	050	050	100	01
10	MC	18HS33	Soft skills (MC)	HS	04	--	--	03	050	---	050	00
Total					**25**	**02**	**04**	**29**	**500**	**450**	**950**	**24**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

11.	MC	18MAD41	Advance Mathematics - I	MAT	02	02	--	03	50	--	--	00

a.) The mandatory non – credit courses Advance Mathematics I and II prescribed at III and IV semesters respectively, to lateral entry Diploma holders admitted to III semester of BE programs shall compulsorily be registered during respective semesters to complete all the formalities of the course and appear for SEE examination.

b.) The mandatory non – credit courses Basic Engineering Mathematics I and II, prescribed to lateral entrant Diploma holders admitted to III and IV semester of BE programs, are to be completed to secure eligibility to VII semester. However, they are not considered for vertical progression from II year to III year of the programme but considered as head of passing along with credit courses of the programme to eligibility to VII semester.

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SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

IV Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1.	BC	18MA41	Probability, Numerical and Optimization Technique	MAT	02	02	--	03	050	050	100	03
2.	PC	18EC41	Analog Circuits	EC	04	--	--	03	050	050	100	04
3.	PC	18EC42	Principles of Communication Systems	EC	03	--	--	03	050	050	100	03
4.	PC	18EC43	Computer Organization and Architecture	EC	04	--	--	03	050	050	100	03
5.	PC	18EC44	Verilog HDL	EC	04	--	--	03	050	050	100	04
6.	PC	18EC45	Signals and Systems	EC	04	--	--	03	050	050	100	04
7.	PC	18ECL46	Analog Circuits and Communication Laboratory	EC	--	--	02	02	050	050	100	01
8.	PC	18ECL47	HDL Lab	EC	--	--	02	02	050	050	100	01
9.	CIV	18HS41/ 42	Constitution of India Professional Ethics and Cyber law/ Environmental Studies	HS/CIV	01	--	--	02	050	050	100	01
10.	MC	18HS43	Soft skills (NCMC)	HS	04	--	--	03	050	--	050	00
				Total	**26**	**02**	**04**	**27**	**500**	**450**	**950**	**24**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

11.	MC	18MAD41	Advance Mathematics - II	MAT	02	02	--	03	50	--	--	00

a.) The mandatory non – credit courses Advance Mathematics I and II prescribed at III and IV semesters respectively, to lateral entry Diploma holders admitted to III semester of BE programs shall compulsorily be registered during respective semesters to complete all the formalities of the course and appear for SEE examination.

b.) The mandatory non – credit courses Basic Engineering Mathematics I and II, prescribed to lateral entrant Diploma holders admitted to III and IV semester of BE programs, are to be completed to secure eligibility to VII semester. However, they are not considered for vertical progression from II year to III year of the programme but considered as head of passing along with credit courses of the programme to eligibility to VII semester.

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

V Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week				Examination			Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	PC	18HS51	IPR	HS	03	--	--	03	050	050	100	03
2	PC	18EC51	Electromagnetic Waves	EC	04	--	--	04	050	050	100	03
3	PC	18EC52	Digital Signal Processing	EC	04	--	--	04	050	050	100	04
4	PC	18EC53	Digital Communication	EC	04	--	--	04	050	050	100	04
5	PC	18EC54	Microprocessor and Microcontroller	EC	03	--	--	04	050	050	100	03
6	PE	18EC55X	Professional Elective-1	EC	03	--	--	03	050	050	100	03
7	OE	18EC56X	Open-Elective A		03	--	--	03	050	050	100	03
8	PC	18ECL57	Microcontroller Laboratory	EC	--	--	02	02	050	050	100	01
9	PC	18ECL58	Digital Signal Processing Laboratory	EC	--	--	02	02	050	050	900	01
				Total	**24**	**00**	**04**	**29**	**400**	**450**	**800**	**25**

18EC55x_Professional Elective – 1		
Sl. No.	**Course Code**	**Course Title**
1	18EC551	Digital Switching System
2	18EC552	Programming with Python
3	18EC553	Artificial Neural Networks
4	18EC554	Object Oriented Programming with C++
5	18EC555	Control Systems

Open Elective-A(OE-A)		
Sl. No.	**Course Code**	**Course Title**
1	18EC561	Real Time Operating System(CS,IS, EI, ML)
2	18EC562	Mechatronics (CS,IS, EI, ML, ME, IEM, EEE)
3	18EC563	Television Engineering (TE, EI, ML)
4	18EC564	Sensors (CS, IS, ML, TC)

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

VI Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing/ Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	PC	18HS61	Management and Entrepreneurship	EC	03	--	--	03	050	050	100	03
2	PC	18EC61	CMOS VLSI Design	EC	04	--	--	03	050	050	100	04
3	PC	18EC62	Embedded Systems	EC	03	--	--	03	050	050	100	03
4	PC	18EC63	Computer Communication Network	EC	04	--	--	03	050	050	100	04
5	PC	18EC64x	Professional Elective – 2	EC	03	--	--	03	050	050	100	03
6	OE	18EC65x	Open Elective –B	EC	03	--	--	03	050	050	100	03
7	PC	18ECL66	Embedded Systems Laboratory	EC	--	--	02	02	050	050	100	01
8	PC	18ECL67	VLSI Laboratory	EC	--	--	02	02	050	050	100	01
9	M	18ECM68	Mini Project					03	050	050	100	02
10	INT	18ECI69	Industry Internship	To be carried out during the intervening vacations of VI an VII semesters				--	--	--	--	--
				Total	**20**	**00**	**04**	**27**	**450**	**450**	**900**	**24**

18EC65x_Professional Elective – 2 (PECEL 2)		
Sl. No.	**Course Code**	**Course Title**
1	18EC641	Semiconductor Fabrication
2	18EC642	Cryptography
3	18EC643	Information Theory & Coding
4	18EC644	System Verilog for verification
5	18EC645	Internet of Things

Open Elective-B(OE-B)		
Sl. No.	**Course Code**	**Course Title**
1	18EC651	Automotive Safety Measurements(ME,IEM,EE)
2	18EC652	Nano Electronics (CS,IS,ML,TC)
3	18EC653	Wireless Sensor Networks(EE,ML,EI)
4	18EC654	Robotics and Machine vision systems(ME,EI,EE,ML)

BOS Chairman Dean(Academics) Principal

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

VII Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	MC	18HS71	Cost Management of Engg Projects	HS	03	--	--	03	050	050	100	02
2	PC	18EC71	Wireless Communication	EC	04	--	--	03	050	050	100	04
3	PC	18EC72	Microwave and Antenna	EC	04	--	--	03	050	050	100	04
4	PE	18EC73X	Professional Elective-3	EC	03	--	--	03	050	050	100	03
5	PE	18EC74X	Professional Elective-4	EC	03	--	--	03	050	050	100	03
6	OE	18EC75X	Open Elective-C	EC	03	--	--	03	050	050	100	03
7	PC	18ECL76	Advance Communication Lab	EC	--	--	02	02	050	050	100	01
8	PC	18ECL77	Computer Communication Network Lab	EC	--	--	02	02	050	050	100	01
9	Project	18ECP78	Project work phase-1	EC	--	--	02	02	050	050	100	02
10	INT	18ECI79	Internship	--	--	--	--	---	---	---	--	--
			Total		**20**	**--**	**06**	**24**	**400**	**400**	**800**	**23**

Internship: All the students admitted to III year of BE have to undergo mandatory internship of 4 weeks during the vacations of VI and VII semesters and /or VII and VIII semesters. A University examination will be conducted during VIII semester and prescribed credit are added to VIII semester. Internship is considered as a head of passing and is considered for the award of degree. Those, who do not take-up/complete the internship will be declared as failed and have to complete during subsequent University examination after satisfy the internship requirements

Note: : PC: Professional Core. PE: Professional Elective, OE: Open Elective. MC: Mandatory Course, PRJ: Project work, INT: Internship

Select **ANY ONE** of the Professional Elective. Open Elective-A: Students can select any one of the open electives (Please refer to consolidated list of Dr AIT for open electives) offered by any Department

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

Professional Elective-3(PE-3)		
Sl. No.	**Course Code**	**Course Title**
1	18EC731	5G Technology
2	18EC732	Virtual Reality
3	18EC733	Real Time Operating systems
4	18EC734	DSP Algorithm and architecture
5	18EC735	Network and Cyber Security
6	18EC736	Optical Fibre Communication

Professional Elective-4(PE-4)		
Sl. No.	**Course Code**	**Course Title**
1	18EC741	Analog and Mixed Mode VLSI
2	18EC742	Operating systems
3	18EC743	Satellite Communication
4	18EC744	Real Time Embedded Systems
5	18EC745	Operations Research
6	18EC746	Adaptive Signal Processing

Open Elective-C (OE-C)		
Sl. No	**Course Code**	**Course Title**
1	18EC751	Internet of Things (CS, IS, EI, TE, ML, ME, IEM, EEE, CV)
2	18EC752	Cryptography (CS, IS, ML,TE, EI,EEE)
3	18EC753	Mobile Communication (EI, EE, ML)
4	18EC754	Bio Mechatronics (CS, IS, EI, TE, ML, ME, IEM, EEE, CV)
5	18EC755	Introduction to Unmanned Aerial Vehicle (UAV) (CS,IS, EI, TE,ML, ME, IEM, EEE,CV)

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

VIII Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing/ Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	MC	18HS81	Occupational and Safety and Health administration	CV	03	--	--	03	050	050	100	02
2	Project	18ECP81	Project Work Phase-2	EC	--	--	03	03	050	050	100	10
3	Seminar	18ECS82	Technical Seminar	EC	--	--	03	03	050	050	100	01
4	INT	18ECI83	Internship	EC	--	--	03	03	050	050	100	02
Total					**03**	**--**	**09**	**12**	**250**	**250**	**500**	**15**

Internship: Those, who have not pursued /completed the internship will be declared as failed and have to complete during subsequent SEE examination after they satisfy the internship requirements.

Note: : PC: Professional Core. PE: Professional Elective, OE: Open Elective. MC: Mandatory Course, PRJ: Project work, INT: Internship

Select **ANY ONE** of the Professional Elective and Open Elective subject

Students can select any one of the open electives (Please refer to consolidated list of Dr. AIT open electives) offered by any Department.
Selection of an open elective is not allowed provided,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of Departmental core courses or professional electives. Registration to electives shall be documented under the guidance of Programme Coordinator/ Mentor.

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

(Applicable to 2022 batch)

Scheme of Teaching and Examination for I /II Semester B.E., (Common to all B.E. Programmes) Academic Year:2022-23

Physics Cycle : I/II Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hours/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BS	21MAT101	Calculus and Linear Algebra	Mathematics	3	2	0	0	5	3	50	50	100	4
		21MAT201	Advanced Calculus and Numerical methods											
2	BS	21PHT102/ 21PHT202	Engineering Physics	Physics	3	0	0	0	3	3	50	50	100	3
3	ES	21EET103/ 21EET203	Basic Electrical Engineering	Electrical	2	2	0	0	4	3	50	50	100	3
4	ES	21CVT104/ 21CVT204	Elements of Civil Engineering & Mechanics	Civil	3	0	0	0	3	3	50	50	100	3
5	ES	21MED105/ 21MED205	Computer aided Engineering Drawing	Mechanical	2	0	2	0	4	3	50	50	100	3
6	BS	21PHL106/ 21PHL206	Engineering Physics Lab	Physics	0	0	2	0	2	3	50	50	100	1
7	ES	21EEL107/ 21EEL207	Basic Electrical lab	Electrical	0	0	2	0	2	3	50	50	100	1
8	HS	21HST108	Communicative English	Humanities	1	0	1*	0	2	2	50	50	100	1
		21HST208	Professional writing skills in English											
9	AE	21HST109	Health and Wellness	Humanities	1	0	1*	0	2	2	50	50	100	1
		21CVT209	Rural Development	Civil										
10	MC	21HSN110	Career Development skill-I	Humanities	1	0	1*	0	2	--	50	-	PP/NP	0
		21HSN210	Career Development skill-II											
									Total	29		500	450	900	20

Note: BS: Basic Science Course, ES: Engineering Science Course, HS: Humanities & Social Science Course,
AE: Ability Enhancement Course, MC: Mandatory Course, * No practical evaluation,
L: Lecture, T:Titorial, P:Practical/drawing, S:Self study, CIE: Continuous Internal Evaluation, SEE: Semester End Examination

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

Scheme of Teaching and Examination for I /II Semester B.E., (Common to all B.E. Programmes) Academic Year:2022-23

Chemistry Cycle: I/II Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BS	21MAT101	Calculus and Linear Algebra	Mathematics	3	2	0	0	5	3	50	50	100	4
		21MAT201	Advanced Calculus and Numerical methods											
2	BS	21CHT102/ 21CHT202	Engineering Chemistry	Chemistry	3	0	0	0	3	3	50	50	100	3
3	ES	21CST103/ 21CST203	Problem solving through Programming	Computer Science	2	2	0	0	4	3	50	50	100	3
4	ES	21ECT104/ 21ECT204	Basic Electronics and Communication Engineering	Electronics	2	2	0	0	4	3	50	50	100	3
5	ES	21MET105/ 21MET205	Elements of Mechanical Engineering	Mechanical	2	2	0	0	4	3	50	50	100	3
6	BS	21CHL106/ 21CHL206	Engineering Chemistry Laboratory	Chemistry	0	0	2	0	2	3	50	50	100	1
7	ES	21CSL107/ 21CSL207	Computer Programming Laboratory	Computer Science	0	0	2	0	2	3	50	50	100	1
8	HS	21HST108	Communicative English	Humanities	1	0	1*	0	2	2	50	50	100	1
		21HST208	Professional writing skills in English											
9	AE	21CVT109	Rural Development	Civil	1	0	1*	0	2	2	50	50	100	1
		21HST209	Health and Wellness	Humanities										
10	MC	21HSN110	Career Development skill-I	Humanities	1	0	1*	0	2	----	50	--	PP/NP	0
		21HSN210	Career Development skill-II											
								Total	30		500	450	900	20

Note: BS: Basic Science Course, ES: Engineering Science Course, HS: Humanities & Social Science Course, AE: Ability Enhancement Course, MC: Mandatory Course, * No practical evaluation,
L: Lecture, T:Titorial, P:Practical/drawing, S:Self study, CIE: Continuous Internal Evaluation, SEE: Semester End Examination

Note –At the end of the second-semester summer internship shall be carried out – based on inter/intra institutional activities credited in the third semester. University /Institutions may swap few courses between a FIRST and SECOND semester to balance the workload teaching and laboratory schedule

Summer Internship - I: All the students admitted shall have to undergo a mandatory summer internship of 03 weeks during the vacation of II semesters. Summer Internship shall include Inter / Intra Institutional activities. Internship A University Viva-voce examination shall be conducted during III semesters and the prescribed credit shall be included in III semesters. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements

Dr Ambedkar Institute of Technology, Bengaluru-56
Department of Electronics and Communication Engineering
Scheme and Syllabus - CBCS – 2021 -2022

Course Title	**BASIC ELECTRONICS AND COMMUNICATION ENGINEERING**						
Course Code	**21ECT104/204**						
Category	Engineering Science Course (ES)						
Scheme and Credits	No. of Hours/Week					Total teaching hours	Credits
	L	T	P	SS	Total		
	03	00	00	00	03	52	03
CIE Marks: 50	**SEE Marks: 50**		**Total Max. marks=100**		**Duration of SEE: 03 Hours**		

COURSE OBJECTIVES:

1. Preparation: To prepare students with fundamental knowledge/ overview in the field of Electronics and Communication Engineering.
2. Core Competence: To equip students with a basic foundation in electronic engineering fundamentals required for comprehending the operation and application of electronic circuits, logic design, embedded systems and communication systems.
3. Professionalism & Learning Environment: To inculcate in first year engineering students an ethical and a professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context and life- long learning needed for a successful professional career.

UNIT I **11 hours**

Electronic Circuits: Rectifiers, Reservoir and smoothing circuits, Full-wave rectifiers, Bi-phase rectifier circuits, Bridge rectifier circuits, Voltage regulators, Output resistance and voltage regulation, Voltage multipliers, Power Supplies–Block diagram, (No Derivations, Numericals on Rectifiers included).

Amplifiers: Types of amplifiers, Class of operation, Input and output resistance, Frequency response, Bandwidth, Phase shift, Negative feedback.

Operational amplifiers: Operational amplifier parameters, Operational amplifier characteristics, Operational amplifier configurations, Operational amplifier circuits, Multi-stage amplifiers.

Oscillators: Positive feedback, Conditions for oscillation, Ladder network oscillator, Wein bridge oscillator. (No Derivations, Numericals on Op-amp included). **Text 1**

Self-study component: BJT types, comparison of BJT, FET & FinFET.

UNIT II **11 hours**

Logic Circuits: Boolean Algebra, Logic gates, Realization of Boolean Expressions using basic gates and their truth table.

Half Adder and Full Adder, Multiplexer and decoder. Shift registers and its types – operation and truth table, Counters and asynchronous counters. Bistables, R-S Bistables, D-type Bistables, J-K Bistables. **Text 4**

Data representation, Data types, Data storage, A microcontroller system.

Sensors and Interfacing: Instrumentation and control systems, Transducers, Sensors. **Text 1**

Actuators, LED, 7-Segment LED Display, Optocoupler, Stepper Motor, Relay, Piezo Buzzer, Push Button Switch, Keyboard. **Text 2**

Self-study component: Actuator types, LCD, Touch screen displays

UNIT III **10 hours**

Embedded Systems: Definition, Embedded systems vs general computing systems, Classification of Embedded Systems, Major application areas of Embedded Systems, Elements of an Embedded System, Core of the Embedded System, Microprocessor vs Microcontroller, RISC vs CISC, Harvard vs Von-Neumann, Big- Endian vs Little-Endian, Memory, Program storage memory (ROM), RAM, Embedded firmware, other system components. **Text 2**

Communication Interface: UART, Parallel Interface, USB, Bluetooth, Wi-Fi, GPRS. **Text 2**

Self-study component: Block diagrams of the architectures of RISC, CISC, Harvard and Von-Neumann.

UNIT IV **10 hours**

Analog and Digital Communication: Modern communication system scheme, Information source and input transducer, Transmitter, Channel – Hardware and Software, Noise, Receiver, Multiplexing, Types of communication systems. **Text 3**

Types of modulation (only concepts) – AM, FM, Phase Modulation, Pulse Modulation, PAM, PWM, PPM, PCM. Concept of Radio wave propagation. Concepts of Sampling theorem, Nyquist rate, Digital Modulation Schemes– ASK, FSK, PSK

Self-study component: Evolution of Wireless Network Communication Technologies (1G, 2G, 3G and4G, 5G).

UNIT V **10 hours**

Data Transmission: Asynchronous Transmission, Synchronous Communication, Data Compression, Encryption.

Radio Waves, Antennas, Satellite Communication, Microwave Communication, Optical Fiber Communication (OFC): Block diagram of OFC, Advantages of OFC, Applications of OFC. **Text 4**

Cellular Wireless Networks - Introduction, cellular telephone system, cellular concept and frequency reuse. **Text 3**

Self-study component: **Co-ordination number, Atomic packing factor (APF) for simple cubic, body centered and face centered cubic structure. Applications of nanomaterials: Medical and Electronics.**

TEACHING LEARNING PROCESS: Chalk and Talk, power point presentation, animations, videos

COURSE OUTCOMES: On completion of the course, student should be able to:

CO1: Describe the concepts of electronic circuits encompassing power supplies, amplifiers and oscillators.

CO2: Explain the concepts of digital logic circuits, sensors, actuators and I/O subsystems.

CO3: Discuss the characteristics of embedded systems and types of communication interface.

CO4: Describe the fundamental concepts of analog communication, digital communication and radio wave propagation.

CO5: discuss the techniques of data transmission, different modes of communication, wired and wireless communication systems.

TEXT BOOKS

1. Mike Tooley, 'Electronic Circuits, Fundamentals & Applications', 4thEdition, Elsevier, 2015. DOI https://doi.org/10.4324/9781315737980. eBook ISBN9781315737980
2. K V Shibu, 'Introduction to Embedded Systems', 2nd Edition, McGraw Hill Education (India), Private Limited, 2016.
3. S L Kakani and Priyanka Punglia, 'Communication Systems', New Age International Publisher, 2017. https://elib4u.ipublishcentral.com/pdfreader/communication-systems
4. D P Kothari, I J Nagrath, 'Basic Electronics', 2nd edition, McGraw Hill Education (India), Private Limited, 2018.

REFERENCE BOOK

1. **Mitchel E. Schultz, 'Grob's Basic Electronics', 11th Edition, McGraw-Hill, 2011.**

ONLINE RESOURCES

1. https://onlinecourses.nptel.ac.in/noc21_ee55/preview

MODERN TOOLS:

1. PSPICE

MAPPING of COs with POs

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2	1		1			2	1	1		3
CO2	3	2	1					2	1	1		3
CO3	3							2	1	1		3
CO4	3							2	1	1		3
CO5	3							2	1	1		3
Strength of correlation: Low-1, Medium- 2, High-3												

Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY

(An Autonomous Institute affiliated to VTU, Accredited by NAAC with 'A' grade)

BDA Outer Ring Road, Mallathalli,Bengaluru-56

Board Of Studies 2022-23

Proposed Courses for Inter/Intra Department Internship

For

Academic Year (AY) : 2022-23

Submitted by

Department of Electronics and Communication Engineering

To

DEAN (Academic)

For Seeking Approval from the Academic Council

Title of the module 1: MATLAB and its applications

Objectives:

1. Use of MATLAB and Math Works and Toolbox.

2. Create and troubleshoot basic m scripts.

3. Plot datasets.

Out comes: After undergoing three weeks of internship the students will be able to

1. Use of MATLAB Tool

2. Identify the various tools and its application

3. Use tools to engineering applications

***Number Students for enrolment: 60**

Title of the module II: Microcontrollers and its applications

Objectives:

1. Use of Micro Controller

2. Create code and execute basic Programme using 8051 Kit

3.Demonstrate Applications of MC

Out comes: After undergoing three weeks of internship the students will be able to

1. Use of Microcontroller Tool
2. Write assembly language programs.
3. Understand microcontrollers-based systems.

***Number Students for enrolment: 60**

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Scheme of Teaching and Examination effective from the Academic Year 2022-23

III Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BSC	21MAT301	Transform Calculus, Fourier Series and Numerical Techniques	Mathematics	2	2	0	0		03	50	50	100	3
2	IPCC	21ECT302	Digital System Design Using Verilog	ECE	3	0	2			03	50	50	100	4
3	IPCC	21ECT303	Basic Signal Processing	ECE	3	0	2			03	50	50	100	4
4	PCC	21ECT304	Analog Electronic Circuits	ECE	3	0	0	1		03	50	50	100	3
5	PCC	21ECL305	Analog & Digital Electronics Lab	ECE	0	0	2			03	50	50	100	1
6	UHV	21HST306	Social Connect and Responsibility		0	0	1			01	50	50	100	1
7	HSS	21HST307	Samskrutika Kannada		1	0	0			01	50	50	100	1
		21HST307	Balake Kannada											
		OR												
		21HST308	Constitution of India and Professional Ethics											
8	AEC	21ECT309X	Ability Enhancement Course - III							01	50	50	100	1
9	HSSC	21HSN310	Professional Skills		1	0	0	1		02	50	----	PP/NP	0
Total											400	400	800	18
10	Scheduled activities from III to VIII semesters	21HSHS803	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE)(Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester. The activities shall be carried out between III semester to VIII semester (for 5 semesters). SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE and Yoga activities.									
		21HSN803	Physical Education (PE) (Sport and activities)	PE										
		21HSN803	Yoga	Yoga										

Course Prescribed to Lateral Entry Diploma Holders Admitted to III Semester B.E. Program

11		**21MAN311**	**Additional Mathematics-I**	**Maths**	**1**	**0**	**0**	**1**		**02**	**50**	**----**	**PP/NP**	**0**

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course. **L** –Lecture, **T** – Tutorial, **P**- Practical/ Drawing, **S** – Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD** Teaching Department, **PSB:** Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and 21KBK37/47 **Balake Kannada** is for non-Kannada speaking, reading, and writing students

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

21INT49Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internship of 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) Placement Training: These courses are prescribed for I to IV semesters respectively to the students of BE programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case any student fails to register for the said course/fails to secure the minimum 40% of the prescribed CIE marks, he/she shall be deemed to have secured an **NP (not pass)** grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.			
Ability Enhancement Course - III			
21ECT3091	LD Lab using Pspice / MultiSIM	**21ECT3093**	LIC Lab using Pspice / MultiSIM
21ECT3092	AEC Lab using Pspice / MultiSIM	**21ECT3094**	LabVIEW Programming Basics

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Scheme of Teaching and Examination effective from the Academic Year 2022-23

IV Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BSC	21MAT401	Maths for Communication Engineers	Mathematics						03	50	50	100	3
2	IPCC	21ECT402	Digital Signal Processing	ECE	3	0	2			03	50	50	100	4
3	IPCC	21ECT403	Circuit analysis and control systems	ECE	3	0	2			03	50	50	100	4
4	PCC	21ECT404	Communication Theory	ECE	3	0	0	1		03	50	50	100	3
5	PCC	21ECL405	Communication Laboratory I	ECE	0	0	2			03	50	50	100	1
6	AEC	21ECT406	Biology For Engineers		0	0	1			02	50	50	100	2
7	HSSC	21HST407	Samskrutika Kannada		1	0	0			01	50	50	100	1
		21HST407	Balake Kannada											
		OR												
		21HST408	Constitution of India and Professional Ethics											
8	AEC	21ECT409X	Ability Enhancement Course - IV							01	50	50	100	1
9	HSSC	21HSN410	Professional Skills	HSS	1	0	1	0		02	50	----	PP/NP	0
10	UHV	21HSN412	Universal Human Values	Any Department	1	0	0	1		01	50	50	100	1
11	INT	21ECI413	Inter/Intra Institutional Internship	Evaluation By the appropriate authorities	Completed during the intervening period ofII and III semesters by students admitted to first year of BE./B.Tech and during the intervening period of III and IV semesters by Lateral entry students admitted to III semester.					03	100		100	2
									Total		550	450	1000	22
Course Prescribed to Lateral Entry Diploma Holders Admitted to III Semester B.E. Program														
12		21MAN411	Additional Mathematics-II	Maths	1	0	0	1		02	50	----	PP/NP	0

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Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

Internship of 04 weeks during the intervening period of IV and V semesters; 21INT68Innovation/ Entrepreneurship/ Societal based Internship.

(1) All the students shall have to undergo a mandatory internship of 04 weeks during the intervening period of IV and V semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the VI semester grade card.The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be considered under F (fail) grade and shall have to complete during subsequently after satisfying the internship requirements.

(2) Innovation/ Entrepreneurship Internship shall be carried out at industry, State and Central Government /Non-government organizations (NGOs), micro, small and medium enterprise (MSME), Innovation centres or Incubation centres. Innovation need not be a single major breakthrough; it can also be a series of small or incremental changes. Innovation of any kind can also happen outside of the business world. Entrepreneurship internships offers a chance to gain hands on experience in the world of entrepreneurship and helps to learn what it takes to run a

small entrepreneurial business by performing intern duties with an established company. This experience can then be applied to future business endeavours. Start-ups and small companies are a preferred place to learn the business tack ticks for future entrepreneurs as learning how a small business operates will serve the intern well when he/she manages his/her own company. Entrepreneurship acts as a catalyst to open the minds to creativity and innovation. Entrepreneurship internship can be from several sectors, including technology, small and medium-sized, and the service sector.

(3) Societal or social internship. Urbanization is increasing on a global scale; and yet, half the world's population still resides in rural areas and is devoid of many things that urban population enjoy. Rural internship is a work-based activity in which students will have a chance to solve/reduce the problems of the rural place for better living. As proposed under the AICTE rural internship programme, activities under Societal or social internship, particularly in rural areas, shall be considered for 40 points under AICTE activity point programme.

Ability Enhancement Course - IV			
21ECT4091	Embedded C Basics	**21ECT4093**	Octave / Scilab for signals
21ECT4092	C++ Basics	**21ECT4094**	DAQ using LabVIEW

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

B.E: Electronics & Communication Engineering

NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2022 – 23)

SEMESTER - III

TRANSFORM CALCULUS, FOURIER SERIES AND NUMERICAL TECHNIQUES			
Course Code	**21MAT 301**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course objectives: The goal of the course Transform Calculus, Fourier series and Numerical techniques 21MAT 31 is

- To have an insight into solving ordinary differential equations by using Laplace transform techniques
- Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis.
- To enable the students to study Fourier Transforms and concepts of infinite Fourier Sine and Cosine transforms and to learn the method of solving difference equations by the z-transform method.
- To develop proficiency in solving ordinary and partial differential equations arising in engineering applications, using numerical methods

Teaching-Learning Process (General Instructions):

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied mathematical skills.
2. State the need for Mathematics with Engineering Studies and Provide real-life examples.
3. Support and guide the students for self–study.
4. You will also be responsible for assigning homework, gradingassignments and quizzes, and documenting students' progress.
5. Encourage the students for group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision of topics (post-lectureactivity).
   - As additional examples (post-lectureactivity).
   - As an additional material of challenging topics (pre-and post-lecture activity).
   - As a model solution for some exercises (post-lecture activity).

Module-1: Laplace Transform

Definition and Laplace transforms of elementary functions (statements only). Problems on Laplace's Transform of $e^{at}f(t)$, $t^n f(t)$, $\frac{f(t)}{t}$. Laplace transforms of Periodic functions (statement only) and unit-step function – problems.

Inverse Laplace transforms definition and problems, Convolution theorem to find the inverse Laplace transforms (without Proof) problems. Laplace transforms of derivatives, solution of differential equations. **(8 Hours)**

Self-study: Solution of simultaneous first-order differential equations.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation **(RBT Levels: L1, L2 and L3)**

Module-2: Fourier Series

Introduction to infinite series, convergence and divergence. Periodic functions, Dirichlet's condition. Fourier series of periodic functions with period 2π and arbitrary period. Half range Fourier series. Practical harmonic analysis.

Self-study: Convergence of series by D'Alembert's Ratio test and, Cauchy's root test.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation **(RBT Levels: L1, L2 and L3)**

Module-3: Infinite Fourier Transforms and Z-Transforms

Infinite Fourier transforms definition, Fourier sine and cosine transforms. Inverse Fourier transforms, Inverse Fourier cosine and sine transforms. Problems.

Difference equations, z-transform-definition, Standard z-transforms, Damping and shifting rules, Problems. Inverse z-transform and applications to solve difference equations.

Self Study: Initial value and final value theorems, problems.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation **(RBT Levels: L1, L2 and L3)**

Module-4: Numerical Solution of Partial Differential Equations

Classifications of second-order partial differential equations, finite difference approximations to derivatives, Solution of Laplace's equation using standard five-point formula. Solution of heat equation by Schmidt explicit formula and Crank- Nicholson method, Solution of the Wave equation. Problems.

Self Study: Solution of Poisson equations using standard five-point formula.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation **(RBT Levels: L1, L2 and L3)**

Module-5: Numerical Solution of Second-Order ODEs and Calculus of Variations

Second-order differential equations - Runge-Kutta method and Milne's predictor and corrector method. (No derivations of formulae).

Calculus of Variations: Functionals, Euler's equation, Problems on extremals of functional. Geodesics on a plane, Variational problems.

Self Study: Hanging chain problem.**(RBT Levels: L1, L2 and L3)**

Course outcomes: After successfully completing the course, the students will be able :

1. To solve ordinary differential equations using Laplace transform.
2. Demonstrate the Fourier series to study the behaviour of periodic functions and their applications in system communications, digital signal processing and field theory.
3. To use Fourier transforms to analyze problems involving continuous-time signals and to apply Z-Transform techniques to solve difference equations
4. To solve mathematical models represented by initial or boundary value problems involving partial differential equations

Determine the extremals of functionals using calculus of variations and solve problems arising in dynamics of rigid bodies and vibrational analysis.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures notless than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together **Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks**

(duration 01 hour)First test at the end of

5th week of the semester
Second test at the end of the 10th
week of the semesterThird test at the
end of the 15th week of the semester
Two assignments each of **10 Marks**
First assignment at the end of 4th week of
the semester Second assignment at the end
of 9th week of the semester
Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks**
(**duration 01 hours**)
At the end of the 13th week of the semester
The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be
scaled down to 50 marks
(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).
CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:
Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**
The question paper will have ten questions. Each question is set for 20 marks.
There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub- questions), **should have a mix of topics** under that module.
The students have to answer 5 full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books:

1. **B. S. Grewal**: "Higher Engineering Mathematics", Khanna publishers, 44th Ed.2018
2. **E. Kreyszig**:"Advanced Engineering Mathematics", John Wiley & Sons, 10th Ed. (Reprint), 2016.

Reference Books

1. **V. Ramana:** "Higher Engineering Mathematics" McGraw-Hill Education, 11th Ed.
2. **Srimanta Pal & Subodh C. Bhunia:** "Engineering Mathematics" Oxford University Press, 3rd Reprint,2016.
3. **N.P Bali and Manish Goyal**: "A textbook of Engineering Mathematics" Laxmi Publications, Latestedition.
4. **C. Ray Wylie, Louis C. Barrett:** "Advanced Engineering Mathematics" McGraw – Hill BookCo.Newyork, Latest ed.
5. **Gupta C.B, Sing S.R and Mukesh Kumar:** "Engineering Mathematic for Semester I and II", Mc- GrawHill Education(India) Pvt. Ltd 2015.
6. **H.K.Dass and Er. Rajnish Verma:** "Higher Engineering Mathematics" S.Chand Publication (2014).
7. **James Stewart: "**Calculus" Cengage publications, 7th edition, 4th Reprint 2019.

Web links and Video Lectures (e-Resources):

- http://.ac.in/courses.php?disciplineID=111
- http://www.class-central.com/subject/math(MOOCs)
- http://academicearth.org/
- http://www.bookstreet.in.

- VTU e-Shikshana Program
- VTU EDUSAT Program

Activity-Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes
- Assignments
- Seminars

Sub Title: Digital System Design Using Verilog		
Sub Code:21ECT302	**No. of Credits:4=**3:0:2:0 **(L: T: P: S)**	**No. of lecture hours/week: 4**
Exam Duration:3 hours	**CIE +Assignment + Group Activity + SEE =45 + 5 + 5+50 =100**	**Total No. of Contact Hours :53**

Course objectives: This course will enable students to:

1. To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
2. To impart the concepts of designing and analyzing combinational logic circuits.
3. To impart design methods and analysis of sequential logic circuits.
4. To impart the concepts of Verilog HDL-data flow and behavioral models for thedesign of digital systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.

Give Programming Assignments.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Principles of Combinational Logic**: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps- up to 4 variables, Quine-McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms. (Section 3.1 to 3.5 of Text 1).	08	L1, L2, L3
2	**Logic Design with MSI Components and Programmable Logic Devices**: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section 5.1 to 5.7 of Text 2)	08	L1, L2, L3

3	**Flip-Flops and its Applications**: The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, JK, D and SRflip-flops. (Section 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text 2)	08	L1, L2, L3
4	**Introduction to Verilog**: Typical Design Flow, Data types, Modules, Ports. **Verilog Data flow description:** Continuous assignments, Delays, Expressions, Operators, and operands, operator types, Examples (Section1.3, 3.2, 6.1 to 6.5 of Text 3)	08	L1, L2, L3
5	**Verilog Behavioral description:** Procedural Assignments, Conditional statements, Multiway branching, Loops, Examples. (Section 7.2, 7.4, 7.5, 7.6 and 7.9 of Text 3) **Verilog Structural description**: Gate types, Examples. (Section 5,1 of Text 3)	08	L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Using suitable simulation software, demonstrate the operation of the following circuits:

Sl.No	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program.
2	To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description: 8:1 mux, 8:3 encoder, Priority encoder
6	To realize using Verilog Behavioral description: 1:8 Demux, 3:8 decoder, 2-bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a) JK type b) SR type c) T type and d) D type
8	To realize Counters - up/down (BCD and binary) using Verilog Behavioral description.

Demonstration Experiments (For CIE only – not to be included for SEE)

Use FPGA/CPLD kits for downloading Verilog codes and check the output for interfacing experiments.

9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface a Relay or ADC to the FPGA/CPLD and demonstrate its working.
11	Verilog programs to interface DAC to the FPGA/CPLD for Waveform generation.
12	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From unit 1 and 2, Assignment2 from units 3,4 and 5
3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 1 - Digital teaching and learning

Course Outcomes

CO1 Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.

CO2 Analyze and design for combinational logic circuits.

CO3 Analyze the concepts of Flip Flops (SR, D, T and JK) and to design the synchronous sequential circuits using Flip Flops.

CO4 Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

COs	**Mapping with Pos**
CO1	PO1, PO2, PO3, PO4
CO2	PO1, PO2, PO3, PO4,
CO3	PO2, PO3, PO4, PO5, PO12
CO4	PO2, PO3, PO4, PO5, PO12

Text Book:

1. **Digital Logic Applications and Design** by John M Yarbrough, Thomson Learning, 2001.
2. **Digital Principles and Design by Donald D Givone**, McGraw Hill, 2002.
3. **Verilog HDL – A guide to Digital Design and Synthesis** by Samir Palnitkar**,** Pearson, 2003

Reference Books:

1. **Fundamentals of logic design**, by Charles H Roth Jr., Cengage Learning
2. **Logic Design,** by Sudhakar Samuel, Pearson/ Sanguine, 2007
3. **Fundamentals of HDL,** by Cyril P R, Pearson/Sanguine 2010

MOOCS:

1. Electronic Design Automation http://nptel.ac.in/courses/106105083/
2. Digital system design with PLDs and FPGA shttp://nptel.ac.in/courses/117108040/ Fundamentals of HDL

Sub Title: Basic Signal Processing		
Sub Code: 21ECT303	**No. of Credits:4=3: 0: 2 (L-T-P)**	**No. of lecture hours/week: 04**
Exam Duration: 3 Hours	**CIE +Group Activity + Assignment +SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Understanding the fundamental knowledge/ overview in the field of Signal Processing.
2. Familiarizing the concepts of vector spaces and orthogonality with a qualitative insight into applications in communications.
3. Understanding the mathematical description of discrete time signals and systems, and analyzing the signals in time domain using convolution sum,
4. To understand classifying signals into different categories based on their properties, and analyzing Linear Time Invariant (LTI) systems in time and transform domains.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Vector Spaces:** Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis and dimension, Dimensions of the four subspaces, Rank-Nullity Theorem, Linear Transformations Orthogonality: Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram-Schmidt Orthogonalization procedure **(Refer Chapters 2 and 3 of Text 1)**	08	L1, L2, L3.
2	**Eigen values and Eigen vectors:** Review of Eigen values and Diagonalization of a Matrix, Special Matrices (Positive Definite Symmetric) and their properties, Singular Value Decomposition. **(Refer Chapter 5, Text 1)**	06	L1, L2,L3
3	**Introduction and Classification of signals:** Definition of signal and systems with examples, Elementary signals/Functions: Exponential, sinusoidal, step, impulse and ramp functions Basic Operations on signals: Amplitude scaling, addition, multiplication, time scaling, time shift and time reversal. Expression of triangular, rectangular and other waveforms in terms of elementary signals System Classification and properties: Linear-nonlinear, Time variant -invariant, causal-noncausal, static-dynamic, stable-unstable, invertible. **(Refer Chapters 1 of Text 2) [Only for Discrete Signals & Systems]**	08	L1,L2,L3
4	**Time domain representation of LTI System**: Impulse response, convolution sum. Computation of convolution sum using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular. LTI system Properties in terms of impulse response: System interconnection, Memory less, Causal, Stable, Invertible and Deconvolution and step response **(Refer Chapters 2 of Text 2) [Only for Discrete Signals & Systems]**	09	L1,L2,L3
5	**The Z-Transforms**: Z transform, properties of the region of convergence, properties of the Z-transform, Inverse Z-transform by partial fraction, Causality and stability, Transform analysis of LTI systems. **(Refer Chapters 2 of Text 7)**	08	L1,L2,L3

PRACTICAL COMPONENT OF IPCC	
1	Program to create and modify a vector (array). b. Program to create and modify a matrix.
2	Programs on basic operations on matrix.
3	Program to solve system of linear equations.
4	Program for Gram-Schmidt orthogonalization.
5	Program to find Eigen value and Eigen vector.
6	Program to find Singular value decomposition.
7	Program to generate discrete waveforms.
8	Program to perform basic operation on signals
9	Program to perform convolution of two given sequences.
10	a. Program to perform verification of commutative property of convolution. b. Program to perform verification of distributive property of convolution. c. Program to perform verification of associative property of convolution.
11	Program to compute step response from the given impulse response.
12	Programs to find Z-transform and inverse Z-transform of a sequence.

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3. The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component

Course Outcomes: After the completion of the Course the student can:
CO1. Understand the basics of Linear Algebra
CO2. Analyze different types of signals and systems
CO3. Analyze the properties of discrete time signals & systems
CO4. Analyze discrete time signals & systems using Z transform

Cos	Mapping with Pos	Mapping with PSOs
CO1	PO1,PO2,PO3, PO4,PO5	PSO1,PSO2,PS03
CO2	PO1,PO2,PO3, PO4,PO5	PSO1,PSO2,PS03
CO3	PO1,PO2,PO3, PO4,PO5	PSO1,PSO2, PS03
CO4	PO1,PO2,PO3, PO4,PO5	PSO1,PSO2, PS03

Text Book:	
1.	Gilbert Strang, **"Linear Algebra and its Applications"**, Cengage Learning, 4th Edition, 2006, ISBN 97809802327
2.	Simon Haykin and Barry Van Veen, **"Signals and Systems"**, 2nd Edition, 2008, Wiley India. ISBN9971-51- 239-4.
Reference Books:	
1.	Michael Roberts, **"Fundamentals of Signals & Systems"**,2nd edition, Tata McGraw-Hill, 2010, ISBN978-0- 07-070221-9.
2.	Alan V Oppenheim, Alan S WiIIsky and S Hamid Nawab, **"Signals and Systems"** Pearson Education Asia / PHI, 2"" edition, 1997. Indian Reprint 2002.
3.	H P Hsu, R Ranjan, **"Signals and Systems",** Schaum's outlines, TMH, 2006.
4.	B P Lathi, "**Linear Systems and Signals**", Oxford University Press, 2005.
5.	S UdayaKumar, "**Signals and Systems**", 7th Edition Pristine Publishing House.
6.	Ganesh Rao and Satish Tunga, "**Signals and Systems**", Pearson/Sanguine.

Web Links:	
1.	Video lectures on Signals and Systems by Alan V Oppenheim Lecture 1, Introduction | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube Lecture Lecture 2, Signals and Systems: Part 1 | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube
2.	NPTEL video lectures signals and system: https://www.youtube.com/watch?v=7Z3LE5uM-6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ_9kfoqZyx
3.	Video lectures on Linear Algebra by Gilbert Strang https://www.youtube.com/watch?v=ZK3O402wf1c&list=PL49CF3715CB9EF31D&index=1

Sub Title: Analog Electronic Circuits		
Sub Code: 21ECT304	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 03**
Exam Duration: 3 Hours	**CIE +Group Activity + Assignment +SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives: This course will enable students to

1. Explain various BJT parameters, connections and configurations**.**
2. Design and demonstrate the diode circuits and transistor amplifiers.
3. Explain various types of FET biasing and demonstrate the use of FET amplifiers.
4. Analyze Power amplifier circuits in different modes of operation.
5. Construct Feedback and Oscillator circuits using FET.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor. Small signal operation and Models: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model, The T model. MOSFETs: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor. Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model. [Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.7), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.7)]	08	L1, L2, L3.
2	MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, Source follower. MOSFET internal capacitances and High frequency model: The gate capacitive effect, Junction capacitances, High frequency model. Frequency response of the CS amplifier: The three frequency bands, high frequency response, Low frequency response. Oscillators: FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) [Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]	08	L1, L2,L3

3	Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). Output Stages and Power Amplifiers: Introduction, Classification of output stages, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. [Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]	08	L1,L2,L3
4	Op-Amp Circuits: Op-amp DC and AC Amplifiers, DAC - Weighted resistor and R-2R ladder, ADC- Successive approximation type, Small Signal half wave rectifier, Absolute value output circuit, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. 555 Timer and its applications: Monostable and Astable Multivibrators. [Text 2: 6.2, 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2,8.13 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3,9.4.3(a)]	08	L1,L2,L3,L4
5	Overview of Power Electronic Systems: Power Electronic Systems, Power Electronic Converters and Applications. Thyristors: Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-off Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A without design consideration. Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit. [Text 3: 1.3, 1.5,1.6, 2.2, 2.3, 2.4,2.6, 2.7,2.9, 2.10, 3.2, 3.5.1, 3.5.2, 3.6.1, 3.6.3,3.6.4]	07	L1,L2,L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3. Unit 1- Digital Teaching and Learning

Course Outcomes: After the completion of the Course the student can:

CO1.Understand the characteristics of BJTs and FETs for switching and amplifier circuits.

CO2. Design and analyze FET amplifiers and oscillators with different circuit configurations and biasing conditions.

CO3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators.

CO4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.

Cos	Mapping with Pos	Mapping with PSOs
CO1	PO1 PO2 PO3 PO5	PSO1 PSO2
CO2	PO1 PO2 PO3	PSO1 PSO2
CO3	PO1 PO2 PO3	PSO1 PSO2
CO4	PO1 PO2 PO3	PSO1 PSO2

Text Book:	
1.	1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6th Edition, Oxford,2015. ISBN:978-0-19-808913-1
2.	2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education,2018. ISBN: 978-93-325-4991-3
3.	3. Electronic Principles, Albert Malvino, David J Bates, 7th Edition, McGraw Hill Education (India)Private Limited, 2017, ISBN:978-0-07-063424-4

Web Links:	
1.	www.nptel.in
2.	. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C.Halkias, McGraw-Hill, 2015.
3.	Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

Analog and Digital Electronics Lab			
Course Code	**21ECL305**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Study the static characteristics of SCR and test the RC triggering circuit.
- Design and test the combinational and sequential logic circuits for their functionalities.
- Use the suitable ICs based on the specifications and functions.

Sl.No.	Experiments
1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator and iii) RC Phase shift oscillator
3	Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator
4	Obtain the static characteristics of SCR and test SCR Controlled HWR and FWR using RC triggering circuit.
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor & Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.
8	Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192

9	Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod-16
10	Pseudorandom sequence generator using IC7495
11	Test the precision rectifiers using opamp: i) Half wave rectifier ii) Full wave rectifier
12	Design and test Monostable and Astable Multivibrator using 555 Timer

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Design and analyze the BJT/FET amplifier and oscillator circuits.
2. Design and test Opamp circuits to realize the mathematical computations, DAC and precision rectifiers.
3. Design and test the combinational logic circuits for the given specifications.
4. Test the sequential logic circuits for the given functionality.
5. Demonstrate the basic electronic circuit experiments using SCR and 555 timer.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Fundamentals of Electronic Devices and Circuits Lab Manual, David A Bell, 5th Edition, 2009, Oxford University Press.
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition.

III Semester –Ability Enhancement courses

LD (Logic Design) Lab using Pspice / MultiSIM			
Course Code	**21ECT3091**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

- Impart the concepts of De Morgan's Theorem, SOP, POS forms.
- Impart the concepts of designing and analyzing combinational logic circuits.
- Impart the concepts of analysis of sequential logic circuits.
- Analyze and design any given synchronous sequential circuits.

Sl.No	Experiments
1	Implementation of De Morgan's theorem and SOP/POS expressions using Pspice/Multisim.
2	Implementation of Half Adder, Full Adder, Half Subtractor and Full Subtractor using Pspice/ Multisim.
3	Design and implementation of 4-bit Parallel Adder/ Subtractor using IC 7483 and BCD to Excess-3 code conversion and vice-versa using Pspice/Multisim.
4	Design and implement of IC 7485 5-bit magnitude comparator using Pspice/Multisim.
5	To Realize Adder & Subtractor using IC 74153 (4:1 MUX) and 4-variable function using IC74151 (8:1MUX) using Pspice/Multisim.
6	To realize Adder and Subtractor using IC 74139/ 74155N (Demux/Decoder) and Binary to Gray code conversion & vice versa using 74139/ 74155N using Pspice/Multisim.
7	SR, Master-Slave JK, D & T flip-flops using NAND Gates using Pspice/Multisim.
8	Design and realize the Synchronous counters (up/down decade/binary) using Pspice/Multisim.
9	Realize the shift registers and their modes (SISO, PISO, PIPO, SIPO) using 7474/7495 using Pspice/Multisim.
10	Design Pseudo Random Sequence generator using 7495 using Pspice/Multisim.
11	Design Serial Adder with Accumulator and simulate using Pspice/Multisim.
12	Design using Pspice/Multisim Mod-N Counters.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Demonstrate the truth table of various expressions and combinational circuits using logic gates.
2. Design various combinational circuits such as adders, subtractors, comparators, multiplexers and code converters.
3. Construct flips-flops, counters and shift registers.
4. Design and implement synchronous counters.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student

shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

- Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001
- Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.

AEC (Analog Electronic Circuits) Lab			
Course Code	21ECT3092	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	2

Course objectives:

- To provide practical exposure to the students on designing, setting up, executing and debugging various electronic circuits using simulation software.
- To give the knowledge and practical exposure on simple applications of analog electronic circuits.

Sl.No	Experiments using Pspice/MultiSIM software
1	Experiments to realize diode clipping (single, double ended) circuits.
2	Experiments to realize diode clamping (positive, negative) circuits.
3	Experiments to realize Full wave rectifier without filter (and set-up to measure the ripple factor, Vp-p, Vrms, etc.).
4	Design and conduct an experiment on Series Voltage Regulator using Zener diode to determine line/load regulation characteristics.
5	Realize BJT Darlington Emitter follower without bootstrapping and determine the gain, input and output impedances (other configurations of emitter follower can also be considered).
6	Set-up and study the working of complementary symmetry class B push pull power amplifier (other power amplifiers can also be suitably considered) and calculate the efficiency.
7	Design and set-up the oscillator circuits (Hartley, Colpitts, etc. using BJT/FET) and determine the frequency of oscillation.
8	Design and set-up the crystal oscillator and determine the frequency of oscillation.
9	Experiment to realize Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.
10	Experiments to realize Transfer and drain characteristics of a MOSFET.
11	Experiments to realize UJT triggering circuit for Controlled Full wave Rectifier.
12	Design and simulation of Regulated power supply.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Understand the circuit schematic and its working.
2. Study the characteristics of different electronic devices.
3. Design and test simple electronic circuits as per the specifications using discrete electronic components.
4. Compute the parameters from the characteristics of active devices.
5. Familiarize with EDA software which can be used for electronic circuit simulation.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book.

Suggested Learning Resources:

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.
2. Muhammed H Rashid, "Introduction to PSpice using OrCAD for circuits and electronics", 3rd Edition, Prentice Hall, 2003.

III Semester

<table>
<tr><th colspan="5">LIC (Linear Integrated Circuits) Lab using Pspice / MultiSIM</th></tr>
<tr><td colspan="2">Course Code</td><td>21ECT3093</td><td>CIE Marks</td><td>50</td></tr>
<tr><td colspan="2">Teaching Hours/Week (L:T:P: S)</td><td>0:0:2:0</td><td>SEE Marks</td><td>50</td></tr>
<tr><td colspan="2">Credits</td><td>1</td><td>Exam Hours</td><td>100</td></tr>
<tr><td colspan="5">Course objectives:
To apply operational amplifiers in linear and nonlinear applications.
To acquire the basic knowledge of special function ICs.
To use Multisim/Pspice software for circuit design and simulation</td></tr>
<tr><td>Sl.No</td><td colspan="4">Experiments using Pspice / MultiSIM
Every experiment has to be designed, circuit to be drawn / constructed and executed in the specified software. Results are also to be noted and inferred.</td></tr>
<tr><td></td><td colspan="4">Note: Standard design procedure to be adopted.</td></tr>
<tr><td>1</td><td colspan="4">To realize using op-amp an Inverting Amplifier and Non-Inverting Amplifier</td></tr>
<tr><td>2</td><td colspan="4">To realize using op-amps i) Summing Amplifier ii)Difference amplifier</td></tr>
<tr><td>3</td><td colspan="4">To realize using op-amps an Instrumentation Amplifier</td></tr>
<tr><td>4</td><td colspan="4">To realize using op-amps i) Differentiator ii)Integrator</td></tr>
<tr><td>5</td><td colspan="4">To realize using op-amps a Full wave Precision Rectifier</td></tr>
<tr><td>6</td><td colspan="4">To realize using op-amps
Inverting and Non-Inverting Zero Crossing Detectors
Positive and Negative Voltage level detectors</td></tr>
<tr><td>7</td><td colspan="4">To realize using op-amp an Inverting Schmitt Trigger</td></tr>
<tr><td>8</td><td colspan="4">To realize using op-amp an Astable Multivibrator</td></tr>
<tr><td>9</td><td colspan="4">To design and implement using op-amps
Butterworth I & II order Low Pass Filter
Butterworth I & II order High Pass Filter</td></tr>
<tr><td>10</td><td colspan="4">To design and implement using op-amp a RC Phase Shift Oscillator</td></tr>
<tr><td>11</td><td colspan="4">To design and implement Mono-stable Multivibrator using 555 timer</td></tr>
<tr><td>12</td><td colspan="4">To design and implement 4 - bit R-2R Digital to Analog Converter</td></tr>
<tr><td colspan="5">Course outcomes (Course Skill Set):
After studying this course, students will be able to;
Sketch/draw circuit schematics, construct circuits, analyze and troubleshoot circuits containing op-amps, resistors, diodes, capacitors and independent sources.
Relate to the manufacturer's data sheets of IC 555 timer and IC μa741 op-amp.
Realize and verify the operation of analog integrated circuits like Amplifiers, Precision Rectifiers, Comparators and Waveform generators.
Design and implement analog integrated circuits like Oscillators, Active filters, Timer circuits, Data converters and compare the experimental results with theoretical values.</td></tr>
</table>

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018.

III Semester

LabVIEW Programming Basics			
Course Code	**21ECT3094**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

- Aware of various front panel controls and indicators.
- Connect and manipulate nodes and wires in the block diagram.
- Locate various toolbars and pull-down menus for the purpose of implementing specific functions.
- Locate and utilize the context help window.
- Familiar with LabVIEW and different applications using it.
- Run a Virtual Instrument (VI).

Sl.No	**VI Programs (using LabVIEW software) to realize the following:**
1	Basic arithmetic operations: addition, subtraction, multiplication and division
2	Boolean operations: AND, OR, XOR, NOT and NAND
3	Sum of 'n' numbers using 'for' loop
4	Factorial of a given number using 'for' loop
5	Determine square of a given number
6	Factorial of a given number using 'while 'loop
7	Sorting even numbers using 'while' loop in an array
8	Finding the array maximum and array minimum
	Demonstration Experiments (For CIE)
9	Build a Virtual Instrument that simulates a heating and cooling system. The system must be able to be controlled manually or automatically.
10	Build a Virtual Instrument that simulates a Basic Calculator (using formula node).
11	Build a Virtual Instrument that simulates a Water Level Detector.
12	Demonstrate how to create a basic VI which calculates the area and perimeter of a circle.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Use Lab VIEW to create data acquisition, analysis and display operations
2. Create user interfaces with charts, graph and buttons
3. Use the programming structures and data types that exist in Lab VIEW
4. Use various editing and debugging techniques

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.

The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI, 2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGraw Hill, Second Edition, 2011.

IV Semester

<table>
<tr><th colspan="4">Maths for Communication Engineers</th></tr>
<tr><td>Course Code</td><td>21MAT401</td><td>CIE Marks</td><td>50</td></tr>
<tr><td>Teaching Hours/Week (L:T:P:S)</td><td>3:0:0:1</td><td>SEE Marks</td><td>50</td></tr>
<tr><td>Total Hours of Pedagogy</td><td>40</td><td>Total Marks</td><td>100</td></tr>
<tr><td>Credits</td><td>3</td><td>Exam Hours</td><td>3</td></tr>
<tr><td colspan="4">Course objectives:
To facilitate the students in understanding the Concepts of Electric and Magnetic Fields through Mathematical representations.
To enable the students in using the concepts of Field theory to arrive at important Mathematical relations associated with Electromagnetic waves.
To provide a foundation in Random variables and Random Processes which find application in Communication.</td></tr>
<tr><td colspan="4">Teaching-Learning Process (General Instructions)
The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:
Explain the importance of Mathematics in Communication links and Prerequisites of the course.
Prepare handouts of related problems and encourage the doubts.
Prepare assignment questions related to theory and problems.
Prepare concept-based quiz questions.
Encourage short videos available on web related to important topics of Digital Signal Processing.
Encourage Students to create a forum wherein they can discuss theoretical concepts and problems.</td></tr>
<tr><td colspan="4">Prerequisites:
[i] Vector Analysis – Scalars and Vectors, Vector Algebra, Rectangular, Cylindrical and Spherical Coordinate system, Vector components and Unit vectors, Scalar and Vector fields, Dot product, cross product, Vector differentiation, Vector integration [Revise Module-2 of 21MAT21 course]
[ii] Probability Basics- Why Probability? Axioms and Properties of Probability, Finding Probability Values, Conditional Probabilities and Independence, Independence among n events, Partitions</td></tr>
<tr><td colspan="4">Module-1: Static Electric Field and Flux Density</td></tr>
<tr><td colspan="4">Coulomb's Law and Electric Field Intensity: The Experimental law of Coulomb, Electric Field Intensity, Field of a line charge
Electric Flux Density and Gauss-Divergence Theorem: Electric Flux Density, Gauss' Law, Application of Gauss' Law for a Differential Volume Element, Divergence, Maxwell's First Equation, Divergence Theorem (From Text-1)</td></tr>
<tr><td>Teaching-Learning Process</td><td colspan="3">Chalk and talk method/Power point presentation
Self-Study: Electric Field of a Sheet of Charge
RBT Level: L1, L2, L3</td></tr>
<tr><td colspan="4">Module-2: Electric Potential, Current Density and Steady Magnetic Field</td></tr>
<tr><td colspan="4">Electric Potential: Energy Expended in moving a point charge in an Electric field, The Line Integral, Definition of Potential Difference and Potential, Potential field of a point charge, Potential Gradient
Current Density: Current and Current Density, Current Continuity Equation
Steady Magnetic field: Biot-Savart's Law, Ampere's Circuital Law (Statement, Illustration and Mathematical representation), Curl, Stokes' Theorem, Magnetic Flux and Flux density (From Text-1)</td></tr>
</table>

Teaching-Learning Process	Chalk and talk method/Power point presentation **Self-Study:** Conductor Properties and Boundary Conditions, Scalar and Vector Magnetic Potential **RBT Level:** L1, L2, L3

Module-3: Time Varying Fields, Maxwell's Equations and Uniform Plane Wave

Time Varying Fields and Maxwell's Equations: Faraday's Law, Displacement Current, Maxwell's Equations in Point Form, Maxwell's Equations in Integral Form
Uniform Plane Wave: Wave Propagation in Free Space, Wave Propagation in Dielectrics, Poynting's Theorem and Wave Power, Propagation in Good Conductors: Skin Depth (From Text-1)

Teaching-Learning Process	Chalk and talk method/Power point presentation **Self-Study:** Reflection of Uniform Plane Waves at Normal Incidence, Standing Wave Ratio **RBT Level:** L1, L2, L3

Module-4: Single Random Variables

Single Random Variables: Definition of Random Variables, Cumulative Distribution Function, Continuous and Discrete Random Variables, Expectations, Characteristic Functions, Functions of Single Random Variables, Conditioned Random Variables (From Text-2)

Teaching-Learning Process	Chalk and talk method/Power point presentation **Self-Study:** Multiple Random Variables **RBT Level:** L1, L2, L3

Module-5: Random Processes

Random Processes: Ensemble, PDF, Independence, Expectations, Stationarity, Correlation Functions (ACF, CCF, Addition and Multiplication), Ergodic Random Processes, Power Spectral Densities (Wiener Khinchin, Addition and Multiplication of RPs, Cross Spectral Densities), Linear Systems (Output Mean, Cross-Correlation and Autocorrelation of Input and Output), Noise (From Text-2)

Teaching-Learning Process	Chalk and talk method/Power point presentation **Self-Study:** Matched Filters **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Recall the basic laws and definitions (with mathematical representations) in Electric and Magnetic fields.
2. Apply the basic laws of Electric and Magnetic fields to arrive at Divergence Theorem, Current continuity Equation, Curl, Stokes' theorem.
3. Apply Electric and Magnetic field concepts to arrive at Maxwell's equations, Electromagnetic wave equations and Poynting's theorem (Important concepts related to Communication link).
4. Recall the definitions related to Random variables and Random Processes.
5. Model the Random events in the Communication set-up and determine useful statistical parameters.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester

2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Books:

1. W H Hayt and J A Buck, "Engineering Electromagnetics", Mc Graw Education, 8th Edition, 2014.
2. Richard H Williams, "Probability, Statistics, and Random Processes for Engineers", Cengage Learning, Second Indian Reprint, 2019.

Reference Books:

1. Mathew N O Sadiku, "Elements of Electromagnetics", Oxford University Press, 4th edition, 2007.
2. Joseph A Edminister, "Electromagnetics", Schaum's Outlines, Revised 2nd Edition, 2017.
3. E C Jordan and K G Balmain, "Electromagnetic Waves and Radiating Systems ", Pearson, 2nd Edition, 2015.
4. Hwei P Hsu, "Theory and Problems of Probability, Random Variables and Random Processes", Schaum's Outlines, Mc Graw Hill, 2017.
5. K N Hari Bhat, K Anitha Sheela and Jayant Ganguly, "Probability Theory and Stochastic Processes for Engineers", Cengage Learning, 2019.

Web links and Video Lectures (e-Resources)

- https://nptel.ac.in/courses/108106073
- https://archive.nptel.ac.in/courses/117/105/117105085

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Form multiple teams in the class and suggest them to prepare charts/models/animations or conduct an interactive quiz based on concepts of the course.

Sub Title : Digital Signal Processing		
Sub Code: 21ECT402	**No. of Credits: 4=3 : 0 : 2 (L-T-P)**	**No. of lecture hours/week : 05**
Exam Duration : 3 Hours	**CIE +Group Activity Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. **Preparation:** To prepare students with fundamental knowledge/ overview in the field of Digital Signal Processing.
2. **Core Competence:** To equip students with a basic foundation of Signal Processing by delivering the basics of Discrete Fourier Transforms & their properties, design of filters and overview of digital signal processors.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level
1	**Discrete Fourier Transforms (DFT):** Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation. 1. **Properties of the DFT:** Periodicity, Linearity and Symmetry properties, circular time shift & circular frequency shift property, Multiplication of two DFTs and Circular Convolution [Text 1]	09	L1, L2, L3.
2	**Linear filtering methods based on the DFT:** Use of DFT in Linear Filtering, Filtering of Long data Sequences. **Fast-Fourier-Transform (FFT) algorithms:** Efficient Computation of the DFT: Radix-2 FFT algorithms: DIT-FFT and DIF-FFT for the computation of DFT and IDFT [Text 1]	09	L1, L2,L3
3	**Design of FIR Filters:** Characteristics of practical frequency-selective filters, Symmetric and Anti- symmetric FIR filters, Design of Linear-phase FIR (low pass and High pass) filters using windows - Rectangular, Hamming, Hanning and Bartlett windows. **Structure for FIR Systems:** Direct form, Cascade form and Lattice structures [Text1] [Text 2]	11	L1,L2,L3
4	**IIR Filter Design:** Infinite Impulse response filter format, Bilinear Transformation Design method: Analog Filters using Low pass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth (Lowpass and Highpass) Filter Design using BLT. **Realization of IIR Filters:** Direct form I and II [Text 2]	11	L1,L2,L3
5	**Digital Signal Processors:** DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, FIR and IIR filter implementations in Fixed point systems. [Text 2]	12	L1,L2,L3

PRACTICAL COMPONENT OF IPCC
List of Programs to be implemented & executed using any programming languages like C++/Python/Java/Scilab / MATLAB/CC Studio (but not limited to) 1. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum. 2. Computation of circular convolution of two given sequences and verification of commutative, distributive and associative property of convolution. 3. Computation of linear convolution of two sequences using DFT and IDFT. 4. Computation of circular convolution of two given sequences using DFT and IDFT 5. Verification of Linearity property, circular time shift property & circular frequency shift property of DFT. 6. Design and implementation of IIR (Butterworth) low pass filter to meet given specifications. 7. Design and implementation of IIR (Butterworth) high pass filter to meet given specifications. 8. Design and implementation of low pass FIR filter to meet given specifications. 9. Design and implementation of high pass FIR filter to meet given specifications. 10. To compute N- Point DFT of a given sequence using DSK 6713 simulator 11. To compute linear convolution of two given sequences using DSK 6713 simulator 12. To compute circular convolution of two given sequences using DSK 6713 simulator

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Determine response of LTI systems using time domain and DFT techniques
2. Compute DFT of real and complex discrete time signals
3. Compute DFT using FFT algorithms
4. Design FIR and IIR Digital Filters
5. Design of Digital Filters and processing of digital signals using DSP processor

Note 1: Unit 1, 2, 3, 4 and Unit 5 will have internal choice.
Note 2: Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2 Assignment - 2 from units 3, 4 and 5.
Note 3: Teaching-Learning Process: Chalk and Talk, YouTube videos, Programming assignments
Note 4: The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated only by CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.

Cos	Mapping with Pos	Mapping with PSOs
CO1	PO1,PO2,PO3	PSO1,PSO2,PS03
CO2	PO1,PO2,PO4,PO8,PO9,PO12	PSO1,PSO2,PS03
CO3	PO1,PO2,PO3,PO4,PO5,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03
CO4	PO1,PO2,PO3,PO4,PO5,PO6,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03
CO5	PO1,PO2,PO3,PO4,PO5,PO6,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03

Text Books:	
1.	Proakis & Manolakis, “Digital Signal Processing - Principles Algorithms & Applications”, 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2.	Li Tan, Jean Jiang, “Digital Signal processing - Fundamentals and Applications”, Academic Press, 2013, ISBN: 978-0-12-415893.

Reference Books:	
1.	Sanjit K Mitra, “Digital Signal Processing, A Computer Based Approach”, 4th Edition, McGraw Hill Education, 2013.
2.	Oppenheim & Schaffer, “Discrete Time Signal Processing", PHI, 2003.
3.	D Ganesh Rao and Vineeth P Gejji, “Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

Web Links:	
1.	By Prof. S. C. Dutta Roy, IIT Delhi https://nptel.ac.in/courses/117102060
2.	MIT OpenCourseWare https://youtu.be/rkvEM5Y3N60

Subject Title : Circuit analysis and control systems

Sub.Code: 21ECT403	No. of Credits:4=2:1:1 (L - T– P)	No. of Lecture Hours/Week : 06
Exam Duration:03 Hrs	CIE+Assignment +SEE=45+5+50=100	Total No.of Contact Hours:78

Course Learning Objectives:

From this course, the students can learn

1. Network analysis techniques and theorems for solving the electrical circuits
2. Applying Laplace transforms to analyse electrical circuits and two port network concepts.
3. The feedback control systems and modelling of the control systems in DEs and Transfer function approach.
4. The time response of control systems and examining the stability of control systems.
5. Analysis of control systems using root-locus and bode-plots.
6. State variable modeling of control systems.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Basic Circuit Concepts:** Ideal and Practical sources, Network reduction using Source transformations, Source Shifting and Star Delta transformation, duality of networks, Loop and Nodal analysis with linearly dependent and independent sources for both DC and AC networks, Concepts of super node and super mesh analysis, Numerical examples. **Network Theorems:** Thevenin's Theorem, Norton's Theorem, Superposition Theorem, Reciprocity Theorem, Maximum Power transfer theorem. Numerical examples *TEXT 1.*	10	L1,L2,L3.L4
2	**Laplace Transforms:** Introduction, Properties and theorems of Laplace Transforms, DC response of electrical circuits with and without initial conditions. **Two port network parameters:** Definitions of Z,Y,T and h- parameters, modeling of two port network parameters, Conditions for Symmetry and Reciprocity, series, parallel and Cascade Connection of Two Port Networks. *TEXT 1.*	10	L1,L2,L3.L4
3	**Introduction to Control systems:** Introduction**,** Types of Control systems, Effect of feedback systems and requirements of good control systems: **Mathematical Modeling of Control Systems:** Modeling of mechanical systems (Rotational and Translational excluding Lever and Gear trains systems). Transfer functions (Multivariable systems), Modeling of Electrical systems (Current and voltage analogy) Electromechanical Systems and its Analogous systems and DC Motors (Armature and Field controlled). **Block diagrams:** Block diagram of a closed loop systems and its reduction techniques, Transfer Functions (Multivariable Systems), Applications of Block diagram **Signal Flow Graphs:** Mason's gain formula, Basic properties of Signal flow graph, Transfer Functions-(Multivariable systems), Construction of Signal	10	L1,L2,L3.L4

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	flow graph for closed loop control systems, and Applications of Signal Flow Graphs. *TEXT 2.*		
4	**Time Response of feedback control systems:** Time response of control systems**,** Standard test signals, Unit step response of First and Second order Systems. Time response specifications and its derivations, Time response specifications of second order systems, steady state errors and Error constants. Types of control systems(Steady state error for Type 0,1 and 2 systems) **Stability analysis:** Concepts of stability, Necessary conditions for Stability, Routh stability criterion, Difficulties in the formulation of the Routh table, Relative stability analysis *TEXT 2.*	10	L1,L2,L3.L4
5	**Root Locus:** Introduction, Root locus concepts, Construction of Root loci, Rules for the construction of Root-Locus (negative feedback systems), Numerical examples. **Frequency responses analysis:** Introduction, Frequency domain specifications (No derivations, Numerical examples), Correlation between time and frequency response for second order systems. Bode plots, General procedure for constructing the Bode plots (Basic factors), Calculation of transfer function from Magnitude plot, Computation of Gain and Phase Margins from Bode plot, Gain adjustment in Bode Plot. **State Space Analysis:** Introduction, Concept of State, State variables & State model, State space representation for dynamic systems (Phase variables and Canonical Variables), Solution of state equations. *TEXT2.*	12	L1,L2,L3.L4

Note 1: Unit 3 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

After successful completion of this course, the students will be able to

CO1: Apply Network analysis techniques and network theorems to solve electrical circuits.
CO2: Analyze electrical circuits using Laplace transforms and explain two port network parameters.
CO3: Obtain mathematical model (both DE and TF approach) and analogous systems for the given systems.
CO4: Explain time response of control systems and examine stability using RH criterion
CO5: Analyze the stability of control systems using Root-Locus and Bode-plots method, and obtain the state space models for the given systems.

Text Books.

1 Charles K Alexander and Mathew N O Sadiku, "Fundamentals of Electric Circuits", 3rd edition, Tata McGraw-Hill, 2009.

2 J.Nagarath and M.Gopal, "Control Systems Engineering", 5th Edition, New Age International (P) Limited Publishers, 2005

Reference Text Books.

1 K.Ogata, "Modern Control Engineering", 4th Edition, Pearson Education Asia/PHI, 2002.
2 Benjamin C. Kuo, "Automatic Control Systems" , 9th Edition, John Wiley India Pvt. Ltd., 2008
3 Joseph J Distefano III et al., "Feedback and Control System", 2nd Edition, Schaum's Outlines, TMH, 2007.
4 Roy Choudhury, "Networks and systems", 2nd edition, New Age International Publications, 2006
5 M.E. Van Valkenberg, "Network analysis", 3rd edition, Prentice Hall of india Publishers, 2000

Web Links.

1 https://www.electrical4u.com/mathematical-modelling-of-various-system/.
2 https://www.tutorialspoint.com/control_systems/control_systems_time_response_analysis.htm.
3 www.facstaff.bucknell.edu/mastascu/econtrolhtml/rootlocus/rlocus1a.html.
4 lpsa.swarthmore.edu/Bode/BodeExamples.html.
5 https://www.calvin.edu/~pribeiro/courses/engr332/Handouts/nyquist-margins.htm.
6 nptel.ac.in/courses/108103008/25.

COs	POs	PSOs
CO1	PO1, PO2, PO3, PO5	PSO1, PSO2
CO2	PO1, PO2, PO3, PO5	PSO1, PSO2
CO3	PO1, PO2, PO3, PO5	PSO1, PSO2
CO4	PO1, PO2, PO3, PO5	PSO1, PSO2
CO5	PO1, PO2, PO3, PO5	PSO1, PSO2

Practical Component

Sl. No.	Experiments
1	Verification of Superposition theorem using PSPICE
2	Verification of Thevenin's theorem using PSPICE
3	Verification of Norton's theorem using PSPICE
4	Determination of time response of second order systems using PSPICE.
5	Draw root locus using MATLAB
6	Draw BODE PLOTs using MATLAB
7	Study the effect of PI controller using MATLAB
8	Study the effect of PD controller using MATLAB
9	Study the effect of PID controller using MATLAB
10	Study of speed characteristics of DC motors using MATLAB.

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Sub Title : Communication Theory		
Sub Code: 21ECT404	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity +Assignment +SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand and analyse concepts of Analog Modulation schemes viz; AM, FM., Low passsampling and Quantization as a random process.
2. Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.
3. Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.
4. Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at a receiver.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**AMPLITUDE MODULATION:** Introduction, Amplitude Modulation: Time & Frequency Domaindescription, switching modulator, Envelop detector. **DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION:** Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. **SINGLE SIDE–BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION:** SSB Modulation, VSB Modulation, Frequency Translation, Frequency Division Multiplexing. [Text1: 3.1 to 3.8]	09	L1, L2, L3.
2	**ANGLE MODULATION:** Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM,Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase–Locked Loop: Nonlinear model of PLL, Linear model of PLL. The Super Heterodyne Receiver [Text1: 4.1 to 4.6]	08	L1, L2,L3
3	**NOISE**: Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth. **NOISE IN ANALOG MODULATION**: Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Pre-emphasis and De-emphasis in FM (Text1: 5.10, 6.1 to 6.6)	08	L1,L2,L3
4	**SAMPLING AND QUANTIZATION:** Introduction, Why Digitize Analog Sources? The Low Pass Sampling Process, Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves. (Text1: 7.1 to 7.7)	07	L1,L2,L3
5	**SAMPLING AND QUANTIZATION (Contd):** The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation (Text1: 7.8 to 7.10), Application examples - (a) Video + MPEG (Text1:7.11) and (b) Vocoders (refer Section 6.8 of Reference Book 1)	07	L1,L2,L3

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

At the end of the course the student will be able to:

CO1. Able to understand and analyze modulation and demodulation techniques for AM, DSBSC, SSB-SC and VSB-SC.

CO2. Able to understand and analyze modulation and demodulation techniques for Angle Modulation.

CO3. Able to characterize the influence of channel noise on analog modulated signals.

CO4. Able to understand and analyze Sampling of Low pass signals, pulse amplitude modulation, pulse position modulation

CO5. Able to understand and analyze PCM, Quantization and Delta Modulation. Illustration of digital formatting representations used for Multiplexers, Vocoders and Video transmission.

Cos	Mapping with POs	Mapping with PSOs
CO1	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12	PSO1,PSO2
CO2	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12	PSO1,PSO2
CO3	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12	PSO1,PSO2
CO4	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12	PSO1,PSO2
CO5	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12	PSO1,PSO2

Text Book:

1. Simon Haykins & Moher, **"Communication Systems"**, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books:

1. B P Lathi and Zhi Ding, **"Modern Digital and Analog Communication Systems"**, Oxford University Press., 4th edition, 2010, ISBN: 97801980738002
2. S *y* India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3. H Taub & D L Schilling, **"Principles of Communication Systems"**, TMH, 2011.

Web Links: www.nptel.in

Communication Laboratory I			
Course Code	**21ECL405**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Model an analog communication system signal transmission and reception.
- Realize the electronic circuits to perform analog and pulse modulations and demodulations.
- Verify the sampling theorem and relate the signal and its spectrum before and after sampling.
- Understand the process of PCM and delta modulations.
- Understand the PLL operation.

Sl.No.	Experiments
1	Design of active second order Butterworth low pass and high pass filters.
2	Amplitude Modulation and Demodulation of (a) Standard AM and (b) DSBSC (LM741 and LF398 ICs can be used)
3	Frequency modulation and demodulation
4	Design and test Time Division Multiplexing and Demultiplexing of two bandlimited signals.
5	Design and test i) Pulse sampling, flat top sampling and reconstruction. ii) Pulse amplitude modulation and demodulation.
6	Design and test BJT/FET Mixer
7	Pulse Code Modulation and demodulation
8	Phase locked loop Synthesis
9	Illustration of (a) AM modulation and demodulation and display the signal and its spectrum. (b) DSB-SC modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)
10	Illustration of FM modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)
11	Illustrate the process of sampling and reconstruction of low pass signals. Display the signals and its spectrums of both analog and sampled signals. (Use MATLAB/SCILAB).
12	Illustration of Delta Modulation and the effects of step size selection in the design of DM encoder. (Use MATLAB/SCILAB)

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Demonstrate the AM and FM modulation and demodulation by representing the signals in time and frequency domain.
2. Design and test the sampling, Multiplexing and PAM with relevant circuits.
3. Demonstrate the basic circuitry and operations used in AM and FM receivers.
4. Illustrate the operation of PCM and delta modulations for different input conditions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.
(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Louis E Frenzel, Principles of Electronic Communication Systems, McGraw Hill Education (India) Private Limited, 2016.
2. B P Lathi, Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press, 2015.

Embedded C Basics			
Course Code	**21ECT4091**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

- Understand the basic programming of Microprocessor and microcontroller.
- To develop the microcontroller-based programs for various applications.

Sl.No	Experiments
	Conduct the following experiments by writing C Program using Keil microvision simulator (any 8051 microcontroller can be chosen as the target).
1	Write a 8051 C program to multiply two 16 bit binary numbers.
2	Write a 8051 C program to find the sum of first 10 integer numbers.
3	Write a 8051 C program to find factorial of a given number.
4	Write a 8051 C program to add an array of 16 bit numbers and store the 32 bit result in internal RAM
5	Write a 8051 C program to find the square of a number (1 to 10) using look-up table.
6	Write a 8051 C program to find the largest/smallest number in an array of 32 numbers
7	Write a 8051 C program to arrange a series of 32 bit numbers in ascending/descending order
8	Write a 8051 C program to count the number of ones and zeros in two consecutive memory locations.
9	Write a 8051 C program to scan a series of 32 bit numbers to find how many are negative.
10	Write a 8051 C program to display "Hello World" message (either in simulation mode or interface an LCD display).
11	Write a 8051 C program to convert the hexadecimal data 0xCFh to decimal and display the digits on ports P0, P1 and P2 (port window in simulator).

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Write C programs in 8051 for solving simple problems that manipulate input data using different instructions of 8051 C.
2. Develop testing and experimental procedures on 8051 Microcontroller, analyze their operation under different cases.
3. Develop programs for 8051 Microcontroller to implement real world problems.
4. Design and Develop Mini projects

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.

Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.

Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).

Weightage to be given for neatness and submission of record/write-up on time.

Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.

In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

The suitable rubrics can be designed to evaluate each student's performance and learning ability.

Rubrics suggested in Annexure-II of Regulation book

The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

"The 8051 Microcontroller: Hardware, Software and Applications", V Udayashankara and M S Mallikarjuna Swamy, McGraw Hill Education, 1st edition, 2017.

IV Semester

C++ Basics			
Course Code	**21ECT4092**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

- Understand object-oriented programming concepts, and apply them in solving problems.
- To create, debug and run simple C++ programs.
- Introduce the concepts of functions, friend functions, inheritance, polymorphism and function overloading.
- Introduce the concepts of exception handling and multithreading.

Sl.No	Experiments
1	Write a C++ program to find largest, smallest & second largest of three numbers using inline functions MAX & Min.
2	Write a C++ program to calculate the volume of different geometric shapes like cube, cylinder and sphere using function overloading concept.
3	Define a STUDENT class with USN, Name & Marks in 3 tests of a subject. Declare an array of 10 STUDENT objects. Using appropriate functions, find the average of the two better marks for each student. Print the USN, Name & the average marks of all the students.
4	Write a C++ program to create class called MATRIX using two-dimensional array of integers, by overloading the operator == which checks the compatibility of two matrices to be added and subtracted. Perform the addition and subtraction by overloading + and – operators respectively. Display the results by overloading the operator <<. If (m1 == m2) then m3 = m1 + m2 and m4 = m1 – m2 else display error
5	Demonstrate simple inheritance concept by creating a base class FATHER with data members: *First Name, Surname, DOB & bank Balance* and creating a derived class SON, which inherits: Surname & Bank Balance feature from base class but provides its own feature: First Name & DOB. Create & initialize F1 & S1 objects with appropriate constructors & display the FATHER & SON details.
6	Write a C++ program to define class name FATHER & SON that holds the income respectively. Calculate & display total income of a family using Friend function.
7	Write a C++ program to accept the student detail such as name & 3 different marks by get_data() method & display the name & average of marks using display() method. Define a friend function for calculating the average marks using the method mark_avg().
8	Write a C++ program to explain virtual function (Polymorphism) by creating a base class polygon which has virtual function areas two classes rectangle & triangle derived from polygon & they have area to calculate & return the area of rectangle & triangle respectively.
9	Design, develop and execute a program in C++ based on the following requirements: An EMPLOYEE class containing data members & members functions: i) Data members: employee number (an integer), Employee_ Name (a string of characters), Basic_ Salary (in integer), All_ Allowances (an integer), Net_Salary (an integer). (ii) Member functions: To read the data of an employee, to calculate Net_Salary & to print the values of all the data members. (All_Allowances = 123% of Basic, Income Tax (IT) =30% of gross salary (=basic_ Salary_All_Allowances_IT).
10	Write a C++ program with different class related through multiple inheritance & demonstrate the use of different access specified by means of members variables & members functions.

11	Write a C++ program to create three objects for a class named count object with data members such as roll_no & Name. Create a members function set_data ( ) for setting the data values & display ( ) member function to display which object has invoked it using „this" pointer.
12	Write a C++ program to implement exception handling with minimum 5 exceptions classes including two built in exceptions.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Write C++ program to solve simple and complex problems
2. Apply and implement major object-oriented concepts like message passing, function overloading, operator overloading and inheritance to solve real-world problems.
3. Use major C++ features such as Templates for data type independent designs and File I/O to deal with large data set.
4. Analyze, design and develop solutions to real-world problems applying OOP concepts of C++

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Object oriented programming in TURBO C++, Robert Lafore, Galgotia Publications, 2002
2. The Complete Reference C++, Herbert Schildt, 4th Edition, Tata McGraw Hill, 2003.
3. Object Oriented Programming with C++, E Balaguruswamy, 4th Edition, Tata McGraw Hill, 2006.

IV Semester

Octave / Scilab for Signals			
Course Code	**21ECT4093**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

1. **Preparation**: To prepare students with fundamental knowledge/ overview in the field of signals and processing.
2. **Core Competence**: To equip students with a basic foundation in electronic engineering and mathematics fundamentals required for comprehending the operation and application of signal processing.
3. **Professionalism & Learning Environment**: To inculcate in students an ethical and professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context, and life-long learning needed for a successful professional career.

Sl.No	Experiments
1	Verify the Sampling theorem.
2	Determine linear convolution, Circular convolution and Correlation of two given sequences. Verify the result using theoretical computations.
3	Determine the linear convolution of two given point sequences using FFT algorithm. Verify the result using theoretical computations.
4	Determine the correlation using FFT algorithm. Verify the result using theoretical computations.
5	Determine the spectrum of the given sequence using FFT. Verify the result using theoretical computations.
6	Design and test FIR filter using Windowing method (Hamming, Hanning and Rectangular window) for the given order and cut-off frequency.
7	Design and test IIR Butterworth 1^{st} and 2^{nd} order low & high pass filter.
8	Design and test IIR Chebyshev 1^{st} and 2^{nd} order low & high pass filter.
9	Generation of an AM – Suppressed Carrier Wave & visualization of the time domain and frequency domain plots.
10	Generation and visualization of standard test signals (both continuous and discrete time).
11	Generation and visualization of audio signal (pre-recorded) and generation of echo.
12	Generation and visualization of the STFT of a chirp (and other related) signal.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Demonstrate the DSP concepts on signal generation and sampling using Scilab/Octave
- Design and verify the computation of discrete signals using Scilab/Octave.
- Demonstrate and verify the application of FFT/DFT algorithm for a given signal using Scilab/Octave.
- Design and demonstrate programs to evaluate different types of low and high pass FIR filters using Scilab/Octave.
- Design, demonstrate and visualize different real world signals using Scilab/Octave programs.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.

Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.

Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).

Weightage to be given for neatness and submission of record/write-up on time.

Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.

In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

The suitable rubrics can be designed to evaluate each student's performance and learning ability.

Rubrics suggested in Annexure-II of Regulation book

The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

Digital Signal Processing Using MATLAB, John G Proakis and Vinay K Ingle, Cengage Learning, 2011

IV Semester

DAQ using LabVIEW			
Course Code	21ECT4094	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

- Process the knowledge of loop constructs.
- Fundamentals of graphical programming and use LabVIEW modules
- Implement 'Timing' functions.
- Input algebraic formulas via 'Formula Nodes' and 'Expression Nodes'.

Sl.No	Experiments
1	Data acquisition using LabVIEW for temperature measurement with thermocouple.
2	Data acquisition using LabVIEW for temperature measurement with AD590.
3	Data acquisition using LabVIEW for temperature measurement with RTD.
4	Data acquisition using LabVIEW for temperature measurement with Thermistor.
5	Creation of a CRO using LabVIEW and measurement of frequency and amplitude from external source.
6	Create function generator using LabVIEW and display the amplitude and frequency on CRO (externally connected)
7	Demonstrate amplitude modulation considering modulating and carrier wave from external source.
8	Interface LEDs to DAQ output and implement counter.
9	Data acquisition using LabVIEW for load / strain measurement using suitable transducers.
10	Demonstrate binary to grey code converter (& vice versa) using DAQ card.
11	Data acquisition using LabVIEW for distance/humidity measurement using suitable transducers.
12	Reading audio input with Microphones and output using DAQ card.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Build temperature indicating instruments using LabVIEW (NI DAQ)
2. Interface peripheral devices/instruments to LabVIEW
3. Build LabVIEW modules to sense and process audio inputs
4. Apply programming structures, data types, and the analysis and signal processing algorithms in LabVIEW
5. Debug and troubleshoot applications

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.

The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI, 2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGraw Hill, Second Edition, 2011.

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2020 Batch)

V Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	PC	18HS51	IPR	HS	03	--	--	03	050	050	100	03
2	PC	18EC51	Microprocessor and Microcontrollers	EC	04	--	--	04	050	050	100	03
3	PC	18EC52	Digital Signal Processing	EC	04	--	--	04	050	050	100	04
4	PC	18EC53	Digital Communication	EC	04	--	--	04	050	050	100	04
5	PC	18EC54	Object Oriented Programming with C++	EC	03	--	--	04	050	050	100	03
6	PE	18EC55X	Professional Elective-1	EC	03	--	--	03	050	050	100	03
7	OE	18EC56X	Open Elective A		03	--	--	03	050	050	100	03
8	PC	18ECL57	Microcontroller Laboratory	EC	--	--	02	02	050	050	100	01
9	PC	18ECL58	Digital Signal Processing Laboratory	EC	--	--	02	02	050	050	100	01
				Total	**24**	**00**	**04**	**29**	**450**	**400**	**900**	**25**

18EC55x_Professional Elective – 1		
Sl. No.	**Course Code**	**Course Title**
1	18EC551	Digital Switching System
2	18EC552	Python Programming
3	18EC553	Artificial Neural Networks
4	18EC554	Nanoelectronics
5	18EC555	Computer Organization and Architecture

Open Elective-A(OE-A)		
Sl. No.	**Course Code**	**Course Title**
1	18EC561	Real Time Operating System(CS,IS, EI, ML)
2	18EC562	Mechatronics (CS,IS, EI, ML, ME, IEM, EEE)
3	18EC563	Television Engineering (TE, EI, ML)
4	18EC564	Sensors (CS, IS, ML, TC)

BOS Chairman Dean(Academics) Principal

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2020 Batch)

VI Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing/ Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	PC	18HS61	Management and Entrepreneurship	EC	03	--	--	03	050	050	100	03
2	PC	18EC61	CMOS VLSI Design	EC	04	--	--	04	050	050	100	04
3	PC	18EC62	Embedded Systems	EC	03	--	--	03	050	050	100	03
4	PC	18EC63	Computer Communication Network	EC	04	--	--	04	050	050	100	04
5	PC	18EC64x	Professional Elective – 2	EC	03	--	--	03	050	050	100	03
6	OE	18EC65x	Open Elective –B	EC	03	--	--	03	050	050	100	03
7	PC	18ECL66	Embedded System Laboratory	EC	--	--	02	02	050	050	100	01
8	PC	18ECL67	VLSI Laboratory	EC	--	--	02	02	050	050	100	01
9	M	18ECM68	Mini Project					03	050	050	100	02
10	INT	18ECI69	Industry Internship	To be carried out during the intervening vacations of VI an VII semesters				--	--	--	--	--
			Total		**20**	**00**	**04**	**27**	**450**	**450**	**900**	**24**

18EC65x_Professional Elective – 2 (PECEL 2)		
Sl. No.	**Course Code**	**Course Title**
1	18EC641	Semiconductor Fabrication
2	18EC642	Cryptography
3	18EC643	Information Theory & Coding
4	18EC644	System Verilog for verification
5	18EC645	Internet of Things
6	18EC646	Autotronics and Vehicle Intelligence

Open Elective-B(OE-B)		
Sl. No.	**Course Code**	**Course Title**
1	18EC651	Automotive Electronics Engineering (CS, IS, EI, ET, ML, ME, IEM, EEE)
2	18EC652	Nano Electronics (CS,IS,ML,TC, ME)
3	18EC653	Wireless Sensor Networks(EE,ML,EI)
4	18EC654	Robotics and Machine vision systems(ME,EI,EE,ML,IEM)

Sub Title : Microprocessor and Microcontrollers		
Sub Code: 18EC51	**No. of Credits:4= 4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. To learn the architecture of 8086 microprocessor, 8051 microcontroller and MSP 430
2. To learn the memory organization of MCS51 and MSP 430. I/O ports and memory interfacing techniques with MCS51.
3. To learn the Instruction set of MCS51 and able to write the assembly language programs and c programs.
4. To learn the Timer/Counter, serial port configurations and able to write programs.
5. To learn the interrupts of MCS51 and MSP 430 able to Interface peripherals with MCS51.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction to microprocessors and microcontrollers:** RISC & CISC CPU Architectures, Harvard & Von- Neumann CPU architecture. **The 8086 Processors:** 8086 Architecture, CPU Architecture-BIU and EU, Register organization, Memory organization and segmentation, pin functions of 8086**.(TEXT 1 and TEXT 2)**	10	L1, L2, L3
2	**8051 Microcontroller:** The 8051 Architecture, Pin diagram of 8051, Memory organization, External Memory interfacing. Classification of Instruction, Addressing modes: Immediate addressing, Register addressing, Direct addressing, Indirect addressing, relative addressing, Absolute addressing, bit direct addressing. **8051 Instructions :** 8051 instructions, Data transfer instructions**.(TEXT 2)**	09	L1,L2,L3
3	**8051 Instructions and Programming:** Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instruction. 8051 programming: Assembler directives, Assembly language programs and Time delay calculations. Stack operations. Introduction to Embedded C, C data types, logical operations, programming 8051 using embedded C**.(TEXT 2 and TEXT 3**)	11	L1,L2,L3,L4
4	**Timers/counters:** 8051 timers/counters, programming 8051 timers in assembly and C. Data communication, Basics of Serial Data Communication, 8051 Serial Communication, Programming in assembly and C. **8051 interrupts and interfacing:** Interrupts and Basics of interrupts, 8051 Interfacing and Applications: Basics of I/O concepts, I/O Port Operation, Interfacing 8051 to DAC, interfacing of Keyboard. **(TEXT 3)**	12	L1,L2,L3,L4,L6
5	**MSP430 Architecture:** Introduction – Where does the MSP430 fit, The outside view, The inside view-Functional block diagram, Memory, Central Processing Unit, Memory Mapped Input and Output, Clock Generator, Exceptions: Interrupts and Resets, MSP430 family**.(TEXT 4)**	10	L1,L2,L3,L4,L6

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3.Unit 5 taught through Digital Learning.

Course Outcomes:

CO1. Understand the architecture and features of 8086 microprocessor, 8051 microcontrollers and MSP 430.
CO2. Understand the memory organization and memory mapping of MCS51 and MSP 430.
CO3. Understand the instruction sets of MCS51 and able to write Assembly and High-level Programs.
CO4. Explain the TIMER/COUNTER configuration able to implement by programs to generate time delay/counting.
CO5. Explain the Interrupt and serial communication and able to apply for real time applications.

Cos	**Mapping with POs**
CO1	PO1, PO5,PO6,PO7,PO8,PO12
CO2	PO1, PO2, PO3, PO5,PO6,PO8,PO9,PO12
CO3	PO1, PO2, PO3, PO5,PO6,PO8,PO9,PO12
CO4	PO1, PO2, PO3, PO5,PO6,PO8,PO9,PO12
CO5	PO1,PO2, PO3, PO5,PO6,PO7,PO8,PO11, PO12

Text Book:	
1.	**Yu-cheng Liu, Glenn A.Gibson,** "Microcomputer Systems: The 8086/8088 Family Architecture, Programming, and Design"
2.	**Kenneth J. Ayala,** "The 8051 Microcontroller Architecture, Programming & Applications", 2e Penram International, 1996 / Thomson Learning 2005.
3.	**Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay,** "The 8051 Microcontroller and Embedded Systems – using assembly and C", PHI, 2006 / Pearson, 2006.
4.	**John Davies,** "MSP430 Microcontroller Basics", Elsevier, 2010.

Reference Books:	
1.	**Doughlas V. Hall**, "Microprocessors and Interfacing Programming and Hardware".

Web Links:	
1.	"MCS51 Microcontroller family user's manual" "MSP430 Web material"**,** Texas Instruments, 2008.
2.	https://swayam.gov.in/nd1_noc20_cs25

Sub Title : Digital Signal Processing		
Sub Code: 18EC52	**No. of Credits:3=2 : 2 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE + Group Activity + Assignment + SEE =40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. To learn and understand sampling process, invertible systems, Discrete Fourier Transforms, Fast Fourier Transforms, IIR filters , FIR filters and their structures
2. To interpret the sampling process, Inverse Systems, DFT and their properties, FFT algorithms, IIR and FIR filters
3. To apply the concept of sampling theorem, DFT, FFT algorithms, IIR and FIR filters
4. To illustrate the DFT, FFT algorithms, IIR and FIR filters
5. To design the analog IIR, digital IIR and FIR filters

UNIT No	Syllabus Contents	No of Hours
1	**Sampling and Invertible systems:** Analog to digital conversion, Sampling of analog signals, Sampling theorem. Inverse systems and de-convolution, Invertibility of LTI systems, minimum phase, maximum phase and mixed phase systems. **TEXT 1 and TEXT 2**	10
2	**Discrete Fourier Transform (DFT) and its Properties:** Frequency domain sampling and reconstruction of discrete time signals: DFT and IDFT, Numerical examples. Properties of DFT: Periodicity, linearity, Symmetry properties, Circular folding, Circular Convolution, Circular time shift, Circular frequency shift, Complex conjugate property, Multiplication of two sequences, Use of DFT in linear filtering, overlap-save and overlap-add method. **TEXT 1 and TEXT 2**	10
3	**Fast-Fourier-Transform (FFT) Algorithms:** Direct computation of DFT, need for efficient computation of the DFT (FFT algorithms). Radix-2 FFT algorithm for the computation of DFT and IDFT: Decimation-in-time (DIT) and Decimation-in-frequency (DIF) algorithms. **TEXT 1**	11
4	**IIR Filter Design:** Characteristics of commonly used analog filters – Butterworth and Chebyshev filters, analog to analog frequency transformation. **Design of IIR Digital filters from analog filters (Butterworth and Chebyshev Type):** Impulse Invariance method and Bilinear transformation method, Derivation and design problems. **TEXT 1**	10
5	**FIR Filter Design:** Introduction to FIR filters, Design of FIR filters using Rectangular, Hamming and Hanning windows. **Implementation of Discrete-Time Systems:** Structures for IIR systems: Direct form I & II, Cascade & Parallel form realization. Structures for FIR systems: Direct form, Linear phase, Cascade form. **TEXT 1 and TEXT 2**	11

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2

Assignment - 2 from units 3, 4 and 5

Note 3.Unit 3 will be taught by online and digital platform

Course Outcomes:

CO1 Define the sampling process, invertible systems, Discrete Fourier Transforms, Fast Fourier Transforms, IIR and FIR filters and their structures

CO2 Understand sampling process, Inverse Systems, DFT and their properties, FFT algorithms and IIR and FIR filters.

CO3 Analyze DFT, FFT algorithms, IIR and FIR filters.

CO4 Apply the concept of sampling theorem, DFT, FFT algorithms, IIR and FIR filters.

CO5 Design the analog IIR, digital IIR and FIR filters.

Cos	Mapping with POs
CO1	PO1,PO8
CO2	PO2,PO6,PO7
CO3	PO4,PO7,PO8
CO4	PO5,PO6,PO8
CO5	PO3,PO10,PO12

Text Book:	
1.	**Proakis & Monalakis,** "Digital Signal Processing-Principles, Algorithms & Applications", Fourth Edition, Pearson Education, New Delhi, 2009
2.	**Emmanuel C Ifeachor and Barrie W Jervis,** "Digital Signal Processing: A Practical Approach", Second edition, Pearson Education, New Delhi, 2002

Reference Books:	
1.	**Alan V. Oppenheim and Schaffer**, "Discrete Time Signal Processing", 2nd edition, PHI, 2007
2.	**Sanjit K. Mitra,** "Digital Signal Processing", 3rd edition, Tata Mc-Graw Hill, 2010
3.	**Lee Tan**, "Digital Signal Processing", edition, Elsevier publications, 2007
4.	**Shenoy**, "Introduction to Digital Signal Processing and Filter Design", 1st edition, John Wiley & Sons, 2010
5.	**Lonnie C. Ludeman,** "Fundamentals of Digital Signal Processing", International edition, John Wiley & Sons, 1988

Web Links.

1 http://nptel.ac.in/courses/117102060/

2 https://ocw.mit.edu/resources/res-6-008-digital-signal-processing-spring-2011/study-materials/

Sub Title : DIGITAL COMMUNICATION		
Sub Code: 18EC53	**No. of Credits: 4 = 4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration: 3 Hours	**CIE +Assignment + SEE = 45 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. A brief overview of the digital communication system and the techniques of formatting the source signal.
2. Demonstrate key concepts like geometrical analysis of signals, probability of error, various receiver types in detection.
3. Understand and analyze different waveform coding techniques and applications and spread spectrum modulation.
4. Understand information on discrete PAM signals, ISI and adaptive equalization for data transmission.
5. Analyze and design of digital modulation techniques and performance analysis based on probability of error.

UNIT No	**Syllabus Contents**	**No of Hours**	**Blooms Taxonomy level.**
1	Introduction: Sources and signals, Basic signal processing operations in digital communications, Channels for digital communication. Detection and Estimation: Model of Digital communication system, Gram-Schmidt Orthogonalization Procedure, geometric interpretation of signals, response of bank of correlators to noisy input, Detection of known signals in noise, probability of error, correlation receiver, matched filter receiver. Text 1, Text 2 and Text 3	13	L1, L2, L3.L4
2	Sampling Process: Sampling Theorem, signal space interpretation, Quadrature sampling of Band pass signal, PAM, TDM. Waveform Coding Techniques: Pulse Code Modulation, channel noise and error probability, Quantization noise and Signal to Noise Ratio, robust quantization, DPCM, DM Text 1 & Text 2	12	L3,L4,L5
3	Base-Band Shaping for Data Transmission: Discrete PAM signals, power spectra of discrete PAM signals, Inter Symbol Interference, Nyquist's criterion for distortion less base-band binary transmission, correlative coding, eye pattern. Text 1 &Text 2	09	L3,L4
4	Digital Modulation Techniques: Digital Modulation formats. Coherent binary modulation techniques: Binary ASK, PSK, and FSK. Coherent Quadrature modulation techniques: Quadriphase-shift keying (QPSK). Non-coherent binary modulation techniques:	09	L2,L3, L4,L5

	Differential phase shift keying (DPSK). Text 1 &Text 2		
5	Spread Spectrum Modulation: Pseudo noise sequences, notion of spread spectrum, Principle of Direct Sequence Spread Spectrum (DSSS), frequency hop spread spectrum. Multiplexing and Multiple Access: FDMA, TDMA, CDMA and SDMA Text 1 & Text 3	09	L1,L2,L3

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1. Able to understand the System approach to Digital communication right at the foundation level and various basic signal processing operations involved.

CO2. Gain the knowledge on the key concepts such as signal space concepts, probability of error, and analyse the detection of signals using correlation receiver and matched filter.

CO3. Gain the knowledge on the sampling process, waveform coding techniques and quantization techniques to improve performance of the digital communication system.

CO4. Capable of analysing Discrete PAM signals and its power spectra and knowledge on to ISI and measures to counter ISI problem using raised cosine filter and correlative coding methods.

CO5. Able to describe the spread spectrum type of communication along with its advantages and know briefly the various multiple access techniques compare them.

Cos	**Mapping with POs**	**Mapping with PSOs**
CO1	PO1,PO2,PO4,PO6	PSO1,PSO2,PS03
CO2	PO1,PO2, PO6	PSO1,PSO2,PS03
CO3	PO1,PO2,PO4,PO6	PSO1,PSO2, PS03
CO4	PO1,PO2PO3,PO4,PO5,PO6	PSO1,PSO2, PS03
CO5	PO1,PO2PO3,PO4,PO5,PO6	PSO1,PSO2,PS03

Text Book:	
1.	Simon Haykins, “Digital Communications”, 4th Edition, John Wiley, 2008(reprint).
2.	Dr. K. N. Hari Bhat & Dr. D. Ganesh Rao, ”Digital communications”, 2nd Edition, Sanguine technical publications, 2008. (Reprint).
3.	Bernard Sklar,” Digital communications”, 3rd Edition, Pearson education, 2007

Reference Books:	
1.	K.Sam Shanmugam, “Digital and analog communication systems”,4th Edition, John Wiley, 1996.
2.	John Proakis, Masoud Salehi,” Digital communications”, 5th Edition, Mac Graw Hill, 2008.
3.	Barry, John R., Lee, Edward A., Messerschmitt, David G,” Digital communications”, 3rd Edition, Springer, 2004
4.	B. P. Lathi, Zhi Ding, “Modern Digital and Analog Communication Systems”, 4th Edition, Oxford, 2009.

Web Links:	
1.	1 http://nptel.ac.in/ online course /Digital Communication
2.	https://lecturenotes.in/subject/45/digital-communication-techniques-dct
3.	https://mrcet.com/downloads/digital_notes/ECE/III%20Year/DIGITAL%20COMMUNICATIONS.pdf

Sub Title : Object Oriented Programming with C++		
Sub Code: 18EC54	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE =40+ 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Listing OOPs concepts and recognizing the programming elements.
2. Developing and managing the object oriented programs.
3. Understanding the concepts of OOPS to develop the robust programs.
4. Understand and manage the error handling.
5. Understand Pointers

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Beginning with C++:** Basic concepts of object oriented programming, structure of C++ program, basic data types, user defined data types, derived data types, reference variables, operators in C++, scope resolution operator, memory management operators, manipulators, implicit conversions and control structures. **Functions in C++:** The main function, function prototyping, call by reference, return by reference, inline function, default arguments, const arguments, recursion, function overloading, Friend and virtual Functions **TEXT-1**	08	L1, L2, L3
2	**Classes and Objects*:*** C structures revisited, Specifying a class, Defining member function, A C++ program with class, making outside function inline, Nesting of member functions, private member function, Arrays with in a class, Memory allocation for the objects, static data members, static member functions, Array of objects, objects as function argument, Friend function, returning an object **TEXT 1**	06	L1,L2,L3
3	**Constructors and Destructors:** Constructors, Parameterized constructors, multiple constructors in a class, Constructors with default arguments, Dynamic initialization of objects, copy constructor, destructors. **Operator overloading:** Overloading of unary operators and overloading of Binary operators, overloading binary operators using friends**. TEXT 1**	09	L1,L2,L3,L4
4	**Inheritance:** Introduction, Defining derived classes, single inheritance, Making private function inheritable, multilevel inheritance, multiple inheritance, Hierarchical inheritance, Hybrid inheritance, virtual base class, abstract class **TEXT 1**	06	L1,L2,L3,L4
5	**Exception Handling:** Introduction, basics of exception handling, Exception handling mechanisms, throwing mechanisms, catching mechanisms, Rethrowing an exception, specifying Exceptions,	10	L1,L2,L3,L4

	Exceptions in constructors and destructors. **Pointers, virtual functions and polymorphisms:** Introduction, pointers, pointers to objects, this pointer, pointers to derived classes, virtual functions, pure virtual functions, virtual constructors and destructors. **TEXT 1**		

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.
Note 2.Each Unit will have assignments that are evaluated for 5 marks.
Note 3.Unit 5 taught through Digital Learning.

Course Outcomes:

CO1. To gain the knowledge of object oriented concepts and get familiarized with basic concepts of programming.
CO2. Ability to design the programs using the classes and managing the objects.
CO3. Ability to design the programs with features of extensibility and use many operators.
CO4. Ability to develop the programs with reusability
CO5. Ability to develop the programs with built in error handling and use of pointers in the program

Cos	Mapping with POs
CO1	PO6
CO2	PO6
CO3	PO6
CO4	PO6, PO12
CO5	PO6, PO12

Text Book:	
1.	**E. Balaguruswamy**," Object Oriented Programming with C++", fifth edition, Tata McGraw Hill, 2012.

Reference Books:	
1.	**Stanley B.Lippmann, JoseeLajore**, "C++ Primer", 4th Edition, Addison Wesley, 2005.
2.	**Paul J Deitel, Harvey M Deitel**, "C++ for Programmers", edition, Pearson Education, 2009.
3.	**Herbert Schildt,** "The Complete Reference C++", 4th Edition, Tata McGraw Hill, 2003.

Web Links:	
1.	.https://www.tutorialspoint.com/cplusplus/cpp_object_oriented.htm
2.	.https://www3.ntu.edu.sg/home/ehchua/programming/cpp/cp3_OOP.html
3.	http://www.josuttis.com/cppbook/code.html

Sub Title : DIGITAL SWITCHING SYSTEM

Sub Title: Digital Switching System		
Sub Code: 18EC551	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Analyze basic switching techniques used in telephone system.
2. Analyze the different types of calls in DSS
3. Analyze time division and space division switching techniques and integrate both to improve Performance the course learning objective
4. Analyze different signaling techniques associated with telephone network.
5. Analyze switching networks with various techniques

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**DEVELOPMENTS OF TELECOMMUNICATIONS**: Network structure, Network services, terminology, Regulation, Standards, telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM . **EVOLUTION OF SWITCHING SYSTEMS:** Message switching, Circuit switching, Functions of switching systems, distributed frames, crossbar systems Electronic switching. (TEXT 1 and TEXT 2)	8	L1,L2,L3.
2	**TELECOMMUNICATION TRAFFIC:** Unit of traffic, Congestion, Traffic measurement, Mathematical model, lost call systems, Queuing systems. **SWITCHING SYSTEMS FUNDAMENTALS** : Introduction Purpose of analysis, Basic central office linkages, Outside plant versus inside plant, Switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems DSS fundamentals Building blocks of a digital switching system, (TEXT 1 and TEXT 2)	8	L1,L2,L3.
3	**COMMUNICATION AND CONTROL:** Introduction scope Switching communication and control Basic functions of interface controller Basic functions of network control processor Basic functions of central processor call processing. **SWITCHING SYSTEM SOFTWARE**: Introduction, Scope, Basic software architecture, Call models, Software linkages during call. (TEXT 1 and TEXT 2)	8	L1,L2,L3.
4	**A GENERIC DIGITAL SWITCHING SYSTEM MODEL:** Introduction, Scope, Hardware and Software architecture, Simple call through a digital system, Common characteristics of digital switching systems Analysis Report. TEXT 2	7	L1,L2,L3.

5	**MAINTENANCE OF DIGITAL SWITCHING SYSTEM:** : Introduction, Scope, Software maintenance, Interface of a typical digital switching system central office, System outage and its impact on digital switching system reliability, Impact of software patches on digital switching system maintainability, methodology for reporting and correction of field problems Upgrade process success rate, Number of patches applied per year, Diagnostic resolution rate, Reported critical and major faults corrected, A strategy improving software quality. **ANALYSIS OF NETWORKED SWITCHING SYSTEMS :**Scope Switching in networked environment, network reliability requirements, current trends in DSS, future trends in DSS (TEXT 2)	8	L1,L2,L3

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3. Unit 4 – Digital Teaching and Learning.

Course Outcomes:

CO1 Demonstrate the understanding of basic fundamentals of a telecommunication and switching system.

CO2 Ability to Analyze traffic management and switching system.

CO3 Ability to describe the common switching & control techniques and switching system software.

CO4 Ability to describe the maintenance of digital switching systems and its controlling.

CO5 Ability to analyze the various types of connection and switching links used by industry for telecommunication system worldwide and recent and future trends in DSS

Cos	**Mapping with POs**	**Mapping with PSOs**
CO1	PO2,PO5,PO6,PO7,PO8,PO9,PO11,PO12	PSO1,PSO2,PS03
CO2	PO2,PO3,PO4, O5,PO6,PO7,PO8,PO9,PO11,PO12	PSO1,PSO2,PS03
CO3	PO2,PO3,PO4,PO6,PO7, PO8,PO9,PO11,PO12	PSO1,PSO2, PS03
CO4	PO4,PO6,PO7, PO8,PO9,PO11,PO12	PSO1,PSO2, PS03
CO5	PO3,PO4,PO6,PO7, PO8,PO9,PO11,PO12	PSO1,PSO2,PS03

Text Book:

1. **J E flood,** "Telecommunication Systems",", First Edition, Pearson Education, 2002
2. **Syed R Ali,** "Digital Switching Systems, edition, publisher, 2002

Reference Books:

1. **John C Bellamy ,** "Digital Telephony", 3rd , Wiley India, 2000
2. **A.Bar-Lev**, "Semiconductor and Electronic Devices", 3rd edition, PHI, 1993

Web Links:	
1.	1 http://nptel.ac.in/ online course /digital switching systems
2.	https://books.google.co.in/books/about/Digital_Switching_Systems K Chandrashekar''Digital Switching Systems
3.	https://www.youtube.com/watch?v=oOMlwW4rBz8/jeflood

Sub Title: Programming with Python		
Sub Code:18EC552	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 03**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understanding the basics and data structure- list, tuples, dictionaries
2. To understand the control flow, functions modules and error handling.
3. To understand the object oriented concepts in python.
4. To get familiarised with the concepts of decorators and regular expressions.
5. To work with files and data structures in python.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**Introduction:** Basics of Python Programming, Using the REPL(Shell), Running Python Scripts, Variables, Assignment, Keywords, Input- Output, Indentation. Data Types - Integers, Strings, Booleans **Operators and Expressions:** Operators- Arithmetic Operators, Relational Operators, Assignment Operators, Logical Operators, Bitwise Operators, Membership Operators, Identity Operators, Expressions and order of evaluations. **Data Structures:** Strings**,** Lists, Tuples, Dictionaries Tuple and Sets **Text1, Text2**	08	L1, L2, L3
2	**Control Flow** - if, if-elif-else, for, while, break, continue, pass. **Functions** - Defining Functions, Calling Functions, Passing Arguments, Keyword Arguments, Default Arguments, Variable-length arguments, Anonymous Functions, Fruitful Functions. **Modules**: Creating modules, import statement, from .import statement, name spacing**,** Programming Examples **Text1, Text2**	08	L1, L2, L3
3	**Object Oriented Programming in Python**: Creating a class, The Self Variable, Namespaces, Types of Methods, Inner classes Inheritance and Polymorphism: Constructors in Inheritance, The Super() Method, Types of Inheritance: Single/Multiple, Method Resolution order, Polymorphism, Operator Overloading, Method overloading, Method Overriding. Programming Examples **Text1**	08	L1, L2, L3
4	**Files in Python**: Types of files, Working with Text files, Working with Binary Files, Pickle Module, reading and writing CSV files. **Data Structures in Python**: Linked Lists, Stacks, Queues, Deques. Programming Examples **Text1, Text2**	07	L1, L2, L3

5	**Decorators:** Introduction, Decorating functions with Parameters, Chaining decorators in python, property decorator: Class without getters and setters, Class with getters and setters **Regular Expressions**: Using special characters, Regular expression methods, Named groups in Python Regular expression, Regular expression in glob module, Programming Examples **Text1, Text2**	08	L1, L2, L3

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5
3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 1 - Digital teaching and learning

Course Outcomes

CO1. Demonstrate the understanding and usage of core python scripting elements, python constructs, data types, lists, tuples and dictionaries

CO2. Demonstrate the understanding and usage of control structures module and exception handling

CO3. Demonstrate usage of object oriented features such as Inheritance, Polymorphism, operator overloading

CO4. Apply the knowledge of python and use the language scripting elements and constructs to develop file handling and build the data structures

CO5. Apply the concept of decorators and regular expressions.

COs	Mapping with POs
CO1	PO5,PO6
CO2	PO5,PO6
CO3	PO5,PO6,PO7,PO8,PO9
CO4	PO5,PO6,PO7,PO8,PO9
CO5	PO5,PO6,PO7,PO8,PO9

TEXT BOOKS:

1. Core Python Programming: Dr.R.Nageshwara Rao, Dream Tech Press 2018

REFERENCE BOOKS/WEB LINKS:

1. Think Python, Allen Downey, Green Tea Press.
2. Core Python Programming, W.Chun, Pearson.
3. Introduction to Python, Kenneth A. Lambert, Cengage.
4. Learning Python, Mark Lutz, Orielly

EBOOKS:

1. http://greenteapress.com/wp/think- python
2. https://www.programiz.com/python-programming/decorator
3. https://www.programiz.com/python-programming/property

Sub Title : ARTIFICIAL NEURAL NETWORK		
Sub Code:18EC553	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To understand the Analysis of different techniques and algorithms in Neural Networks.
2. To study the concepts of setting parameters and multilayered Networks.
3. To understand the concepts of Prediction, Polynomial Neural Networks.
4. To analyze the Optimization techniques in Neural Networks
5. To enable the student to apply these technique in real life applications which involve neural models.

UNIT No	Syllabus Content	No of Hours	Bloom's Taxonomy
1	Introduction, Fundamental concepts and models of Artificial Neural Network, Biological Neural Networks, structure and function of single neuron, neural network architectures, modelling of neural network, benefits of neural networks. Learning process. Supervised learning and Un-supervised learning.	08	L1, L2, L3
2	Supervised Learning for single layer network: Perceptron, linear separability, Perceptron Training Algorithm, Delta rule, guarantees of success, modifications. Supervised Learning for Multi- layer network: multilevel discrimination, preliminaries, Back propagation, setting parameter values, theoretical results.	09	L1, L2, L3
3	Prediction networks: Introduction, Recurrent network, William's and Zipser's Algorithm, Radial Basis Functions, Polynomial networks, Higher order network, Sigma–pi network, Function link architecture,Pi-sigma network, Regularization	08	L1, L2, L3
4	Unsupervised learning: Winner take all networks. Hamming networks, Maxnet, Simple competitive learning, Hebb rule, Optimization Methods: Hop filed networks, Travelling Sales person problem, Solving simultaneous Liner equations, Allocating documents to multiprocessors, Iterated Gradient Descent	08	L1, L2, L3
5	Case studies on neural network modelling: Application of MATLAB in Neural Network, UC Irvine Machine Learning Repository	06	L4,L5

Note 1: All Units will have internal choice.

Note 2: Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2. Assignment - 2 from units 3, 4 and 5.

Note 3 : Digital learning – Unit 05

Course Outcomes:

CO1. Understand the basic concepts of Neural Networks.
CO2. Analysis and development of different techniques in neural networks.
CO3. Analysis the concepts of Prediction Networks and Polynomial networks in Artificial.
CO4. Use different optimization, machine learning technique for different model and enveloping the application.
CO5. Analyze and design a real world problem for implementation and understand the dynamic behavior of a system.

Cos	Mapping with POs
CO1	P01,P02,P05,PO6
CO2	P02,P07
CO3	P08,P09
CO4	P09,P10
CO5	P05,P07,P09

TEXT BOOKS:

1. Kishan Mehrotra, C. K. Mohan, Sanjay Ranka,Penram, **"Elements of Artificial Neural Networks"**, ***1997.***
2. J. Zurada, Jaico, **"Introduction to Artificial Neural Systems"**, ***2003.***

REFERENCE BOOKS/WEBLINKS:

1. Simon Hayking, **"Neural Networks: A Comprehensive Foundation",**2nd Edition, PHI.
2. Laurene Fausett, **"Fundamentals of Neural Networks: Architecture, Algorithms and Applications",** Person Education, 2004.

Sub Title : NANOELECTRONICS		
Sub Code: 18EC554	**No. of Credits:3=3: 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Enhance basic engineering science and technical knowledge of Nanoelectronics.
2. Explain basics of top-down and bottom-up fabrication process, devices and systems.
3. Describe technologies involved in modern day electronic devices.
4. Know various nanostructures of carbon and the nature of the carbon bond itself.
5. Learn the photo physical properties of sensor used in generating a signal.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction** Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction. Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials. **(Text 1)**	08	L1,L2
2	**Inorganic semiconductor nanostructures** Overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super lattices, band offsets, and electronic density of states. **(Text 1).**	08	L1, L2
3	**Physical processes** Modulation doping, quantum hall effect, resonant tunnelling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural. **(Text 1).**	07	L1,L2
4	**Carbon Nanostructures** Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. **(Text 2).**	08	L1,L2
5	**Applications:** Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS **(Text 1)**	08	L1,L2

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3.Unit 5---digital teaching and learning.

Course Outcomes:

CO1. Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
CO2. Know the properties of carbon and carbon nanotubes and its applications.
CO3. Apply the knowledge to prepare and characterize nanomaterials.
CO4. Apply the knowledge to prepare and characterize nanomaterials.
CO5. Analyse the process flow required to fabricate state-of-the-art transistor technology.

Cos	Mapping with POs
CO1	PO1,PO2,PO3,PO5
CO2	PO1,PO2,PO3
CO3	PO1,PO2,PO3
CO4	PO1,PO2,PO3
CO5	PO1,PO2,PO5

Text Book:	
1.	**Ed Robert Kelsall, Ian Hamley, Mark Geoghegan**, "Nanoscale Science and Technology", John Wiley, 2007.
2.	**Charles P Poole, Jr, Frank J Owens**, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.

Reference Books:	
1.	**Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate**, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.
2.	T Pradeep, "Nano: The essentials-Understanding Nanoscience and Nanotechnology", TMH

Web Links:	
1.	https://www.youtube.com/watch?v=w8Dq8blTmSA
2.	http://nptel.ac.in

Sub Title : Computer Organization and Architecture		
Sub Code: 18EC555	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand the meaning of basic structure of computers, and machine instructions and programs.
2. Analyze addressing modes and assembly language.
3. Compute the quantitative parameters for functions of input and output organization.
4. Associate the concepts of memory system

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Basic Structure of Computers:** Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance – Processor Clock, Basic Performance Equation (upto 1.6.2 of Chap 1 of Text). **Machine Instructions and Programs**: Numbers, Arithmetic Operations and Characters, IEEE standard for Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing, (upto 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text).	08	L1, L2, L3
2	Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions (from 2.4.7 of Chap 2, except 2.9.3, 2.11 & 2.12 of text).	08	L1,L2,L3,L4
3	**Input/Output Organization:** Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access, (upto 4.2.4 and 4.4 except 4.4.1 of Chap 4 of text).	08	L2,L3,L4
4	**Memory System:** Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage-Magnetic Hard Disks (5.1, 5.2, 5.2.1, 5.2.2, 5.2.3, 5.3, 5.5 (except 5.5.1 to 5.5.4), 5.7 (except 5.7.1), 5.9, 5.9.1 of Chap 5 of Text).	08	L1,L2,L3
5	**Basic Processing Unit:** Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Microprogrammed Control (upto 7.5 except 7.5.1 to 7.5.6 of Chap 7 of Text).	07	L1,L2,L3

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Each Unit will have assignments that are evaluated for 5 marks.

Note 3.Unit 5 will be taught online.

Course Outcomes:

CO1. Associate the concepts of structure of computer, the machine instruction and programs
CO2. Analyse and addressing modes.
CO3. Demonstrate the input/output organization
CO4. Demonstrate the memory system
CO5. Analyse the Basic Processing Unit.

Cos	Mapping with POs
CO1	PO1,PO2,PO3,PO5
CO2	PO1,PO2,PO5,PO6
CO3	PO1,PO2,PO3
CO4	PO1,PO2,PO3
CO5	PO1,PO2,PO5

Text Book:	
1.	**Carl Hamacher, Zvonko Vranesic, Safwat Zaky** " Computer Organization", 5th Edition, Tata McGraw Hill, 2002.

Reference Books:	
1.	**David A. Patterson, John L. Hennessy** "Computer Organization and Design – The Hardware / Software Interface", ARM Edition, 4th Edition, Elsevier, 2009.
2.	**William Stallings** "Computer Organization & Architecture", 7th Edition, PHI, 2006.
3.	**Vincent P. Heuring & Harry F. Jordan** "Computer Systems Design and Architecture", 2nd Edition, Pearson Education, 2004.

Web Links:	
1.	https://mrcet.com/downloads/digital_notes/IT/COMPUTER%20ORGANIZATION%20(R17A0510).pdf
2.	https://swayam.gov.in/nd1_noc20_cs25

Sub Title: BIO-MECHATRONICS DEVICES		
Sub Code:18EC556	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Learn basic knowledge about Bio mechanics, Bio sensors and actuators, and bio- mechatronics devices.
2. Impart the bio assist devices.
3. Know the different types, bio imaging and processing.
4. Understand about bio mechatronics devices and their functions.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**Bio Mechanics :** Cardiovascular biomechanics, Musculoskeletal and orthopedic biomechanics, human ergonomic, Rehabilitation **Text1**	08	L1, L2
2	**Bio Sensors and Actuators :** Introduction to Bio mechatronics, Electrodes - Types, - Measurement of blood pressure - Blood Gas analyzers: pH of blood, Smart actuators for biological applications **Text1**	08	L1, L2
3	**Medical Measurements:** Heart rate - Heart sound -Pulmonary function measurements -spirometer -finger-tip oximeter - ESR, GSR measurements **Text1**	08	L1, L2, L3
4	**Wearable mechatronics devices:** Wearable Artificial Kidney, Wireless capsule endoscope, Wearable Exoskeletal rehabilitation system, Wearable hand rehabilitation **Text1**	07	L1, L2, L3
5	**Sensory Assist Devices:** Hearing aids – Implants, Optical Prosthetics, Visual Neuroprostheses – Sonar based systems, Respiratory aids, Tactile devices for visually challenged. **Text1**	08	L1, L2, L3

Note:

1. **Unit 1,2,3,4, and Unit 5 will have the internal choice**
2. **Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5**
3. **Group activity for a group of 4 or 5 students -5 marks**
4. **UNIT 1 - Digital teaching and learning**

Course Outcomes

CO1. Demonstrate the basic knowledge about the Bio mechanics, Bio sensors and actuators, and bio- mechatronics devices.

CO2. Acquire the different bio imaging and processing.

CO3. Analyse the Signal processing with bio sensors and actuators.

CO4. Analyse modern medical measurement devices.

CO5. Understand the properties of bio assist devices.

COs	**Mapping with POs**
CO1	PO5,PO6
CO2	PO5,PO6
CO3	PO5,PO6,PO7,PO8,PO9
CO4	PO5,PO6,PO7,PO8,PO9
CO5	PO5,PO6,PO7,PO8,PO9

TEXT BOOKS:

1. Graham M. Brooker, "Introduction to Bio-Mechatronics", Sci Tech Publishing, 2012.

REFERENCE BOOKS/WEB LINKS:

1. Leslie Cromwell, Fred J. Weibell, Erich A. Pfeiffer, "Bio-Medical Instrumentation and Measurements", II edition, Pearson Education, 2009.
2. Raymond Tong Kaiyu . "Bio-mechatronics in Medicine and Healthcare" Pan Stanford Publishing, CRC Press, 2011

Sub Title : **Real Time Operating System**		
Sub Code: 18EC561	**No. of Credits:3=3: 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. study the basic concepts of specialized processors
2. study the various Scheduling strategies
3. study multi-resource services
4. study the embedded system components
5. understand design trade-offs

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction to real-time embedded systems:** Brief history of real time systems, a brief history of embedded systems. **System Resources:** resource analysis, real-time service utility, scheduling classes, the cyclic executive, scheduler concepts, preemptive fixed priority scheduling policies, Real-Time OS, thread safe reentrant functions. Text1	08	L1,L2
2	**Processing**: preemptive fixed-priority policy, feasibility, rate monotonic least upper bound, necessary and sufficient feasibility, deadline – monotonic policy, dynamic priority policies. **I/O Resources**: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture. Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems. Text1	08	L1, L2, L3
3	**Multi-resource Services**: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion. Soft Real-Time Services: Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services. Text1	08	L1, L2
4	**Embedded system components**: firmware components, RTOS system software mechanisms, software application components. **Debugging components:** exceptions assert, checking return codes, single-step debugging, kernel scheduler traces, test access ports, trace ports, power-on self test and diagnostics, external test equipment, application-level debugging. Text1	08	L1, L2
5	**High availability and reliability design:** reliability and availability, similarities and differences, reliability, reliable software, available software, design trade- offs, hierarchical applications for fail-safe design. Text1	07	L1, L2

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3.Unit 4---digital teaching and learning.

Course Outcomes:

CO1: Understand the basics of Real Time Embedded System and System Resources

CO2: Analyse the concepts Processing and IO Resources

CO3: Analyse Various multi-resource services

CO4: Analyse different Embedded System Components and Debug components.

CO5: Analyze and Categorize the design trade-offs

Cos	Mapping with POs
CO1	PO1, PO2
CO2	PO2, PO6
CO3	PO2,PO6, PO10,P12
CO4	PO2,PO6, PO10,P12
CO5	PO2,PO6, PO10,P12

Text Book:	
1.	Sam Siewert, "**Real-Time Embedded Systems and Components**," Cengage Learning India Edition, **2007**.
2.	John Wiley, **"Programming for Embedded Systems"**, Dreamtech SoftwareTeam, India Pvt. Ltd.,2008.

Reference Books:	
1.	Raj Kamal, "**Embedded Systems**", Tata McGraw Hill, New Delhi, ***2008***.
2.	Phillip. A. Laplante, "**Real-Time Systems Design and Analysis**", Prentice Hall India,2nd Edition, ***2005***.
3	Jane. W. S. Liu, "**Real Time Systems**", Pearson Education, ***2005***

Sub Title : **MECHATRONICS**		
Sub Code: 18EC562	**No. of Credits:3=3: 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand various elements of a mechatronics system and how they integrate
2. Understand the concept of signal conditioning and signal processing
3. Know the various components of microprocessor and micro controller.
4. Know the working of sensors and actuator systems.
5. Learn how different types of electrical and mechanical systems are used for various practical applications.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**INTRODUCTION:** Evolution, Components of Mechatronics system, Measurement systems, Control systems-open loop and closed loop systems, Applications of Mechatronics system. **BASIC SYSTEM MODELS:** Basic concepts of mechanical, electrical, fluid and thermal systems building blocks. *TEXT 1 .TEXT 2*	08	L1,L2,L3.
2	**INTRODUCTION TO DIGITAL LOGIC:** Logic gates, Half and Full adders, Boolean Algebra, simple applications of logic gates, Sequential logic, Introduction to Flip-flops and counters. **MICROPROCESSORS AND MICROCONTROLLERS OVERVIEW:** Structure of microcomputer, block diagram of microprocessor and microcontroller, Applications of Microprocessor control: temperature monitoring system, Washing machine system. *TEXT 1 TEXT 2*	08	L1,L2,L3
3	**SIGNAL CONDITIONING**: Introduction, Analog signal processing; Operational amplifiers (no analytical treatment). **NOISE REDUCTION AND FILTERING:** Passive and Active filters, ADC, DAC, and Data acquisition. *TEXT 1 TEXT 2*	08	L1,L2,L3
4	**TRANSDUCERS AND SENSORS:** - Classification of Transducer, classification of sensors, Resistance Thermometers, LVDT, Light sensors, Proximity Sensors. **ELECTRICAL ACTUATING SYSTEM:** Relays, Types of DC motors, AC motors, Stepper motor. *TEXT 3 TEXT 2 TEXT 1.*	08	L1,L2,L3,L4
5	**DESIGN OF MECHATRONIC SYSTEM:** Mechatronics design elements, Embedded systems, MEMS, Engine management system, Automatic camera, washing machine and temperature control system. *TEXT 1 TEXT 2.*	07	L1,L2,L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1: Understand the basic elements and building blocks of Mechatronics system.

CO2: Make use of the functions of various signal conditioning and processing devices

CO3: Choose various combinational and sequential circuits for various applications

CO4: Identify and Make use of various sensors and actuation systems

CO5: Take part in design of the Mechatronics system.

Cos	Mapping with POs
CO1	PO1, PO6, PO11, PO12
CO2	PO1, PO2, PO5, PO11, PO12
CO3	PO1, PO2, PO4, PO11, PO12
CO4	PO1, PO2, PO5, PO11, PO12
CO5	PO1, PO2, PO4, PO11, PO12

Text Book:	
1.	Bolton W **Mechatronics-Electronics Control Systems in Mechanical and Electrical Engineering,** 4th edition, Pearson Education press, 2010
2.	R.K Rajput, **"A text book of Mechatronics"**, 1st edition, S. Chand and Company Ltd., 2007
3.	Dr. H.D. Ramachandra, ***"Mechatronics and Microprocessors"*** reprint edition 2014.

Reference Books:	
1.	K. P. Ramachandran, "Mechatronics-Integrated mechanical electronics system" 1st Edition, Wiley India Pvt, Ltd, 2008
2.	Histand B,H Alciatore D.G., "Introduction to Mechatronics and Measurement systems", 3rd Edition, Tata McGraw Hill publishing Company Ltd,, 2007.

Web Links.

1. http://mechatronics.colostate.edu/
2. http://nptel.ac.in/courses/112103174/
3. http://nptel.ac.in/courses/Webcourse-contents/IIT KANPUR/microcontrollers/micro/ui/Course_home1_1.htm

Sub Title: Digital Television Engineering		
Sub Code: 18EC563	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration: 3 Hrs	**CIE +Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To learn and understand basic and advance Digital TV transmission standards.
2. To learn channel coding and modulation techniques for Digital TV
3. To identify RF amplifiers
4. To identify transmission lines and antennas suitable for Digital TV
5. Test a Digital TV Transmitter and Receiver

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level
1	Digital Television Transmission Standards ATSC terrestrial transmission standard, vestigial sideband modulation, DVB-T transmission standard. Performance Objectives for Digital Television: System noise, external noise sources, transmission errors, error vector magnitude, eye pattern, interference, cochannel interference, adjacent channel interference, analog to digital TV, transmitter requirements. **Text1**	7	L1,L2
2	Channel Coding and Modulation for Digital Television: Data synchronization, randomization/scrambling, forward error correction, interleaving, inner code, frame sync insertion, quadrature modulation, 8 VSB, bandwidth, error rate, COFDM, flexibility, bandwidth. **Text1**	8	L1,L2,L3
3	Transmitters for Digital Television: Precorrection and equalization, up conversion, precise frequency control, RF amplifiers, solid-state transmitters, RF amplifier modules, power supplies, power combiners, Wilkinson combiner, ring combiner, starpoint combiner, cooling, automatic gain or level control, ac distribution, transmitter control, tube transmitters, tube or solid-state transmitters, performance quality, retrofit of analog transmitters for DTV Radio-Frequency Systems for Digital Television: Constant-impedance filter, output filters, elliptic function filters, cavities, channel combiners. **Text1**	8	L1,L2,L3
4	Transmission Line for Digital Television: Fundamental parameters, efficiency, effect of VSWR, system AERP, rigid coaxial transmission lines, dissipation, attenuation, and power handling, higher order modes, peak power rating, frequency response, standard lengths, corrugated coaxial cables, wind load, waveguide, bandwidth, waveguide attenuation, power rating, frequency response, size trade-offs, waveguide or coax pressurization Transmitting Antennas for Digital Television : Antenna patterns, elevation pattern, mechanical stability, null fill, azimuth pattern, slotted cylinder antennas, gain and directivity, power handling, antenna impedance, bandwidth and	9	L2,L3

	frequency response, multiple-channel operation, types of digital television broadcast antennas, antenna mounting. **Text1**		
5	Test and Measurement for Digital Television: Power measurements, average power measurement, calorimetry, power meters, peak power measurement, measurement uncertainty, testing digital television transmitters. **Text1**	7	L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1. Compare Digital TV transmission standards and performance parameters.
CO2. Understand channel coding and modulation techniques for Digital TV.
CO3. Analyze RF amplifiers, modules and systems for Digital TV.
CO4. Identify Transmission lines and antennas suitable for Digital TV.
CO5. Test a Digital TV Transmitter and receiver

Cos	**Mapping with Pos**
CO1	PO1,PO5,PO6
CO2	PO2,PO5
CO3	PO2,PO5
CO4	PO5,PO6
CO5	PO2,PO5,PO7

Text Book:

1.	**R. R. Gulati,** Modern Television Practice, Principles, Technology and servicing, , 2nd edition, New Age International Publishers, 2001.
2.	**Gerald w. Collins,** Fundamentals of Digital Television Transmission', John Wiley, 2001.

Reference Books:

1.	**R.G.Gupta, "**Audio and Video Systems(Second Edition) **",**McGraw Hill Education Limited.

Sub Title : SENSORS		
Sub Code: 18EC564	**No. of Credits:3=3: 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand various kinds of a sensors and their working principle
2. Understand the working of various mechanical ,electro mechanical sensors.
3. Know the various thermal and magnetic sensors and their working principle.
4. Know the working of smart sensors..
5. Learn how different types of sensors are used for various practical applications.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**INTRODUCTION:** What are sensors/transducers?, principles, classification, parameters, Environmental parameters, Characterization. **MECHANICAL AND ELECTROMECHANICAL SENSORS:** Introduction, resistive potentiometer, Strain gauge, Inductive sensors, capacitive sensors, Force/stress sensors using Quartz Resonators, Ultrasonic sensors. ***TEXT 1***	08	L1,L2,L3.
2	**THERMAL SENSORS:** Introduction, Gas thermometric sensors, Thermal expansion type thermometric sensors, Dielectric constant and refractive index thermo sensors. Nuclear thermometer, magnetic thermometer, Resistance change type thermometric sensors, thermo emf sensors, Thermal radiation sensors. ***TEXT 1***	08	L1,L2,L3.
3	**MAGNETIC SENSORS:** Introduction, Sensors and the principle behind, Magneto resistive sensors, Hall effect and sensors, Inductance and eddy current sensors, Angular/rotary movement transducer, Eddy current sensors, Electromagnetic flow meter, Switching magnetic sensor, SQUID sensor. ***TEXT 1***	08	L1,L2,L3.
4	**SMART SENSORS:** Introduction, Primary sensors, Excitation, Amplification, filters, converters, Compensation, Information coding/ processing, Data communication, The Automation. ***TEXT 1.***	07	L1,L2,L3.
5	**SENSORS- THEIR APPLICATIONS:** Introduction, Automotive sensors, Home Appliance sensors, Aerospace sensors, Sensors for Manufacturing, Medical diagnostic sensors, Sensors for environmental monitoring. ***TEXT 1.***	08	L1,L2,L3,L5

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1: Understand the basic knowledge of various kinds of sensors and their working principle..

CO2: Analyze the functions of various thermal and magnetic sensors.

CO3: Apply the basic principles of various kinds of sensors, to build some home appliance sensors.

CO4: analyze the working of various smart sensors.

CO5: list and illustrate the various applications of different sensors.

Cos	Mapping with POs
CO1	PO1, PO11, PO12
CO2	PO1, PO2, PO5, PO11, PO12
CO3	PO1, PO2, PO8, PO11, PO12
CO4	PO1, PO2, PO5, PO11, PO12
CO5	PO1, PO2, PO3, PO11, PO12

Text Book:	
1.	D.Patranabis, "Sensors and Transducers", PHI Learning Private Limited, New Delhi – 110 001, Second Edition 2010

Reference Books:	
1.	ohn Vetelino, Aravind Reghu, "Introduction to Sensors", 2011

Web Links.

1 http://nptel.ac.in/courses/117105082/

2 http://www.electronics-tutorials.ws/io/io_3.html

3 http://www.dowaytech.com/en/1776.html

Sub Title : **Microcontroller Lab**		
Sub Code: 18ECL57	**No. of Credits:1=0 : 0 : 1 (L-T-P)**	**No. of lecture hours/week : 02**
Exam Duration : 3 Hours	**CIE + SEE = 50 + 50 =100**	**Total No. of Contact Hours :26**

Course objectives:

1. 1. To learn the architecture of 8051 Microcontroller.
2. To learn the Instruction set and Embedded C for MCS51.
3. Ability to write a ALP and C program for a given algorithm and implement the same
4. To learn the I/O ports and interfacing techniques with MCS51.
5. Ability to develop single chip solution using MCS51.

Unit No.	Syllabus contents	No of Hours	RBT level
PART-A PROGRAMMING WITH 8051 MICROCONTROLLER			
1.	**Data Transfer**: Block move, Exchange, Finding largest element in an array, sorting.	2	L1,L2,L3
2.	**Arithmetic Instructions**: Addition/subtraction, multiplication and division, square, Cube	3	L1,L2,L3
3.	**Counters:** 8/16 bit (Software)	2	L1,L2,L3
4.	**Boolean & Logical Instructions (Bit manipulations):** Logic gates, Adder/Subtractor, multiplexer circuits	2	L1,L2,L3
5.	**Code conversion**: BCD – ASCII; ASCII – Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX.	2	L1,L2,L3
6.	**Programs to generate time delay using** on-Chip timer/Counter, Program as event counter, Programs using serial port and Programs using interrupts.	2	L1,L2,L3
PART B INTERFACING PROGRAMS:			
1.	Program to display BCD UP counting	2	L1,L2,L3
2.	DAC interfacing(square, triangular and ramp)	2	L1,L2,L3
3.	Program to control the stepper motor	4	L1,L2,L3
4.	Program to display the key pressed	2	L1,L2,L3
5.	LCD interfacing		L1,L2,L3

Course Outcomes:

CO1. Understand the architectural features of microcontrollers.
CO2. Explain the instruction sets of Microcontrollers and write Assembly and High level Programs.
CO3. Study the various features of Microcontrollers based systems.
CO4. Study the applications of Microcontrollers for real time systems.
CO5. Development of single chip solutions

Cos	Mapping with POs
CO1	PO2, PO3
CO2	PO2, PO3

CO3	PO2, PO3, PO11, PO12
CO4	PO2, PO3, PO11, PO12
CO5	PO2, PO3, PO11, PO12

Text Book:	
1.	**Kenneth J, Ayala**, "The 8051 Microcontroller Architecture, Programming & Applications", 2edition, 1996 / Thomson Learning 2005.
2.	**Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay,** "The 8051 Microcontroller and Embedded Systems – using assembly and C",; PHI, 2006 / Pearson, 2006.

Sub Title : Digital Signal Processing Laboratory		
Sub Code: 18ECL58	**No. of Credits:1=0 : 0 : 1 (L-T-P)**	**No. of lecture hours/week : 02**
Exam Duration : 3 Hours	**CIE + SEE = 50 + 50 =100**	**Total No. of Contact Hours :26**

Course Objectives:

1. To analyze the sampling process, impulse response, convolution, frequency domain response
2. of LTI systems
3. To analyze and design digital IIR and FIR filters
4. To demonstrate the DSP algorithms using Matlab software
5. To demonstrate the DSP algorithms using Code Composer Studio

Unit No.	Syllabus contents	No of Hours	RBT level
1.	**Matlab Programs** 1. Verification of sampling theorem. 2. Impulse response of a given system 3. Linear convolution of two given sequences. 4. Circular convolution of two given sequences 5. Autocorrelation of a given sequence and verification of its properties. 6. Cross correlation of given sequences and verification of its properties. 7. Solving a given difference equation. 8. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum. 9. Linear convolution of two sequences using DFT and IDFT. 10. Circular convolution of two given sequences using DFT and IDFT 11. Design and implementation of FIR filter to meet given specifications. 12. Design and implementation of IIR filter to meet given specifications. . **TEXT 1 and TEXT2**	24	L1, L2,L3
2.	**Hardware experiments** 1. Linear convolution of two given sequences. 2. Circular convolution of two given sequences. 3. Computation of N- Point DFT of a given sequence 4. Noise: Add noise above 3 KHz and then remove; Interference suppression using 400 Hz tone. 5. Impulse response of first order system. **TEXT 2**	12	L3,L4, L5

NOTE: Experiments from1 to 5 will be taught by digital and online platform.

Course Outcomes:

CO1	Define and verify the sampling theorem, impulse response, convolution and frequency response of the system
CO2	Understand DFT, IDFT, Auto correlation and Cross correlation
CO3	Analyze and design digital IIR and FIR filters.
CO4	Demonstration of DSP algorithms using Matlab software.
CO5	Demonstration of DSP algorithms using Code Composer Studio software.

Course Outcomes Mapping with Programme Outcomes.

CO1	PO1,PO2,PO3,PO4,PO5, PO12	PO11,
CO2	PO1,PO2,PO3,PO4,PO5, PO12	PO11,
CO3	PO1,PO2,PO3,PO4,PO5, PO12	PO11,
CO4	PO1,PO2,PO3,PO4,PO5, PO12	PO11,
CO5	PO1,PO2,PO3,PO4,PO5, PO12	PO11,

Text Books.

1 Sanjeet K. Mitra, “Digital Signal Processing using MATLAB”, Edition, TMH, 2001

2 B. Venkataramani and Bhaskar, “Digital Signal Processors”, edition, TMH, 2002

Reference Text Books.

1 J. G. Proakis & Ingale, “Digital Signal Processing using MATLAB”, edition, Mc Graw Hill,
2000

Sub Title : CMOS VLSI DESIGN		
Sub Code: 18EC61	**No. of Credits:4=4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Impart knowledge of MOS transistor theory and CMOS technologies
2. Learn the operation principles and analysis of inverter circuits, Understand basic circuit concepts and scaling of MOS circuits.
3. Representation of different forms of diagrams like layout & stick diagram.
4. Different CMOS logic structures
5. Analyze adder & multiplier circuits, Design Combinational, sequential and dynamic logic circuits as per the requirements.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**MOS Transistor theory:** Enhancement and Depletion mode operation MOS transistors (p & n type), MOS fabrication (p & n type), CMOS fabrication. MOS device design equations, Second order effects of MOS, Static CMOS Inverter DC Characteristics, Beta Ratio Effect, Noise Margin, Pass Transistor, Transmission Gate, Tristate Inverter. **Scaling of MOS Circuits:** Scaling models and scaling factors, Scaling factors for device parameters, Limitation of Scaling (Points). (**Text 1, 2)**	10	L1,L2
2	**Circuit Design Processes:** MOS layers, Stick diagrams, Design rules and layout, lambda-based design rules. **Basic Circuit Concepts:** Sheet resistance, Area capacitances, Capacitance calculations, the delay unit, Inverter delays, driving capacitive loads. **(Text 1)**	9	L1, L2
3	**CMOS Logic Structures:** CMOS Complementary Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic, BiCMOS logic, Cascaded Voltage Switch Logic (CVSL). **(Text 2, 3).**	10	L1,L2,L3

4	**Datapath Subsystem I:** Single bit addition, carry generation & propagation, PG Carry-Ripple Addition, Manchester carry chain adder, carry skip adder, carry select, conditional sum adders. **DataPath Subsystems II:** Unsigned Array Multiplication, 2's Complement Array Multiplication (Modified Baugh-Wooley two's complement Multiplier), Booth encoding (Radix 4). **(Text 3).**	11	L1,L2
5	**Sequential MOS Logic Circuitry:** SR Latch Circuitry, Clocked latch and Flip Flop Circuitry, CMOS D-Latch and Edge Triggered Flip-Flop. **(Text 4)**	12	L1,L2,L3

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2 Assignment - 2 from units 3, 4 and 5.

Note 3. Unit 5- Digital Teaching and Learning.

Course Outcomes:

CO1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling
CO2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
CO3. Describe different logic structures.
CO4. Design of Adder and Multiplier circuits using MOS transistors
CO5. Demonstrate ability to design Combinational, sequential and dynamic logic circuits.

Cos	**Mapping with POs**
CO1	PO1,PO2,PO3,PO5
CO2	PO1,PO2,PO3
CO3	PO1,PO2,PO3
CO4	PO1,PO2,PO3
CO5	PO1,PO2,PO5

Text Book:

1.	**Douglas A Pucknell & Kamran Eshragian**, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
2.	**Neil H. E. Weste, and David Money Harris** , "CMOS VLSI Design- A Circuits and Systems Perspective", 4th Edition, Pearson Education.
3.	**Neil H.E Weste, David Harris, Ayan Banerjee,** "CMOS VLSI design- A circuits and systems perspective", Third edition Pearson Education (Asia) Pvt. Ltd, 2006
4.	**Sung Mo Kang & Yosuf Leblebici**, "CMOS Digital Integrated Circuits: Analysis and Design" -, Third Edition, Tata McGraw-Hill.

Reference Books:	
1.	**R. Jacob Baker**, "CMOS Circuit Design, Layout and Simulation", edition, John Wiley India Pvt. Ltd, year
2.	**Behzad Razavi,** "Design of Analog CMOS Integrated Circuits", TMH, 2007.

Web Links:	
1.	http://nptel.ac.in

Subject Title : Embedded Systems		
Sub. Code: 18EC62	**No. of Credits:03=03:0:0 (L -T – P)**	**No. of Lecture Hours/Week : 03**
Exam Duration: 03 Hrs	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours:39**

Course objectives:

1. Understand the basic concepts of Embedded Systems.
2. Explain the Characteristics and quality attributes and Program of Embedded Systems.
3. Get exposure to an advanced microcontroller Cortex M3.
4. Understand the definition, structure and Working of Real Time Operating system.
5. Analyze different Embedded Systems in various Domain applications.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Typical Embedded System:** Definition, Embedded systems vs. General Computing Systems, Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components, PCB and Passive Components. TEXT 1	10	L1,L2,L3.
2	**Characteristics and Quality Attributes of Embedded Systems:** Characteristics of an Embedded system, Quality attributes of Embedded Systems. **Hardware Software Co-Design and Program Modelling:** Fundamental issues in Hardware Software Co-Design, Computational Models in Embedded Design.	07	L1,L2,L3.
3	**ARM-32bit Microcontroller:** ARM Cortex-M3 Processor-Introduction, Overview of the Cortex-M3, Cortex-M3 Basics, Instruction Sets. TEXT 2	07	L1,L2,L3.
4	**RTOS for Embedded System Design:** Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Multiprocessing and Multitasking, Task scheduling, Task Communication, Device Drivers, How to choose an RTOS. TEXT 1	08	L1,L2,L3.
5	**Trends in the Embedded Industry:** Processor trends in embedded system, Embedded OS trends, Development Language Trends, Open Standards, Frameworks and Alliances, Bottlenecks. **Embedded Systems-Application and Domain Specific**: Washing Machine-application specific Embedded System, Automotive-Domain Specific Example of Embedded Systems, Key Players of Automotive Embedded Market. **Design Case Studies**: Digital camera, Embedded Systems in Automobile, Smart Card Reader, Automated Meter Reading System. TEXT 1	07	L1,L2,L3.

Note 1.Unit 1, 2, 3, 4 and 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3. Unit 4-Digital Teaching and Learning.

CO1. Understand different blocks of a Typical Embedded System.
CO2. Analyse different characteristics, quality attributes and modelling Techniques of embedded system design
CO3. Apply the knowledge of Instruction Set to program ARM 32bit Microcontroller.
CO4. Analyze the concepts of Real time kernel & Operating System services.
CO5. Evaluate the current trends in embedded industry and analyse different application and domain specific examples of embedded systems through case studies.

COs	**Mapping with POs**
CO1	PO1,PO3
CO2	PO1,PO2,PO3,PO4,PO5
CO3	PO1,PO2,PO3,PO4,PO5,PO6
CO4	PO1,PO2,PO3,PO4,PO5
CO5	PO1,PO2,PO3,PO4,PO5,PO6

Text Book:	
1.	Shibu K V, "Introduction to Embedded Systems", First Edition, Tata McGraw Hill Education Private Limited, 2009
2.	Joseph Yiu,"The Definitive Guide to the ARM Cortex-M3", Second Edition, Newnes, (Elsevier), 2008

Reference Books:	
1.	Raj Kamal, "Embedded Systems – Architecture, Programming and Design", edition, Mc Graw Hill, 2012
2.	James K Peckol "Embedded Systems – A contemporary Design Tool", edition, John Weily, 2008

Web Links:	
1.	https://onlinecourses.nptel.ac.in/noc20_cs15/course

Sub Title: Computer Communication Network		
Sub Code:18EC63	**No. of Credits:4=4: 0: 0 (L-T-P)**	**No. of lecture hours/week: 4**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Insight into the basics of networking, OSI reference and TCP/IP model.
2. Study of access links, protocols, error detection and correction techniques in the data link layer.
3. Understanding of router, routing algorithms, addressing techniques of the network layer.
4. Reliable data transfer, multiplexing, demultiplexing and congestion control techniques of the transport layer.
5. Services, Protocols, directory service and Sockets of the application layer

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Basics of computer Communications Network:** Network Components, The Network Core, Protocol Layers and their Service Models, Delay, Loss, and Throughput in packet switched Network. Network types, Network Addressing, Network topologies, Network connecting devices. **Text1, Text2**	10	L1, L2, L3
2	**The Link Layer: Links, Access Networks, and LANs:** Introduction to the Link Layer, Error-Detection and Correction Techniques, Multiple Access Links and Protocols, Switched Local Area Networks, Link Virtualization **Text1**	10	L1, L2, L3
3	**The Network Layer:** Introduction, Virtual Circuit and Datagram Networks, What's Inside a Router? The Internet Protocol (IP): Forwarding and Addressing in the Internet, Routing Algorithms, Routing in the Internet, Broadcast and Multicast Routing **Text1**	11	L1, L2, L3
4	**Transport Layer:** Introduction and Transport-Layer Services, Multiplexing and De-multiplexing, Connectionless Transport: UDP, Principles of Reliable Data Transfer, Connection-Oriented Transport: TCP, Principles of Congestion Control, TCP Congestion Control. **Text1**	11	L1, L2, L3
5	**Application Layer:** Principles of Network Applications, The Web and HTTP, File Transfer: FTP, Electronic Mail in the Internet, DNS—The Internet's Directory Service, Peer-to-Peer Applications, Socket Programming. **Text1**	10	L1, L2, L3

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From unit 1 and 2, Assignment2 from units 3,4 and 5
3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 1 - Digital teaching and learning

Course Outcomes	
CO1	Define the network components, layers, addressing, topology, connectivity and network types for data transmission.
CO2	Distinguish the basic network configurations and standards associated with each network.
CO3	Describe the layering architecture of computer networks and distinguish between the OSI reference model and TCP/IP protocol suite.
CO4	Identify the protocols and functions associated with the transport layer services.
CO5	Construct a network model and determine the routing of packets using different routing algorithms

COs	**Mapping with POs**
CO1	PO2, PO3, PO4
CO2	PO2, PO3, PO4, PO5
CO3	PO2, PO3, PO4, PO5, PO12
CO4	PO2, PO3, PO4, PO5, PO12
CO5	PO2, PO3, PO4, PO5, PO12

Text Book:

1. James F. Kurose, Keith W. Ross, "**Computer Networks**", Pearson Education, 6th Edition, **2017**.
2. B.Forouzan ," **Data Communication and Networking**", TMH, 4th Edition, ***2006***.
   CCNA routing and Switching study guide.
3.

Reference Books:

1. Russel Bradford, "**The Art of Computer Networking"**, Pearson Education, Ist Edition, **2007**.

MOOCS:

1. nptel.ac.in/courses/106105081/1
2. http://www.bau.edu.jo/UserPortal/UserProfile/PostsAttach/10617_1870_1.pdf

Sub Title : Semiconductor Fabrication		
Sub Code: 18EC641	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 05 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To be able to understand Scope of semiconductor Materials and Devices.
2. To be able to understand the Process of Crystal Growth.
3. To be able to understand the Photolithography and Etching.
4. To be able to classify the Diffusion and Ion Implantation.
5. To be able to understand the Film Deposition and Process Integration.

UNIT No	Syllabus Content	No of Hours
1	**Introduction to Semiconductor:** semiconductor Materials, Devices, Semiconductor process technology-key semiconductor technology, technology trends. Basic Fabrication Steps-oxidation, photolithography, etching, diffusion, Ion Implantation and metallization. **Text1**	7
2	**Crystal Growth:** Silicon crystal growth from the melt-starting material, czochralski technique, distribution dopant, effective segregation coefficient. Silicon float zone process. GaAs crystal growth techniques- starting materials, crystal growth techniques. Material characterization- wafer shaping, crystal characterization. **Silicon Oxidation:** Thermal oxidation process-kinetics of growth, thin oxide growth. Impurity redistribution during oxidation, Masking properties of silicon dioxide, oxide quality, oxide thickness characterization. **Text1**	8
3	**Photolithography and Etching:** Optical Lithography- the clean room, exposure tools, masks, photo resist, pattern transfer and resolution enhancement technique. **Etching:** Wet chemical etching-Si etching, Silicon dioxide etching, silicon Nitride and poly silicon etching, Aluminum etching and GaAs etching. Dry etching- Plasma Fundamentals, Etch mechanism. **Text1**	8
4	**Diffusion and Ion Implantation:** Basic Diffusion Process- Diffusion Equation, Diffusion profiles. Extrinsic Diffusion and Lateral diffusion. **Introduction Ion Implantation:** Range of Implanted Ions- Ion Distribution, Ion Stopping, Ion Channeling. Implant Damage and Annealing- Implant Damage, Annealing. **Text1**	8
5	**Film Deposition and Process Integration:** Epitaxial Growth Techniques-Chemical Vapor Deposition. Structures and Defects in Epitaxial Layers, Dielectric Deposition- Si Dioxide, Si Nitride. Poly silicon Deposition. Metallization- Physical Vapor Deposition and Aluminum Metallization and copper Metallization.	8

	Text1	

Note 1: All the units will have internal choice.

Note 2: Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1: Identify the Semiconductor Materials.
CO2: Ability to interpret Fabrication Steps.
CO3: Creation of semiconductor devices
CO4: Ability to Compare the types of Diffusion and Ion Implantation.

Cos	Mapping with POs
CO1	PO5,PO7,PO8
CO2	PO7,PO8,PO10
CO3	PO5,PO8,PO12
CO4	PO5,PO9,PO11

TEXT BOOK:

1. Gary S. May, Simon M. Sze, **"Fundamentals of Semiconductor Fabrication"** Wiley, 1st Edition, 2003.

REFERENCE BOOKS/WEBLINKS:

1. Anderson, Anderson" **Fundamentals of Semiconductor Devices**" McGraw-Hill Education, Indian Edition 2013.

2. Gary S. May, Costas J S, **"Fundamentals of Semiconductor Manufacturing and Process Control**" Wiley IEEE Press, 1st Edition, 2006

Sub Title : Cryptography		
Sub Code: 18EC642	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 05 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To impart the basic concepts of network security and classical encryption, number theory, stream ciphers, block ciphers and authentication
2. To interpret the cryptographic algorithms like stream ciphers and block ciphers using classical encryption techniques
3. To apply the concept of classical encryption techniques to stream ciphers and block ciphers
4. To analyse the stream ciphers, block ciphers and authentication functions
5. To design the stream ciphers, block ciphers and authentication functions

UNIT No	Syllabus Content	No of Hours
1	**Introduction:** Services, mechanisms and attacks, OSI security architecture, Model for network security. **Symmetric ciphers:** Symmetric Cipher Model, Substitution Techniques: Caesar Cipher, Mono Alphabetic Cipher, Playfair Cipher, Hill Cipher, polyalphabetic Cipher and One-Time Pad (OTP). Transposition Techniques, Rotor Machines, Steganography.	08
2	**Finite Fields:** Groups, Rings, Fields. Modular Arithmetic: Divisors, properties of modulo operator, modular arithmetic operations and properties. Euclid's Algorithm, Greatest Common Divisor (GCD), finding GCD. Finite Fields of the form GF (p): Finite fields of order p, finding multiplicative inverse in GF (p).	08
3	**Private Key Encryption:** Simplified DES, Block Cipher Principles, Data encryption standard (DES), Strength of DES, Block Cipher Design Principles and Block Cipher Modes of Operation, Evaluation Criteria for Advanced Encryption Standard, The AES Cipher.	08
4	**Public Key Encryption:** Principles of Public-Key Cryptosystems, The RSA algorithm. Key Management, Diffie - Hellman Key Exchange.	08
5	**Authentication Functions and Hash Functions:** Authentication functions, message authentication codes, hash functions, security of Hash functions and MACs	07

Note 1: All the units will have internal choice.

Note 2: Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1 - Define the basic concepts of network security, classical encryption, number theory, Private key, public key, authentication.

CO2 -Understand the structure of cryptographic algorithms and their applications.

CO3 -Apply the concept of classical encryption techniques to existing standard algorithms.

CO4 -Illustrate the significance of cryptographic algorithms and their applications.

CO5 -Design the private key and public key, authentication functions for applications.

Cos	Mapping with POs
CO1	PO1,PO2,PO10,P12
CO2	PO1,PO2,PO10,P12
CO3	PO1,PO2, PO3, PO10,P12
CO4	PO1,PO2, PO3, PO10,P12
CO5	PO1,PO2,PO10,P12

TEXT BOOK:

1. William Stallings, Cryptography & Network Security – Principles and Practice, 5th Edition, Pearson, 2011.

REFERENCE BOOKS/WEBLINKS:

1. Behrouz Forouzan, Cryptography and Network Security, 2nd Edition, TMH, 2010
2. Alfred J. Menezes, Paul C. Van Oorschot and Scott A. Vanstone, Handbook of Applied Cryptography, CRC Press, Reprint 2001.
3. Bruce Scheiner, Applied cryptography: protocols, algorithms, and source code in C, 2nd Edition, Wiley, 2008.

Web Links:

1. http://www.nptel.ac.in/courses/106105031/
2. http://faculty.mu.edu.sa/public/uploads/1360993259.0858Cryptography%20and%20Network%20Security%20Principles%20and%20Practice,%205th%20Edition.pdf

Sub Title : INFORMATION THEORY AND CODING		
Sub Code: 18EC643	**No. of Credits:03=03:0:0 (L :T :P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives: This course will enable students

1. Understand the basic concepts of information theory.
2. Apply the concepts of source coding.
3. Analyze the fundamental limits on performance of a communication system.
4. Study the different error control coding techniques.
5. Analyze the various types of binary cyclic codes.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**INFORMATION THEORY:** Introduction, Measure of information, Average information content of symbols in long independent sequences, Average information content of symbols in long dependent sequences. Markoff statistical model for information source, Entropy and information rate of mark-off source. TEXT 1	08	L1,L2, L3, L4
2	**SOURCE CODING:** Encoding of the source output, Shannon's encoding algorithm, Source coding theorem, Huffman coding.(Only binary codes) TEXT 1	06	L1,L2,L3, L4
3	**FUNDAMENTAL LIMITS ON PERFORMANCE:** Communication Channels: Discrete communication channels, Continuous communication channels. Discrete memory less Channels, Mutual information, Channel Capacity, Channel coding theorem, Channel capacity Theorem. TEXT 1 and TEXT 2	08	L1,L2,L3, L4
4	**INTRODUCTION TO ERROR CONTROL CODING:** Introduction, Types of errors, examples, Types of codes, Linear Block Codes: Matrix description, Error detection and correction, Standard arrays and table look up for decoding. TEXT 1 and TEXT 2	09	L1,L2,L3 L4,L5
5	**Binary Cycle Codes**, Algebraic structures of cyclic codes,		

	Encoding using an (n-k) bit shift register, Syndrome calculation. BCH codes, RS codes, Golay codes, Turbo codes, LDPC codes. TEXT 1	08	L1,L2,L3 L4,L5,L6

Note 1.Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2 Assignment - 2 from units 3, 4 and 5.

Note 3.Unit 4 (Introduction to Error control coding) will be taught using Digital learning platform.

Course Outcomes:

CO1: Understand the concepts of information theory and mark-off statistical model, Evaluate Entropy and information rate of markov source

CO2: Apply information theory to source coding, analyze various types of coding techniques and evaluate average code Length, Source coding efficiency and redundancy

CO3: Analyze different types of special channels and Evaluate Channel capacity, channel capacity theorem

CO4: Analyze Various types of errors and error control coding techniques, error detection and correction techniques..

CO5: Design source encoder and syndrome calculation circuits, understand various codes like binary cyclic codes, RS code, Golay code, LDPC and Turbo codes

Cos	Mapping with POs
CO1	PO1,PO2,PO8
CO2	PO1,PO2,PO3,PO8
CO3	PO1,PO2,PO3,PO8
CO4	PO1,PO2,PO3,PO8
CO5	PO1,PO2,PO8

Text Book:

1.	K. Sam Shanmugam,"Digital and Analog communication systems ", Second Edition, John Wiley India Pvt, 1996
2.	Simon Haykins, "Digital communication", Second edition, John Wiley India Pvt. Ltd, 2008

Reference Books:

1.	J. Das, S. K. Mullick, P. K. Chatterjee ,"Principles of digital communication",Wiley, 1986 - Technology & Engineering
2.	P.S Satyanarayana, "Information Theory and Coding", edition, Dyanaram Publications, Reprint 2001
3.	Giridhar, "Information Theory and Coding", 2nd edition, Pooja Publications, 2006

4.	Ranjan Bose, “Information Theory and coding and Cryptography”, 2nd edition, TMH, 2009

Sub Title: System Verilog for verification		
Sub.Code: 18EC644	**No. of Credits:3=3:0:0 (L - T – P)**	**No. of Lecture Hours/Week : 03**
Exam Duration:03 Hrs	**CIE+Assignment+Group Activity +SEE=45+5+50=100**	**Total No.of Contact Hours:39**

Course objectives:

1. Insight to apply System Verilog concepts to do synthesis, analysis and architecture design.
2. Understanding of System Verilog and SVA for verification, and understand the improvements in verification efficiency.
3. Analyze coverage driven verification for given design under test (DUT).
4. Understand advanced verification features, such as the practical use of classes, randomization, checking, and coverage.
5. Knowledge to communicate the purpose and results of a design experiment in written and oral presentations.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Verification Guidelines:** Introduction, Verification Process, Verification Plan, Verification Methodology Manual, Basic Test bench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage. **Text 1**	08	L1, L2, L3
2	**Data Types:** Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings. **Text 1**	07	L1, L2, L3
3	**Basic Object Oriented Programming:** Where to Define a Class, OOP Terminology, Understanding Dynamic Objects. **System Verilog Assertions**: Types of Assertions and examples. **Text 1**	08	L1, L2, L3
4	**Threads and Inter-process Communication:** Working with Threads, Inter-process Communication, Events, Semaphores, Mailboxes, Building a Test bench with Threads and IPC Functional Coverage: Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Coverage Options, Parameterized Cover Groups. **Text 1 and Text 2**	08	L1, L2, L3, L4
5	**Introduction to formal verification:** Introduction to formal techniques and property specification, Reachability analysis, Elements of property languages, Property language layers, PSL basics, Formal test plan process. **Text 2 and Text 3**	08	L1, L2, L3

Note 1.Two assignments are evaluated for 5 marks

Note 2.Group activity is evaluated for 5 marks.

Note 3.Unit-5-Digital learning and teaching.

Course Outcomes

CO1. Use System Verilog to create correct, efficient, and re-usable models for digital designs.
CO2. Use System Verilog to create test benches for digital designs.
CO3. Understand and effectively exploit new constructs in System Verilog for verification.
CO4. Use of threads and inter-process communication for system Verilog.
CO5. Understand the process of formal verification.

COs	**Mapping with POs**
CO1	PO2, PO3, PO4
CO2	PO2, PO3, PO4, PO5
CO3	PO2, PO3, PO4, PO5, PO12
CO4	PO2, PO3, PO4, PO5, PO12
CO5	PO2, PO3, PO4, PO5, PO12

Text Book:	
1.	Chris Spear, "**System Verilog for Verification: A Guide to Learning the Test bench Language Features"**, Springer 2006.
2.	Janick Bergeron, **"Writing Test benches Using System Verilog**", Springer, 2006.
3.	Stuart Sutherland, Simon Davidman and Peter Flake, **"System Verilog for Design: A Guide to Using System Verilog for Hardware Design and Modeling**", 2nd Edition, Springer.

Reference Books:	
1.	Janick Bergeron, **"Writing Test benches: Functional Verification of HDL Models**", Second edition, Kluwer Academic Publishers, 2003.
2.	Mark Glasser, **"Open Verification Methodology Cookbook**", Springer, 2009.
3.	Andreas S. Meyer, **"Principles of Functional Verification**", Elsevier Science, 2004.
4.	Harry D. Foster, Adam C. Krolnik, David J. Lacey, "**Assertion-Based Design**", 2nd Edition, Kluwer Academic Publishers, 2004.

MOOCS:

1. ElectronicDesignAutomationhttp://nptel.ac.in/courses/106105083/
2. DigitalsystemdesignwithPLDsandFPGAshttp://nptel.ac.in/courses/117108040/ Fundamentals of HDL (Lecture #008)
3. https://www.youtube.com/watch?v=rdAPXzxeaxs&index=8&list=PLE3BC3EBC9CE 15FB0

Sub Title : Internet of Things		
Sub Code: 18EC645	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE =40+ 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Assess the genesis and impact of IoT applications, architectures in real world.
2. Illustrate diverse methods of deploying smart objects and connect them to network.
3. Understanding IP as the IoT Network Layer.
4. Compare different Application protocols for IoT.
5. Infer the role of Data Analytics.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	What is IoT, Genesis of IoT, IoT and Digitization,IoT Impact, Convergence of IT and IoT, IoT Challenges, IoT Network Architecture and Design, Drivers Behind New Network Architectures, Comparing IoT Architectures, A Simplified IoT Architecture, The Core IoT Functional Stack, IoT Data Management and Compute Stack. TEXT-1	09	L1, L2, L3
2	Smart Objects: The "Things" in IoT, Sensors, Actuators, and Smart Objects, Sensor Networks, Connecting Smart Objects, Communications Criteria, IoT Access Technologies. TEXT 1	10	L1,L2,L3
3	IP as the IoT Network Layer, The Business Case for IP, The need for Optimization, Optimizing IP for IoT, Profiles and Compliances TEXT 1	06	L1,L2,L3,L4
4	Application Protocols for IoT, The Transport Layer, IoT Application Transport Methods. TEXT 1	06	L1,L2,L3,L4
5	Data and Analytics for IoT, An Introduction to Data Analytics for IoT, Machine Learning, Big Data Analytics Tools and Technology, Edge Streaming Analytics, Network Analytics, TEXT 1	08	L1,L2,L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Each Unit will have assignments that are evaluated for 5 marks.

Note 3.Unit 2 taught through Digital Learning.

Course Outcomes:

CO1. Interpret the impact and challenges posed by IoT networks leading to new architectural models.
CO2. Compare and contrast the deployment of smart objects and the technologies to connect them to network.
CO3. Appraise the role of IoT protocols for efficient network communication.
CO4. Analyse higher layer IoT Protocols.
CO5. Elaborate the need for Data Analytics

Cos	Mapping with POs

CO1	PO6
CO2	PO6
CO3	PO6
CO4	PO6, PO12
CO5	PO6, PO12

Text Book:	
1.	**David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry**,"IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things", 1st Edition, Pearson Education (Cisco Press Indian Reprint).

Reference Books:	
1.	**Srinivasa K G**, "Internet of Things",CENGAGE Leaning India, 2017
2.	**Vijay Madisetti and ArshdeepBahga**, "Internet of Things (A Hands-on-Approach)", 1st Edition, VPT, 2014. (ISBN: 978-8173719547)
3.	**Raj Kamal,** "Internet of Things: Architecture and Design Principles", 1st Edition, McGraw Hill Education, 2017. (ISBN: 978-9352605224)

Web Links:	
1.	https://swayam.gov.in/nd1_noc20_cs22
2.	*www.tutorialspoint.com › internet_of_things › internet...*

Sub Title: Autotronics and Vehicle Intelligence		
Sub Code:18EC646	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Assignment + SEE = 40 + 5 +5+ 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To understand overview of the automobile with emphasis on the basic operation of the engine
2. To understanding of electronic technology
3. To examine how electronics has been applied to the major systems
4. To understand various sensors and actuators and get some ideas and methods that may be used in the future
5. Understand the concepts of vehicle motion control.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	Automotive Fundamentals Overview – Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Ignition Timing, Drive Train Transmission, Brakes, Steering System. TEXT 1 and REFERENCE TEXT 1	08	L1, L2
2	Safety systems - Collision Avoidance Radar warning Systems, Low tire pressure warning system, navigation-navigation sensor, radio navigation signpost navigation, dead reckoning navigation, voice recognition cell phone dialing. TEXT BOOK:1,REF. BOOK :3	08	L1, L2
3	Sensors – Airflow rate sensor, Strain gauge MAP sensor, Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle angle sensor, Temperature sensor, Exhaust Gas Oxygen Sensor Knock Sensor. TEXT 1 REFERENCE TEXT 2	08	L1, L2, L3
4	Vehicle Motion Control – Cruise Control System-speed response curves, digital cruise control, Antilock Brake System (ABS), Electronic Suspension system, Electronic suspension control system. TEXT BOOK:1,REF. BOOK :3	07	L1, L2, L3
5	Principle and Construction of Lead Acid and Lithium-Ion Battery-Characteristics of Battery Rating Capacity and Efficiency of Batteries-Various Tests on Batteries- Maintenance and Charging. Lighting System and Photometry: insulated and Earth Return System- Details of Head Light and Side Light- LED Lighting System- Head Light Dazzling and Preventive Methods Horns- Wiper System and Trafficator. TEXT 2	08	L1, L2, L3

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 1 - Digital teaching and learning

Course Outcomes

CO1. Identify the different sensors, Actuators, Engine Control, Ignition System and Spark plug.

CO2. Relate Safety systems.

CO3. Summarize the concepts of an electronic engine control system, Cruise Control System.

CO4. Demonstrate the Engine Efficiency.

CO5. To analyse the concepts of an electronic engine control system, Vehicle Motion Control, Safety systems, sensors and actuators.

COs	Mapping with POs
CO1	PO1,PO6
CO2	PO5,PO6
CO3	PO2,PO6,PO10
CO4	PO3,PO10,PO12
CO5	PO10,PO12,PO6

TEXT BOOKS:

1. William Ribbons, "Understanding Automotive Electronics", Seventh Edition, Elsevier Publishing, 2012
2. Young A.P & Griffiths "Automotive Electrical Equipment" , ELBS & New Press -1999.

REFERENCE BOOKS/WEB LINKS:

1. Robert Bosch GmbH, "Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive",Fifth Edition, Springer Fachmedien Wiesbaden Publishing, 2014
2. ASPENCORE Guide to: Sensors in Automotive — Making Cars See and Think Ahead" 2019
3. Vehicle Technology: Technical Foundations of Current and Future Motor Vehicles (De Gruyter Textbook) by Dieter Schramm (, Benjamin Hesse , Niko Maas , Michael Unterreiner

Sub Title: Automotive Electronics Engineering		
Sub Code:18EC651	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To understand overview of the automobile with emphasis on the basic operation of the engine
2. To understanding of electronic technology
3. To examine how electronics has been applied to the major systems
4. To understand various sensors and actuators and get some ideas and methods that may be used in the future
5. Understand the concepts of vehicle motion control.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	Automotive Fundamentals Overview – Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Ignition Timing, Drive Train Transmission, Brakes, Steering System. **TEXT 1 and REFERENCE TEXT 1**	08	L1, L2
2	Safety systems - Collision Avoidance Radar warning Systems, Low tire pressure warning system, navigation-navigation sensor, radio navigation signpost navigation, dead reckoning navigation, voice recognition cell phone dialing. **TEXT BOOK:1,REF. BOOK :3**	08	L1, L2
3	Sensors – Airflow rate sensor, Strain gauge MAP sensor, Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle angle sensor, Temperature sensor, Exhaust Gas Oxygen Sensor Knock Sensor. **TEXT 1 REFERENCE TEXT 2**	08	L1, L2, L3
4	Vehicle Motion Control – Cruise Control System-speed response curves, digital cruise control, Antilock Brake System (ABS), Electronic Suspension system, Electronic suspension control system. **TEXT BOOK:1,REF. BOOK :3**	07	L1, L2, L3
5	Electronic Engine Control – Concepts of an electronic engine	08	L1, L2, L3

	control system, definition of general terms - Engine parameters, variables, Engine Performance terms –Power , BSFC, Torque, Volumetric efficiency, thermal efficiency, calibration, Effect of air/fuel ratio on performance. **TEXT 1**		

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5
3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 1 - Digital teaching and learning

Course Outcomes

CO1. Identify the different sensors, Actuators, Engine Control, Ignition System and Spark plug.
CO2. Relate Safety systems.
CO3. Summarize the concepts of an electronic engine control system, Cruise Control System.
CO4. Demonstrate the Engine Efficiency.
CO5. To analyse the concepts of an electronic engine control system, Vehicle Motion Control, Safety systems, sensors and actuators.

COs	**Mapping with POs**
CO1	PO1,PO6
CO2	PO5,PO6
CO3	PO2,PO6,PO10
CO4	PO3,PO10,PO12
CO5	PO10,PO12,PO6

TEXT BOOKS:

1. William Ribbons, “Understanding Automotive Electronics”, Seventh Edition, Elsevier Publishing, 2012

REFERENCE BOOKS/WEB LINKS:

1. Robert Bosch GmbH, “Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive”,Fifth Edition, Springer Fachmedien Wiesbaden Publishing, 2014
2. ASPENCORE Guide to: Sensors in Automotive — Making Cars See and Think Ahead” 2019
3. Vehicle Technology: Technical Foundations of Current and Future Motor Vehicles (De Gruyter Textbook) by Dieter Schramm (, Benjamin Hesse , Niko Maas , Michael Unterreiner

Sub Title : NANOELECTRONICS		
Sub Code: 18EC652	**No. of Credits:3=3: 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Enhance basic engineering science and technical knowledge of Nanoelectronics.
2. Explain basics of top-down and bottom-up fabrication process, devices and systems.
3. Describe technologies involved in modern day electronic devices.
4. Know various nanostructures of carbon and the nature of the carbon bond itself.
5. Learn the photo physical properties of sensor used in generating a signal.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction** Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction. Fabrication methods: Top down processes, Bottom up processes. **(Text 1)**	08	L1,L2
2	**Inorganic semiconductor nanostructures** Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques. **(Text 1).**	08	L1, L2
3	**Carbon Nanostructures** Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. **(Text 2).**	08	L1,L2
4	**Fabrication techniques:** Requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques. **(Text 1).**	07	L1,L2

5	**Applications:** Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS **(Text 1)**	08	L1,L2

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3.Unit 5---digital teaching and learning.

Course Outcomes:

CO1. Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
CO2. Know the properties of carbon and carbon nanotubes and its applications.
CO3. Apply the knowledge to prepare and characterize nanomaterials.
CO4. Apply the knowledge to prepare and characterize nanomaterials.
CO5. Analyse the process flow required to fabricate state-of-the-art transistor technology.

Cos	Mapping with POs
CO1	PO1,PO2,PO3,PO5
CO2	PO1,PO2,PO3
CO3	PO1,PO2,PO3
CO4	PO1,PO2,PO3
CO5	PO1,PO2,PO5

Text Book:

1.	**Ed Robert Kelsall, Ian Hamley, Mark Geoghegan**, "Nanoscale Science and Technology", John Wiley, 2007.
2.	**Charles P Poole, Jr, Frank J Owens**, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.

Reference Books:

1.	**Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate**, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.
2.	**T Pradeep**, "Nano: The essentials-Understanding Nanoscience and Nanotechnology", TMH

Web Links:

1.	https://www.youtube.com/watch?v=w8Dq8blTmSA
2.	http://nptel.ac.in

Sub Title : Wireless Sensor Network		
Sub Code: 18EC653	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity + Assignment + SEE =40+ 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Students will be able to describe the unique issues in sensor networks.
2. Students will be able to describe current technology trends for the implementation and deployment of wireless sensor networks.
3. Students will be able to discuss the challenges in designing MAC, routing and transport protocols for wireless sensor networks.
4. Interpret the goals for different protocols
5. Students will be able to describe and implement protocols

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	Introduction: Unique Constraints and Challenges, Advantages of Sensor Networks, Energy advantage, Detection advantage, Sensor Network Applications, Habitat monitoring, Wildlife conservation through autonomous, non-intrusive sensing, Tracking chemical plumes, Ad hoc, just-in-time deployment mitigating disasters, Smart transportation: networked sensors making roads safer and less congested, Collaborative Processing.. TEXT1	08	L1, L2,L4
2	**Canonical Problem: Localization and Tracking,** A Tracking Scenario, Sensing Model, Collaborative Localization, Bayesian State Estimation, Distributed Representation and Inference of States: Impact of Choice of Representation, Design consideration in Distributed Tracking, Tracking Multiple Objects: State-Space Decomposition, Data Association, Sensor Models, Performance Comparison and Metrics TEXT 1	08	L1, L2,L4,L5
3	Networking Sensors: Key Assumptions, Medium Access Control, General Issues, Geographic, Energy-Aware Routing: Unicast Geographic Routing, Routing on a Curve, Energy-Minimizing Broadcast, Energy-Aware Routing to a Region, Attribute-Based Routing. **Infrastructure Establishment:** Topology Control, Clustering, Time Synchronization, Localization and Localization Services, **Sensor Tasking and Control :**Task-Driven Sensing ,Roles of Sensor Nodes and Utilities Information-Based Sensor Tasking Sensor Selection IDSQ: Information-Driven Sensor Querying ,Cluster Leader–Based Protocol ,Sensor Tasking in Tracking Relations TEXT 1	08	L1,L2,L3,L4,L5
4	Sensor Network Databases: Sensor Network Databases, Sensor Database Challenges, Querying The Physical Environment, Query Interfaces, Cougar sensor database and abstract data types,	08	L1,L4,L5

	Probabilistic queries, High-level Database Organization, In-Network Aggregation, Query propagation and aggregation, Tiny DB query processing, Query processing scheduling and optimization, Data-Centric Storage, Data Indices and Range Queries, One-dimensional indices, Multidimensional indices for orthogonal range searching, Non-orthogonal range searching, Distributed Hierarchical aggregation, Multi-resolution, Partitioning, Fractional cascading, Locality preserving hashing, Temporal Data, Data aging, Indexing motion data. TEXT 1		
5	Sensor Network Platforms: Sensor Node Hardware, Sensor Network Programming Challenges, Node-Level Software Platforms, Node-Level Simulators, Programming Beyond Individual Nodes: State-Centric Programming, and Tools Applications and Future Directions: Emerging Applications, Future Research Directions TEXT 1	07	L1,L2,L6

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.
Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.
Note 3.Unit 5 taught through Digital Learning.

Course Outcomes:
CO1. Define WSN, identify issues related to different protocols for WSN
CO2. Understand protocols require for Wireless Sensor Network
CO3. Explore current sensor technologies through algorithms, protocols, and applications
CO4. Analyse routing ,tracking problems, data base requirement and programing challenges
CO5. Interpret the design goals consideration tracking and evaluate the performance of different protocols for wireless Sensor Network

Course Outcomes Mapping with Programme Outcomes.	
CO1	PO1,PO2,PO5,PO6,PO10
CO2	P01, PO2, PO5,PO8
CO3	P01, PO4,PO5,PO6
CO4	P01, PO2,PO3
CO5	PO2, PO5,PO6,PO9

Text Book:

1.	Feng Zhao, Leonidas Guibas, "Wireless Sensor Networks, An Information Processing Approach", Elsevier, 2004

Reference Books:

1.	Kazem Sohrabi,Daniel Minoli.Taieb Znati "Wireless Sensor Networks", Wiley Inter science, Wiley India, 2007

Web Links:	
1.	https://onlinecourses.nptel.ac.in/noc17_cs07

Sub Title : ROBOTICS AND MACHINE VISION SYSTEM		
Sub Code: 18EC654	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity + Assignment + SEE =40+ 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To make the student understand various elements of robotic system and how they integrate.
2. To make the student understand various operations of robot end effectors.
3. To make the student understand various sensors that can be used in robotics
4. To make the student understand robot mechanics and artificial intelligence.
5. To make the student understand the fundamentals of machine vision

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**FUNDAMENTALS OF ROBOTICS:** Automation and Robotics, Robotics in science Fiction, A brief history of robotics, Robot Anatomy, Work volume, Robot drive systems, Control systems and Dynamic performance, Precision of movement, End effectors, Robotic sensors,. Robot applications *TEXT 1* .	7	L1,L2,L4
2	**ROBOT END EFFECTORS:** Introduction, Types of end effectors, Mechanical gripper, Other types of grippers, Tools as end effectors, The Robot/End effectors interface, Considerations in gripper selection and design. **SENSORS IN ROBOTICS:** Transducers and sensors, sensors in robotics, tactile sensors, proximity and range sensors, miscellaneous sensors and sensor based system. Use of sensors in Robotics. *TEXT 1*.	8	L1,L2,L3,L4,L5
3	**ROBOT MECHANICS:** Introduction to manipulator kinematics, homogeneous transformation and robot kinematics, manipulator path control, robot dynamics, configuration of a robot controller. **MACHINE VISION FUNDAMENTALS:** Introduction to machine vision, the sensing and digitizing function in machine vision, Image processing and Analysis. *TEXT 1*.	8	L1,L2,L3,L4
4	**ROBOT PROGRAMMING:** Methods of robot programming, leadthrough programming methods, a robot program as a path in space, motion interpolation, WAIT, SIGNAL and DELAY commands, branching. **ARTIFICIAL INTELLIGENCE:** Introduction, goals of AI research, AI techniques, LISP programming, AI and Robotics**.** *TEXT 1*.	9	L1,L2,L3,L4
5	**ROBOT APPLICATIONS IN MANUFACTURING:** Material transfer and machine loading/unloading. Processing operations. *TEXT 1*.	7	L1,L2,L3,L4,L6

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3.Unit 5 taught through Digital Learning.

Course Outcomes:

CO1. The student will get the basic knowledge of, various robotic elements, end effectors and various sensors that can be used in robotics.
CO2. The student will be able to analyze the robot mechanics using homogeneous transformation.
CO3. The student will be able to apply the robotic principles to build a new artificially intelligent system.
CO4. The student will be able to study the importance of Artificial Intelligence and robotics in Science fiction.
CO5. The student will be able to study and analyze the fundamentals of machine vision.

Course Outcomes Mapping with Programme Outcomes.	
CO1	PO1, PO11, PO12
CO2	PO1, PO2, PO11, PO12
CO3	PO1, PO2, PO3, PO11, PO12
CO4	PO1, PO2, PO3, PO6, PO11, PO12
CO5	PO1, PO2, PO3, PO11, PO12

Text Book:	
1.	M.P. Groover, M. Weiss, R.N. Nagel, N.G. Odrey, "Industrial Robotics-Technology, Programming and Applications", Choose an item. Tata McGraw-Hill Education Pvt Ltd,, 2008
2.	R.K.Mittal, I.J.Nagrath, Robotics and controls, Tata McGraw Hill Education Pvt.

Reference Books:	
1.	Sathya Ranjan Deb, "Robotics Technology and flexible Automation", 6th Edition, TMH, 2003.

Web Links:	
1.	http://www.galileo.org/robotics/intro.html
2.	http://www.columbiaokura.com/blog/blog/2013/10/14/types-of-robotic-end-effectors-(end-of-arm-tools)
3.	http://nptel.ac.in/courses/112103174/39

Subject Title: Embedded Systems Lab		
Sub. Code: 18ECL66	**No. of Credits: 1 = 0:1:0 (L - T – P)**	**No. of Lecture Hours/Week : 02**
Exam Duration:03 Hrs	**CIE +SEE = 50 + 50 = 100**	**Total No.of Contact Hours: 24**

Course objectives:

1. To study the features of LPC 1768 MCU.
2. Develop the Assembly level programming of ARM Cortex M3 Processor.
3. Develop the Embedded C level programming of ARM Cortex M3 Processor.
4. Understand Interfacing of different modules to LPC 1768 MCU.
5. Develop 32-bit microcontroller based Embedded system applications.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	Write a Assembly language program to link Multiple object files and link them together.	2	L1, L2, L3, L4
2	The Assembly language program i. To calculate the value of the function. ii. To store data in desired Memory location.	2	L1, L2, L3, L4
3	The Assembly language program 1. To calculate the 2's Complement of a number. 2. To calculate the Square of a number .	2	L1, L2, L3, L4
4	Write a C program to Output the message using UART of LPC1768.	2	L1, L2, L3, L4
5	Write a C Program to interface LED using LPC 1768.	2	L1, L2, L3, L4
6	Write a C Program to interface Relay using LPC 1768.	2	L1, L2, L3, L4
7.	Write a C Program for DC motor/Stepper motor rotation using LPC 1768.	2	L1, L2, L3, L4
8.	Write a C program to interface a Real Time Clock (RTC) of LPC 1768.	2	L1, L2, L3, L4
9	Write a program to read on-chip ADC value and display it on UART terminal using LPC 1768.	2	L1, L2, L3, L4
10	.Write a C programs to interface a DAC of LPC 1768.	2	L1, L2, L3, L4
11	Write a C program to demonstrate the use of an External interrupt in LPC 1768	2	L1, L2, L3, L4
12	Write a C program to interface Keypad using LPC 1768.	2	L1, L2, L3, L4

CO1. Understanding features of the architecture of ARM Cortex M3.
CO2. Understanding features of the architecture of LPC 1768 MCU

CO3. Write assembly level programs to program ARM Cortex M3

CO4. Interface different modules to LPC 1768 MCU.

CO5. Design and testing a program for Different Embedded applications.

COs	**Mapping with POs**
CO1	PO1, PO2,PO3, PO9
CO2	PO1, PO2,PO3 PO9
CO3	PO1, PO2, PO3, PO5, PO9
CO4	PO1, PO2, PO3, PO5,PO9
CO5	PO1, PO2, PO3, PO5,PO9

Reference Books:	
1.	Shibu K V, **"Introduction to Embedded Systems**", First Edition, Tata McGraw Hill Education Private Limited, 2009
2.	Joseph Yiu, "**The Definitive Guide to the ARM CORTEX-M3**", Second Edition, Newnes , **2008**
3.	NXP Semiconductors, "**LPC17xx user manual**",
4.	Micro-CM3768, "**ARM Cortex-M3 Development Board User Manual**

Note: Programming to be done in **Keil µvision-5** IDE tool and download the program on to a Cortex-M3 evaluation board **NXP LPC1768** using **Flash Magic Tool.**

Web Links:	
1.	https://www.youtube.com/watch?v=nyUry1o2SQQ&list=PLnFckqm074doPiUQkkhwpHzP0JI7tAg4p

Subject Title: CMOS VLSI DESIGN LAB		
Sub. Code: 18ECL67	**No. of Credits: 1 = 0:1:0 (L - T – P)**	**No. of Lecture Hours/Week : 02**
Exam Duration:03 Hrs	**CIE +SEE = 50 + 50 = 100**	**Total No. of Contact Hours: 24**

Course objectives:

1. Design, model, simulate and verify CMOS digital circuits
2. Design layouts CMOS digital circuits
3. Perform physical verification of CMOS digital circuits
4. Perform RTL- flow and understand the stages in ASIC design.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	DC, Transient analysis of CMOS logic-Universal gates schematic	2	L1, L2, L3, L4
2	DC, Transient analysis of CMOS full adder schematic	2	L1, L2, L3, L4
3	DC, Transient analysis of Pass transistor and transmission gates schematic	2	L1, L2, L3, L4
4	DC, Transient analysis of Sequential circuits schematic 1. Clocked D Latch 2. Master-Slave Edge Triggered Register	2	L1, L2, L3, L4
5	DRC and LVS analysis of CMOS Inverter layout	2	L1, L2, L3, L4
6	DRC and LVS analysis of Common Source Amplifier Layout	2	L1, L2, L3, L4
7.	DRC and LVS analysis of Common Drain Amplifier Layout	2	L1, L2, L3, L4
8.	DRC and LVS analysis of Differential Amplifier Layout	2	L1, L2, L3, L4
9	Synthesis and Simulation of Inverter using Verilog code	2	L1, L2, L3, L4
10	Synthesis and Simulation of Buffer Verilog code	2	L1, L2, L3, L4
11	Synthesis and Simulation of Basic/Universal Gate using Verilog code	2	L1, L2, L3, L4
12	Synthesis and Simulation of JK, MSJK flip-flops using Verilog code	2	L1, L2, L3, L4

CO1. Design and simulate basic CMOS circuits like different logic structures.
CO2: Design and simulate basic CMOS circuits like inverter, common source amplifier and

Differential Amplifier.
CO3: Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list.
CO4: Design and simulate combinational and sequential digital circuits using Verilog HDL.

COs	**Mapping with POs**
CO1	PO1, PO2,PO3, PO9
CO2	PO1, PO2,PO3 PO9
CO3	PO1, PO2, PO3, PO5, PO9
CO4	PO1, PO2, PO3, PO5,PO9

Text Books:	
1.	**Douglas A Pucknell & Kamran Eshragian**, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
2.	**Neil H. E. Weste, and David Money Harris** , "CMOS VLSI Design- A Circuits and Systems Perspective", 4th Edition, Pearson Education.
3.	**Neil H.E Weste, David Harris, Ayan Banerjee,** "CMOS VLSI design- A circuits and systems perspective", Third edition Pearson Education (Asia) Pvt. Ltd, 2006
4.	**Sung Mo Kang & Yosuf Leblebici**, "CMOS Digital Integrated Circuits: Analysis and Design" -, Third Edition, Tata McGraw-Hill.

Note: Digital Teaching and Learning: DRC and LVS analysis of Differential Amplifier Layout.

Software required: Cadence/or any other equivalent software

Web Links:	
1	http://nptel.ac.in

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

VII Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	MC	18HS71	Cost Management of Engg Projects	HS	03	--	--	03	050	050	100	02
2	PC	18EC71	Wireless Communication	EC	04	--	--	03	050	050	100	04
3	PC	18EC72	Microwave and Antenna	EC	04	--	--	03	050	050	100	04
4	PE	18EC73X	Professional Elective-3	EC	03	--	--	03	050	050	100	03
5	PE	18EC74X	Professional Elective-4	EC	03	--	--	03	050	050	100	03
6	OE	18EC75X	Open Elective-C	EC	03	--	--	03	050	050	100	03
7	PC	18ECL76	Advance Communication Lab	EC	--	--	02	02	050	050	100	01
8	PC	18ECL77	Computer Communication Network Lab	EC	--	--	02	02	050	050	100	01
9	Project	18ECP78	Project work phase-1	EC	--	--	02	02	050	050	100	02
10	INT	18ECI79	Internship	--	--	--	--	---	---	---	--	--
			Total		**20**	**--**	**06**	**24**	**400**	**400**	**800**	**23**

Internship: All the students admitted to III year of BE have to undergo mandatory internship of 4 weeks during the vacations of VI and VII semesters and /or VII and VIII semesters. A University examination will be conducted during VIII semester and prescribed credit are added to VIII semester. Internship is considered as a head of passing and is considered for the award of degree. Those, who do not take-up/complete the internship will be declared as failed and have to complete during subsequent University examination after satisfy the internship requirements

Note: : PC: Professional Core. PE: Professional Elective, OE: Open Elective. MC: Mandatory Course, PRJ: Project work, INT: Internship

Select **ANY ONE** of the Professional Elective. Open Elective-A: Students can select any one of the open electives (Please refer to consolidated list of Dr AIT for open electives) offered by any Department

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

Professional Elective-3(PE-3)		
Sl. No.	**Course Code**	**Course Title**
1	18EC731	5G Technology
2	18EC732	Virtual Reality
3	18EC733	Real Time Operating systems
4	18EC734	DSP Algorithm and architecture
5	18EC735	Network and Cyber Security
6	18EC736	Optical Fibre Communication

Professional Elective-4(PE-4)		
Sl. No.	**Course Code**	**Course Title**
1	18EC741	Analog and Mixed Mode VLSI
2	18EC742	Operating systems
3	18EC743	Satellite Communication
4	18EC744	Real Time Embedded Systems
5	18EC745	Operations Research
6	18EC746	Adaptive Signal Processing

Open Elective-C (OE-C)		
Sl. No	**Course Code**	**Course Title**
1	18EC751	Internet of Things (CS, IS, EI, TE, ML, ME, IEM, EEE, CV)
2	18EC752	Cryptography (CS, IS, ML,TE, EI,EEE)
3	18EC753	Mobile Communication (EI, EE, ML)
4	18EC754	Bio Mechatronics (CS, IS, EI, TE, ML, ME, IEM, EEE, CV)
5	18EC755	Introduction to Unmanned Aerial Vehicle (UAV) (CS,IS, EI, TE,ML, ME, IEM, EEE,CV)

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2022-23

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2019 Batch)

VIII Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing/ Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	MC	18HS81	Occupational and Safety and Health administration	CV	03	--	--	03	050	050	100	02
2	Project	18ECP81	Project Work Phase-2	EC	--	--	03	03	050	050	100	10
3	Seminar	18ECS82	Technical Seminar	EC	--	--	03	03	050	050	100	01
4	INT	18ECI83	Internship	EC	--	--	03	03	050	050	100	02
Total					**03**	**--**	**09**	**12**	**250**	**250**	**500**	**15**

Internship: Those, who have not pursued /completed the internship will be declared as failed and have to complete during subsequent SEE examination after they satisfy the internship requirements.

Note: : PC: Professional Core. PE: Professional Elective, OE: Open Elective. MC: Mandatory Course, PRJ: Project work, INT: Internship

Select **ANY ONE** of the Professional Elective and Open Elective subject

Students can select any one of the open electives (Please refer to consolidated list of Dr. AIT open electives) offered by any Department.
Selection of an open elective is not allowed provided,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of Departmental core courses or professional electives. Registration to electives shall be documented under the guidance of Programme Coordinator/ Mentor.

Sub Title: WIRELESS COMMUNICATION		
Sub Code:18EC71	**No. of Credits:4=4: 0: 0 (L-T-P)**	**No. of lecture hours/week: 4**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Understand the basics of wireless communication used for mobile telephony
2. Apply the basic methodologies of cellular system designing.
3. Describe the 3G network architecture and cellular network
4. Understand GSM and TDMA technologies and GSM Call establishment, Cal handoff and Roaming
5. Distinguish between CDMA technology, wireless LAN and PAN technologies

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	Introduction to wireless telecommunication systems and Networks, History and Evolution of wireless radio system, Development of modern telecommunication infrastructure, overview of existing Network infrastructure, Wireless Network applications, Future Wireless Network. Different generations of wireless cellular networks 1G, 2G,2.5G ,3G and 4G Cellular system and beyond, Wireless standard organizations. **TEXT 1**	10	L1,L2,L3.
2	Common Cellular System components, Common cellular network components, Hardware and software, views of cellular networks, 3G cellular systems components. Cellular component identification, Call establishment. **TEXT 1**	10	L1,L2,L3
3	Wireless network architecture and operation: The cellular concept Cell fundamentals, Capacity expansion techniques, Cellular backhaul networks, Mobility management, Radio resources and power management, Wireless network security.**TEXT1**	10	L1,L2,L3.
4	GSM and TDMA Technology: GSM system overview-introduction to GSM and TDMA,GSM Network and System Architecture, GSM channel concept, GSM system operations-GSM identities, GSM system operations (Traffic cases). **TEXT1**	11	L1,L2,L3,L4
5	CDMA Technology: CDMA system overview, introduction to CDMA,CDMA network and system architecture CDMA basics: CDMA Channel concept, CDMA operations(Layer 3) 3g CDMA,IS95B,CDMA 2000 and WCDMA Wireless LANs/IEEE 802.11X: Introduction and Evolution of Wireless LANs, Design issues.	11	L1,L2,L3,L4,L6

	Wireless PAN/IEEE 802.15x: Introduction, Wireless Pan application and Architecture. **TEXT1**		

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

Course Outcomes:

CO1: Understand and Identify the telecommunication system and networks system, Different generations of wireless cellular networks 1G, 2G,2.5G ,3G and 4G Cellular system and beyond, Wireless standard organizations.

CO2: Analyze Common Cellular System components, Common cellular network components, Hardware and software views of cellular networks.

CO3: Understand Wireless network architecture and operation, power management and network security and Capacity expansion techniques,.

CO4: Understand GSM and TDMA Technologies. GSM frame concept , GSM system operation registration, call setup, location updating, and call hand off procedure,

CO5: Analyze the design issues in CDMA, Wireless LAN and PAN Networks 3G cellular system components; list the components of wireless cellular network and different frequency band used in GSM and CDMA

COs	Mapping with POs
CO1	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12
CO2	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12
CO3	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12
CO4	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12
CO5	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12

Text Books.

1. Garry J Mullet, "Introduction to Telecommunication Systems and Networks: , India Edition, Delmar Cengage Learning,2007

Reference Text Books.

1. T L Singal, "Wireless Communications", Tata McGraw-Hill, Education, 2010
2. Vijay K Garg, "IS-95 CDMA and cdma2000: Cellular/PCS Systems Implementation", Pearson Education, reprint 2006

Web Links.

1. http://www.nptel.ac.in /courses/117102062/

SubTitle : Microwave and Antenna		
Sub Code: 18EC72	**No. of Credits:4=4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Understanding the basics of microwave and waveguides.
2. Understanding the concepts of microwave networks, microwave passive devices and semiconductor devices.
3. Understanding microwave tubes, microwave design principles and antenna basics.
4. Understanding the importance of point sources, arrays and radiations from wires.
5. To understand different types of antennas like aperture, reflector, broadband and Microstrip antennas.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction to Microwaves** -History of Microwaves, Microwave Frequency bands, applications of Microwaves, Losses associated with microwave transmission, Concept of Impedance in Microwave transmission. **Waveguides**-Rectangular waveguide, Introduction to Circular waveguide (No derivations and Numerical examples), Strip line, Micro strip line. **TEXT 1,2**	09	L1, L2, L3.
2	**Microwave Network Analysis** - Network parameters for microwave circuits, Scattering Parameters. **Microwave Passive devices and semiconductor Devices** - Microwave passive devices - Directional Coupler, Power Divider, Magic Tee, Attenuator, Resonator.Microwave Semiconductor Devices - Gunn Diodes, IMPATT diodes, PIN diodes**. TEXT 1,2**	09	L1, L2,L3
3	**Microwave Tubes:** Klystron- two cavity klystron amplifier and reflex klystron (klystron oscillator) **Antenna Basics** - Physical concept of radiation, near and far field regions, basic antenna parameters: radiation patterns, beam area, radiation Intensity, beam efficiency, reciprocity, directivity and gain, antenna apertures, effective height, bandwidth, radiation efficiency, radio communication Link and antenna field zones. **TEXT 1,2,3.4**	11	L1,L2,L3
4	**Radiations from wires:** Short electric dipole, fields of a short dipole, radiation resistance of dipole, Half wave dipole antenna, folded dipole antennas. **Point Sources & their arrays** - Arrays, Point source, Power theorem and its application, Examples of power patterns, Field patterns, Phase patterns, Array of isotropic point sources different cases, non-isotropic sources, principle of pattern multiplication, linear arrays of n elements of equal amplitude & spacing, broad side, end fire arrays **TEXT 3,4**	11	L1,L2,L3,L4
5	**Aperture and Reflector Antennas**- Huygens' principle, Babinet's principle, Radiation from sectoral and pyramidal horns, design concepts, prime-focus parabolic reflector and cassegrain antennas. **Broadband Antennas**- Log-periodic and Yagi-Uda antennas, frequency independent antennas, broadcast antennas. **Micro strip Antennas**- Basic characteristics of micro strip antennas, feeding methods **TEXT 3,4**	12	L1,L2,L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3. Unit 1- Digital Teaching and Learning

Course Outcomes: After the completion of the Course the student can:

CO1. Identify the microwave frequency band, its applications and different types of waveguides
CO2. Analyze microwave networks, microwave passive devices and semiconductor devices.
CO3. Apply microwave design principle, microwave tubes andantenna basics.
CO4. Be able to analyzethe radiation patterns from different types of wires, point sources and their arrays.
CO5. Illustrate and design antennas like aperture, reflector, and broadband. Microstrip antenna.

Cos	Mapping with POs	Mapping with PSOs
CO1	PO1,PO2,PO8,PO9	PSO1,PSO2,PS03
CO2	PO1,PO2,PO4,PO8,PO9,PO12	PSO1,PSO2,PS03
CO3	PO1,PO2,PO3,PO4,PO5,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03
CO4	PO1,PO2,PO3,PO4,PO5,PO6,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03
CO5	PO1,PO2,PO3,PO4,PO5,PO6,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03

Web Links:	
1.	www.nptel.in
2.	https://www.academia.edu/12559664/Collin_Foundations_for_Microwave_Engineering
3.	https://www.academia.edu/13759443/Basic_Antennas_Understanding_Practical_Antennas_and_Design_Joel_R_Hallas_2009
4.	www.youtube/microwave , www.youtube/antennas

Text Book:	
1.	Collin RE. **Foundations for microwave engineering**. John Wiley & Sons; 2007.
2.	Annapurna Das, Sisir K Das, **Microwave Engineering,** TMH Publication, 2001
3.	J.D. Kraus**, Antennas**, McGraw Hill, 1988.
4.	C.A. Balanis, **Antenna Theory** - Analysis and Design, John Wiley, 1982.

Reference Books:	
1.	Microwave Devices and circuits- Liao / Pearson Education. 1992
2.	M.Kulkarni., "Microwave devices and Radar Engg."Umesh Publications, 2011
3.	R.E. Collin, Antennas and Radio Wave Propagation, McGraw Hill, 1985.
4.	I.J. Bahl and P. Bhartia, Micro Strip Antennas, Artech House, 1980.

Sub Title: 5G Technology		
Sub Code:18EC731	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hrs	**CIE +Assignment+Group Activity + SEE = 40 + 5 +5+ 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Assess the genesis and impact of 5G and use case requirement in real world.
2. Understanding the 5G architecture and its deployment.
3 Understanding the security features in 5G technology..
4. Understanding the wireless spectrum crunch 5G technologies.
5. Analyzing and understanding SON and Green flexible RF in 5G technology.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**Drivers for 5G: The 'Pervasive Connected World'** Introduction, Historical Trend of Wireless Communications, Evolution of LTE Technology to Beyond 4G, 5G Roadmap, 10 Pillars of 5G, 5G in Europe, 5G in North America, 5G in Asia, 5G Architecture**Text1**	08	L1, L2, L3
2	**The 5G Internet Introduction,** Internet of Things and Context-Awareness, Internet of Things, Context-Awareness, Networking Reconfiguration and Virtualization Support, Software Defined Networking, Network Function Virtualization, Mobility, An Evolutionary Approach from the Current Internet, A Clean-Slate Approach, Quality of Service Control, Emerging Approach for Resource Over-Provisioning **.Text1**	08	L1, L2, L3
3	**Security for 5G Communications:** Introduction, Overview of a Potential 5G Communications, System Architecture, Security Issues and Challenges in 5G Communications Systems, User Equipment, Access Networks,, Mobile Operator's Core Network, External IP Networks **Text1**	08	L1, L2, L3
4	**The Wireless Spectrum Crunch: White Spaces for 5G?.** Introduction, Background, Early Spectrum Management, History of TV White Spaces, History of Radar White Spaces, TV White Space Technology, Standards, Approaches to White Space, White Space Spectrum Opportunities and Challenges, TV White Space Applications, International Efforts, Role of WS in 5G Text1	07	L1, L2, L3

5	**SON Evolution for 5G Mobile Networks,** Introduction, SON in UMTS and LTE, The Need for SON in 5G, Evolution towards Small-Cell Dominant HetNets, Towards a New SON Architecture for 5G, **Green Flexible RF for 5G:** Introduction, Radio System Design, Nonlinear Crosstalk in MIMO Systems **Text1**	08	L1, L2, L3

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5
3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 1 - Digital teaching and learning

Course Outcomes

CO1. Introduction to drivers in 5G technology.

CO2. Analyze the 5G architecture and its deployment.

CO3. Elaborate security features in 5G technology.

CO4. Analyze the role of wireless spectrum crunch 5G technologies.

CO5. Elaborate the SON and Green flexible RF in 5G technology.

COs	Mapping with POs
CO1	**PO1,PO2,PO8,PO12**
CO2	**PO1,PO3,PO8,PO12**
CO3	**PO1,PO6,PO8,PO12**
CO4	**PO1,PO3,PO8,PO12**
CO5	**PO1,PO2,PO8,PO12**

TEXT BOOKS:

1. **Jonathan Rodriguez**, "Fundamentals of 5G Mobile", Wiley Publications, 2015.

REFERENCE BOOKS/WEB LINKS:

1. **Afif Osseran, Jose F.Monserrat, Patrick Marsch,** " 5G Mobile and Wireless Communications Technology" Cambridge University Press, 2016
2. **Harri Holma, Antti Toskala, Takehiro Nakamura**, " 5G Technology: 3GPP New Radio", John Wiley & Sons Ltd. 2020

Subject Title : VIRTUAL REALITY		
Sub.Code: 18EC732	No. of Credits:03=03:0:0 (L - T – P)	No.ofLectureHours/Week:03
Exam Duration:03 Hrs	CIE+Assignment +SEE=45+5+50=100	Total No.of Contact Hours:39

Course Learning Objectives:

1 To become familiar with the basic concepts of virtual reality Technology and input devices

2 To understand the output devices.

3 TostudytheconceptsofModeling in virtual

4 To understand the human factors in VR

5 To become familiar with the applications of VR

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**INTRODUCTION:** Three I's of virtual reality, commercial VR technology, five classic components of a VR system. Input Devices: 3D position trackers: Tracker Performance Parameters, Ultrasonic Trackers, Optical Trackers, Hybrid Inertial Trackers Navigation and Manipulation interfaces: Tracker-Based Navigation/Manipulation Interfaces, Trackballs, 3D Probes. Gesture interfaces: Pinch Glove, 5DT Data Glove, Didji glove, Cyber Glove. **Text book1: 1.1, 1.3, 1.5, 2.1: 2.1.1, 2.1.4,2.1.5,2.1.6, 2.2: 2.2.1, 2.2.2,2.2.3 and 2.3:2.3.1, 2.3.2, 2.3.3,2.3.4**	09	L1,L2,L3.
2	**OUTPUT DEVICES**: Graphics displays: Human Visual System. Personal Graphics Displays: Head-Mounted, Hand-Supported, Floor-Supported and Desk Supported Displays. Large-Volume Displays: Monitor-Based, Large-Volume, and projector Based Displays. Sound displays: Human Auditory System, Convolvotron, Speaker-Based 3D Sound. Haptic feedback: Human Haptic System, Sensory-Motor Control. **Text book1: 3.1: 3.1.1,3.1.2, 3.1.3, 3.2: 3.2.1, 3.2.2, 3.2.3 and 3.3: 3.3.1, 3.3.1.**	07	L1,L2,L3,L4
3	**MODELING:** Geometric modeling: Virtual Object Shape, Kinematics modeling: Homogeneous Transformation Matrices, Physical modeling: Collision Detection, Behavior modeling, Model management: Cell Segmentation.	08	L1,L2, L3,L4

	Text book1: 5.1: 5.1.1, 5.2:5.2.1 and 5.3: 5.3.1, 5.4 and 5.5:5.5.2		
4	**HUMAN FACTORS:** Methodology and terminology: Data Collection and Analysis, Usability Engineering Methodology User performance studies: Testbed Evaluation of Universal VR Tasks. VR health and safety issues: Direct Effects of VR, Simulations on Users, Cyber sickness, Adaptation and Aftereffects, Guidelines for Proper VR Usage. **Text book1: 7.1:7.1.1,7.1.2, 7.2:7.2.1 and 7.3:7.3.1,7.3.2,7.3.3,7.3.4.**	07	L1,L2,L3.
5	**APPLICATIONS:** Medical applications, Education, arts, and entertainment, Military applications, Robotics applications. **Text book1: 8.1,8.2, 8.3 and 9.2**	08	L1,L2, L3

Note 1: Each Unit will have internal choice
Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Describe the basic concepts of virtual reality and input devices.
CO2 Compare the input and output devices
CO3 Use the virtual reality modeling techniques
CO4 Illustrate the human factors in virtual reality
CO5 Understanding and identifyingthe applications of virtual reality

Course Outcomes Mapping with Programme Outcomes.

CO1	PO1,PO2,PO4,PO5,PO8, PO12	PSO1,PSO2,PS03
CO2	PO2,PO3,PO4,PO5,PO10,PO12	PSO1,PSO2,PS03
CO3	PO1,PO2,PO3,PO5,PO6,PO7,PO12	PSO1,PSO2, PS03
CO4	PO1,PO2,PO4,PO5,PO11,PO12	PSO1,PSO2, PS03
CO5	PO1,PO2,PO5, PO11,PO12	PSO1,PSO2, PS03

Text Books.

1 Virtual Reality Technology, Second Edition, Gregory C. Burdea& Philippe Coiffet,

John Wiley & Sons. 2003
2 Introduction to Virtual Reality, John Vince, Springer, London, Springer-Verlag London Limited 2004

Reference Text Books.

1 Virtual Reality Systems. John Vince, Pearson Education, 2007

Web Links.

1 https://doi.org/10.1007/978-0-85729-386-2, 978-1-85233-739-1
2 www.nptelcoursematerial
3 www.youtube/virtual
4 Introduction - Learning Virtual Reality [Book] (oreilly.com)
5 https://www.geeksforgeeks.org/virtual-reality-introduction

Sub Title : **Real Time Operating System**		
Sub Code: 18EC733	**No. of Credits:3=3: 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. study the basic concepts of specialized processors
2. study the various Scheduling strategies
3. study multi-resource services
4. study the embedded system components
5. understand design trade-offs

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction to real-time embedded systems:** Brief history of real time systems, a brief history of embedded systems. **System Resources:** resource analysis, real-time service utility, scheduling classes, the cyclic executive, scheduler concepts, preemptive fixed priority scheduling policies, Real-Time OS, thread safe reentrant functions. Text1	08	L1,L2
2	**Processing**: preemptive fixed-priority policy, feasibility, rate monotonic least upper bound, necessary and sufficient feasibility, deadline – monotonic policy, dynamic priority policies. **I/O Resources**: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture. Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems. Text1	08	L1, L2, L3
3	**Multi-resource Services**: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion. Soft Real-Time Services: Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services. Text1	08	L1, L2
4	**Embedded system components**: firmware components, RTOS system software mechanisms, software application components. **Debugging components:** exceptions assert, checking return codes, single-step debugging, kernel scheduler traces, test access ports, trace ports, power-on self test and diagnostics, external test equipment, application-level debugging. Text1	08	L1, L2
5	**High availability and reliability design:** reliability and availability, similarities and differences, reliability, reliable software, available software, design trade- offs, hierarchical applications for fail-safe design. Text1	07	L1, L2

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3.Unit 4---digital teaching and learning.

Course Outcomes:

CO1: Understand the basics of Real Time Embedded System and System Resources

CO2: Analyse the concepts Processing and IO Resources

CO3: Analyse Various multi-resource services

CO4: Analyse different Embedded System Components and Debug components.

CO5: Analyze and Categorize the design trade-offs

Cos	Mapping with POs
CO1	PO1, PO2
CO2	PO2, PO6
CO3	PO2,PO6, PO10,P12
CO4	PO2,PO6, PO10,P12
CO5	PO2,PO6, PO10,P12

Text Book:	
1.	Sam Siewert, "**Real-Time Embedded Systems and Components**," Cengage Learning India Edition, **2007**.
2.	John Wiley, **"Programming for Embedded Systems"**, Dreamtech SoftwareTeam, India Pvt. Ltd.,2008.

Reference Books:	
1.	Raj Kamal, "**Embedded Systems**", Tata McGraw Hill, New Delhi, ***2008***.
2.	Phillip. A. Laplante, "**Real-Time Systems Design and Analysis**", Prentice Hall India,2nd Edition, ***2005***.
3	Jane. W. S. Liu, "**Real Time Systems**", Pearson Education, ***2005***

Sub Title : DSP Algorithms and Architecture		
Sub Code: 18EC734	**No. of Credits:3=3: 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To gain the knowledge of basics of DSP like DFT, FFT, LTI systems, Digital Filters.
2. To understand the architectures of DSP processors.
3. To study the implementation of DSP algorithms.
4. To understand the interfacing of DSP processors with memory and I/O devices.
5. To study the applications of DSP processor.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction to Digital Signal Processing:** Introduction, a Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **Architectures for Programmable Digital Signal Processors:** Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing. TEXT 1	09	L1,L2
2	**Programmable Digital Signal Processors:** Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54xx., Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On-Chip peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor. TEXT 1	08	L1, L2
3	**Implementation of Basic DSP Algorithms:** Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). TEXT 1	06	L2, L3,L4
4	**Implementation of FFT Algorithms:** Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit-Reversed Index Generation & Implementation on the TMS32OC54xx. **Interfacing Memory and Parallel I/O Peripherals to DSP Devices:** Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface,	10	L2, L3,L4

	Programmed I/O, Interrupts and I / O Direct Memory Access (DMA). TEXT 1		
5	**Interfacing and Applications of DSP Processor:** Introduction, Synchronous Serial Interface, A CODEC Interface Circuit. DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System. TEXT 1	06	L3,L4.L5

Note 1: Unit 1, Unit 2, Unit 3, Unit 4 and Unit 5 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5.

Course Outcomes:

CO1: Define the fundamentals of DSP and the general architecture of DSP

CO2: Understand the general architecture of DSP processor and in particular TMS320C54xx DSP to run algorithms.

CO3: Applying the concept of DSP algorithms.

CO4: Analyse the implementation of FFT algorithms and interfacing memory to DSP processor.

CO5: Creating new designs based on existing algorithms targeted to DSP processor.

Cos	**Mapping with POs**
CO1	PO2, PO3, PO4, PO5,PO11,PO12
CO2	PO2, PO3, PO4, PO5,PO11,PO12
CO3	PO2, PO3, PO4, PO5,PO11,PO12
CO4	PO2, PO3, PO4, PO5,PO11,PO12
CO5	PO2, PO3, PO4, PO5,PO11,PO12

Text Book:

1. Avatar Singh and S. Srinivasan, "Digital Signal Processing", Third Edition, Thomsoc Learning, 2004

Reference Books:

1. Ifeachor E. C., Jervis B. W Pearson-Education, "Digital Signal Processing: A Practical Approach", edition, Pearson Education, 2002
2. B Venkataramani and M Bhaskar, "Digital Signal Processors", 2nd edition, TMH, 2010
3 Peter Pirsch, "Architectures for Digital Signal Processing", 4th edition, John Wiley, 2007

Web Links:

1. http://bwrcs.eecs.berkeley.edu/Classes/CS252/Notes/Lec09-DSP.pdf
2. http://nptel.ac.in/courses/117102060/

Sub Title: **NETWORK AND CYBER SECURITY**		
Sub Code:18EC735	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Assignment+ Group Activity + SEE = 40 + 5 +5+ 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Know about security concerns in Email and Internet Protocol. ·
2. Understand cyber security concepts. ·
3. List the problems that can arise in cyber security. ·
4. Discuss the various cyber security frame work.
5. Will be in a position to apply the concepts of cyber security framework in computer system administration.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**Transport Level Security:** Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS, Secure Shell (SSH) Text 1:	08	L1, L2
2	**E-mail Security**: Pretty Good Privacy, S/MIME, Domain keys identified mail (Text1)	08	L1, L2
3	**IP Security**: IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP), Combining security Associations Internet Key Exchange. Cryptographic Suites (Text 1:)	08	L1, L2, L3
4	**Cyber network security concepts**: Security Architecture antipattern: signature based malware detection versus polymorphic threads, document driven certification and accreditation, policy driven security certifications. Refactored solution: reputational, behavioural and entropy based malware detection. The problems: cyber antipatterns concept, forces in cyber antipatterns, cyber anti pattern templates, cyber security antipattern catalog (Text-2)	07	L1, L2, L3
5	**Cyber network security concepts:** Enterprise security using Zachman framework Zachman framework for enterprise architecture, primitive models versus composite models, architectural problem solving patterns, enterprise workshop, matrix mining, mini patterns for problem solving meetings. (Text-2: Chapter 3 & 4).	08	L1, L2, L3

Note:

1. **Unit 1,2,3,4, and Unit 5 will have the internal choice**
2. **Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5**
3. **Group activity for a group of 4 or 5 students -5 marks**
4. **UNIT 1 - Digital teaching and learning**

Course Outcomes

CO1. Explain network security protocols ·

CO2. Understand the basic concepts of cyber security ·

CO3. Discuss the cyber security problems ·

CO4. Explain Enterprise Security Framework ·

CO5. Apply concept of cyber security framework in computer system administration.

COs	**Mapping with POs**
CO1	PO5,PO6
CO2	PO5,PO6
CO3	PO5,PO6,PO7,PO8,PO9
CO4	PO5,PO6,PO7,PO8,PO9
CO5	PO5,PO6,PO7,PO8,PO9

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325- 1877-3.
2. 2. Thomas J. Mowbray, "Cyber Security – Managing Systems, Conducting Testing, and Investigating Intrusions", Wiley.

REFERENCE BOOKS/WEB LINKS:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

Sub Title: Optical Fiber Communication		
Sub Code:18EC736	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand the basic concept of adaptive filter and adaptive system
2. Identify the geometrical significance of Eigenvectors and values
3. Analyse the Simple, Newton's and Steepest Descent Gradient search method to search performance surface
4. Study estimation of LMS algorithm
5. Familiar with design of adaptive communication system, adaptive noise canceller and adaptive modeling in FIR digital filter synthesis

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**OVERVIEW OF OPTICAL FIBER COMMUNICATION:** Introduction, Historical development, general system, advantages, disadvantages, and applications of optical fiber communication, optical fiber waveguides, Ray theory transmission: total internal reflection, acceptance angle, numerical aperture , skew rays, Cylindrical fiber: modes, mode coupling, step index fibers and graded index fibers, single mode fibers: cutoff wave length and mode filed diameter. **TEXT 1**	07	L1.L2.L3
2	**TRANSMISSION CHARACTERISTICS OF OPTICAL FIBERS:** Introduction, Attenuation, Material absorption: Intrinsic and extrinsic absorption, linear scattering losses: Rayleigh scattering and Mie scattering, Dispersion: Chromatic dispersion: Material and Waveguide dispersion, bending loss. . **TEXT 1**	07	L1.L2.L3,L4
3	**OPTICAL FIBERS AND CABLES:** Cable design: Fiber buffering, cable structural and strength members, cable sheath and water barrier, examples of fiber cables. **OPTICAL SOURCES AND DETECTORS: Laser** :Introduction, basic concepts: absorption and emission of radiation, population inversion. Optical emission from semiconductors: The p-n junction, spontaneous emission, carrier recombination, stimulated emission and lasing, heterojunctions, semiconductor materials. **LED:** Introduction, power & efficiency: double heterojuncation LED **Detectors:** Introduction, quantum efficiency, responsivity. Semiconductor photodiodes: p-i-n and Avalanche photodiode, Phototransistors, photoconductive detectors. **TEXT 1**	09	L1.L2.L3,L4
4	**DIGITAL TRANSMISSION SYSTEMS:** Point –to-point links: System considerations, Link power Budget, Rise Time Budget, First window transmission distance, Transmission distance	07	L1.L2.L3

	for single mode Links **TEXT 2**		
5	**OPTICAL NETWORKS:** Introduction, Optical networks concepts: Optical networking terminology, Optical network node and switching elements, Optical network transmission modes, layers and protocols: Synchronous networks, Asynchronous transfer mode, internet protocol, Optical network deployment: Long haul networks, Metropolitan area networks, Access networks, Local area networks. Optical Ethernet, Network protection, restoration and survivability. TEXT 1	09	L1.L2.L3

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

Course Outcomes

CO1	Describe the basic concepts of propagation of optical energy in single and multimode optical fibers.
CO2	Compare the fiber losses and its measurements to provide background for optical fiber communications.
CO3	Use the cable design and Identify the optical sources and detectors.
CO4	Illustrate the digital transmission system of optical fiber communication
CO5	Understanding and Identifying the different optical Networks and its communication.

COs	**Mapping with POs**
CO1	PO1,PO2,PO4, PO12
CO2	PO2,PO3,PO4,PO10,PO12
CO3	PO1,PO2,PO3,PO6,PO7,PO12
CO4	PO1,PO2,PO4,PO11,PO12
CO5	PO1,PO2,PO11,PO12

Text Books.

1 John M. Senior, "**Optical Fiber Communications**", 3rd Impression Reprint v, Pearson Education, 2012

2 Gerd Keiser, "**Optical Fiber Communication**", 3rd Ed.,, MGH, Reprint, 2012

Reference Text Books.

1 Joseph C Palais, "**Fiber Optic Communication**", 4th Edition, Pearson Education, 2012

2 GowerJohn , "Optical Communication System", second edition, Prentice, 2013

Web Links.

1. www.google.com, Optical Fiber Communications", John M. Senior pdf
2. www.google.com, optical fiber communication gerd keiser 4th edition pdf
3. www.nptelcoursematerial
4. Nptel.ac.in/lectures/courses/117101002
5. www.youtube/opticalfibercommunication

Sub Title : Analog and Mixed Mode VLSI Design		
Sub Code: 18EC741	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand the concept of Analog Design.
2. Analysis of Single stage amplifiers in VLSI perspective.
3. Analysis of Current sources and sinks in VLSI perspective.
4. Understand the concept of Data Converter Fundamentals.
5. Design and Mismatch Error Analysis of DAC and ADC Architectures.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Basic MOS Device Physics:** General considerations: MOSFET as a Switch, MOSFET Structure, MOS symbols, MOS I/V Characteristics: Threshold Voltage, Derivation of I/V Characteristics, Second Order Effects, MOS Device Models: MOS Device Layout, capacitances, MOS Small-signal Model, NMOS versus PMOS devices, Long-channel vs Short-channel devices.**(Text 1)**	09	L1,L2,L3
2	**Single Stage Amplifiers:** Basic Concepts, Common source stage, Common Source stage with resistive load, Common Source stage with Diode connected load, Common Source Stage with Current Source load, Common Source stage with Triode load, Common Source stage with source degeneration. **(Text 1)**	07	L1, L2,L3
3	**Current Sources and Sinks:** The current mirror, The Cascade Connection, Sensitivity Analysis, Transient response, other current sources & sinks. **(Text 1, 2)**	07	L2,L3,L4
4	**Data Converter Fundamentals:** Analog versus Digital discrete time signals, Converting Analog signals to Digital signals, Sample and Hold Characteristics, DAC specifications, ADC specifications, Mixed signal layout issues. **(Text 2)**	07	L2,L3,L4
5	**Data Converter Architectures:** DAC architecture, Digital input code, Resistors string, R-2R ladder networks, Current steering, Charge scaling DACs, Cyclic DAC, Pipeline DAC. **ADC Architecture:** Flash, 2-step flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC. **(Text 2)**	09	L2,L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
CO2. Ability to Analyse and Design of Single Stage Amplifiers.
CO3. Ability to Analyse and Design of Current sources and sinks.
CO4. Understand concepts of ADC and DAC
CO5. Analysis of ADC, DAC Architectures and Mismatch errors.

Cos	Mapping with POs
CO1	PO3, PO4
CO2	PO4, PO5
CO3	PO5, PO7
CO4	PO10, PO12
CO5	PO3, PO12

Text Book:	
1.	Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Twenty Fifth Reprint, TATA McGraw Hill, 2013.
2.	R Jacob Baker, "CMOS Circuit Design, Layout and Simulation", PHI, 2005.

Reference Books:	
1.	Philip E Allen and Douglas R Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2004.
2.	Adel Sedra and K C Smith, "Microelectronics Circuits", Fifth edition, Oxford University Press, 2009.

Web Links:	
1.	http://nptel.ac.in

Sub Title: Operating System		
Sub Code:18EC742	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand the history and types of operating systems.
2. Understand the design issues associated with operating systems development.
3. Understand the process management and scheduling.
4. Understand the concepts of memory management.
5. Understand the file and I/O operation

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**INTRODUCTION :** Goals of an O.S, Operation of an O.S **OVERVIEW OF OPERATING SYSTEMS:**, OS and computer system, Efficiency, system performance and user convenience, Classes of operating systems, O.S and the computer system, Batch processing system, Multi programming systems, Time sharing systems, Real time operating systems. TEXT 1 .	10	L1,L2
2	**STRUCTURE OF THE OPERATING SYSTEMS:** Operation of an O.S, Structure of an operating system, Operating systems with monolithic structure, Layered design of an operating system, Virtual machine operating systems, Kernel based operating systems. TEXT1	10	L1,L2.L3
3	**PROCESS MANAGEMENT:** Process and programs, Programmer view of processes, OS view of processes, Threads. **SHEDULING:** Preliminaries, Non pre-emptive scheduling policies, pre-emptive scheduling policies, scheduling in practice. TEXT 1	11	L1,L2,L3.
4	**MEMORY MANAGEMENT:** Managing the memory hierarchy, static and dynamic memory allocations, memory allocation to a process, reuse of memory, contiguous and non contiguous memory allocation, paging, segmentation, segmentation with paging. **VIRTUAL MEMORY:** Virtual memory Basics, Demand paging, page replacement policies. TEXT 1	11	L1,L2
5	**FILE SYSTEMS:** File system and IOCS, Files and file	10	L1,L2

	organization, Fundamentals of file organizations, Directory structures, File protection, Interface between file system and IOCS, Allocation of disk space. implementation of file access. TEXT 1		

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

Course Outcomes:

CO1: Understand the evolution of operating systems and various types of operating systems in practice

CO2: Analyze the structure of operating system.

CO3: Analyze the concepts of process management and different scheduling management.

CO4: Understand the design issues in memory management and virtual meamory.

CO5: Understand the file and I/O management techniques

COs	Mapping with POs
CO1	PO1,PO2,PO4, PO12
CO2	PO2,PO3,PO4,PO10,PO12
CO3	PO1,PO2,PO3,PO6,PO7,PO12
CO4	PO1,PO2,PO4,PO11,PO12
CO5	PO1,PO2,PO11,PO12

Text Books.

D.M.Dhamdhare, "**Operating Systems**", Second Edition, TMH, 2008

Reference Text Books.

1. Stalling William, "Operating Systems", Sixth edition, Pearson Education,
2. Avi Silberchatz, Peter Baer Galvin, Greg Gagne, "Operating system Concepts", Ninth edition, John wiley & Sons

Web Links.

1. faculty.salina.k-state.edu/tim/ossg/Introduction/OSrole.html
2. https://users.dimi.uniud.it/~antonio.dangelo/OpSys/.../Operating_System_Concepts.pdf

Sub Title: SATELLITE COMMUNICATION		
Sub Code:18EC743	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To be able to familiar with satellite systems and laws governing satellite orbit.
2. To understand concept of geostationary orbit and various losses on signal transmission in satellite system.
3. To evaluate link power budget estimation, System noise and various space segment subsystems.
4. To study earth segment, interference between satellite circuits and multiple access systems
5. To understand Direct Broadcast System, Satellite mobile and specialized services.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**OVER VIEW OF SATELLITE SYSTEMS:** Introduction, frequency allocation, INTELSAT , Orbits and launching methods : Kepler's laws, definitions of terms for earth orbiting satellites. Orbital element, apogee and perigee heights, orbit perturbations, inclined orbits, calendars, universal time, sidereal time, orbital plane, local mean time and sun synchronous orbits. Numerical problems. **Text 1, Ref 1**	10	L1, L2
2	**GEOSTATIONARY ORBIT:** Introduction, antenna, look angles, polar mount antenna, Limits of visibility, earth eclipse of satellite, sun transit outage, launching orbits. Numerical problems. **Text 1 , Ref. 1**	06	L1,L2
3	**SPACE SEGMENT:** Introduction, power supply unit, attitude control: spinning satellite stabilization, momentum wheel stabilization. Station keeping, thermal control, TT&C subsystem, transponders. **SPACE LINK:** Introduction, EIRP, transmission losses: free space transmission, feeder losses, and antenna misalignment losses. Link power budget equation, System noise: antenna noise, amplifier noise temperature, overall system noise temperature. **Text 1, Ref. 2**	08	L1,L2,L3
4	**EARTH SEGEMENT:** Introduction, receive only home TV system: out-door unit, indoor unit, MATV, CATV, Tx – Rx earth station. **Text 1** **INTERFERENCE AND SATELLITE ACCESS:** Introduction, interference between satellite circuits. S**atellite access**: single access, Pre-assigned FDMA, demand assigned FDMA, spade system, TDMA: pre-assigned TDMA, **Text 1**	10	L2,,L3
5	**SATELLITE SERVICES:** satellite mobile services, VSAT, RadarSat, Global positioning satellite system, orbcomm. **Text 1**	05	L1,L2,L3

Note:

1. **Unit 1,2,3,4, and Unit 5 will have the internal choice**
2. **Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5**

Course Outcomes:

CO1: Identify the characteristics of satellite communication Orbits, Launching Methods and channels.

CO2: Explain the concept of geostationary orbit and mathematical model for various losses on signal transmission in satellite system.

CO3: Apply analytical and empirical models in the design of satellite networks and space segments. Able to compute link power budget estimation, System noise

CO4: Illustrate the multiple access schemes for satellite access.

CO5: Compile the Direct Broadcast System, satellite mobile and specialized services

COs	Mapping with POs
CO1	PO1,PO2
CO2	PO1,PO2,PO6
CO3	PO2,PO6,PO12
CO4	PO2,PO6,PO12
CO5	PO2,PO6,PO12

Text Books.

1. Dennis Roddy, "Satellite Communications",4th Edition, McGraw- Hill International edition, 2006,

Reference Text Books.

1. Timothy Pratt, Charles Bostian and Jeremy Allnutt, "Satellite Communications", 2nd Edition, John Wiley Pvt. Ltd & Sons, 2008.Pearson Education Asia / PHI, Indian Reprint, 1997.
2. W. L. Pitchand, H. L. Suyderhoud, R. A. Nelson. , "'Communication Systems"", 2nd Edition, Pearson Education , 2007

Web Links.

1. https://www.amazon.com/Satellite-Communications-2nd-Dennis-Roddy/.../00705337...
2. https://www.flipkart.com/satellite-communications-2nd/p/itme9z9vfzvc9gea

Sub Title: Real Time Embedded Systems		
Sub Code:18EC744	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Introduce the fundamental concepts of the Real time Embedded systems.
2. Study concepts relating to Real time Embedded systems such as Scheduling techniques, Dynamic priority policies.
3. Describe concepts related to Multi resource services like blocking, Deadlock, live lock & soft real time services.
4. Understand the basic hardware and software components of Real time embedded systems.
5. Expose to Real time embedded system applications through different case studies.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**Real-Time Embedded Systems:** Introduction, Brief history of Real Time Systems, A brief history of Embedded Systems. **System Resources:** Introduction, Resource analysis, Real-Time Service Utility, scheduling classes, Scheduler concepts, Real-Time OS. (Text 1)	07	L1,L2, L3,
2	**Processing with Real Time Scheduling:** Introduction, Pre-emptive Fixed Priority Scheduling Policies with timing diagrams, Problems and issues, Feasibility, Rate Monotonic least upper bound (No derivation), Necessary and Sufficient feasibility, Dynamic priority policies. (Text 1)	08	L1,L2, L3
3	**I/O Resources**: Execution efficiency, I/O Architecture. **Memory:** Physical hierarchy, ECC Memory, **Multi-resource Services:** Blocking, Deadlock and livelock. **Soft real-time services:** Missed deadline, QoS. (Text 1)	08	L1,L2, L3
4	**Embedded System Components:** HARDWARE COMPONENTS: Sensors, Actuators, IO Interfaces, Processor Complex or SoC, Processor and IO Interconnection, Bus Interconnection, High-Speed Serial Interconnection, Low-Speed Serial Interconnection, Interconnection Systems, Memory Subsystems. FIRMWARE COMPONENTS: Boot Code, Device Drivers, Operating System Services. (Text 1)	08	L1,L2, L3, L4,L5

5	**Case Studies:** ROBOTIC APPLICATIONS: Robotic Arm, Actuation, End Effector Path, Sensing, Tasking, Automation and Autonomy. COMPUTER VISION APPLICATIONS: Object Tracking, Image Processing for Object Recognition, Characterizing Cameras, Pixel and Servo Coordinates, Stereo-Vision. (Text 1)	08	L1,L2, L3,L6

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

Course Outcomes:

CO1: Discuss the fundamentals of various real time services, real time service utilities, and Real time embedded system.

CO2: Apply priority based static and dynamic Real time scheduling techniques for the given real time embedded system specifications.

CO3: Analyze deadlock conditions, shared memory problem, priority inversion, missed deadlines and QoS of Real time embedded systems.

CO4: Choose the appropriate real time embedded system components to improve the performance.

CO5: Develop the simple real time embedded systems.

COs	**Mapping with POs**
CO1	PO1, PO2, PO6, PO12
CO2	PO1, PO2, PO4, PO5, PO12
CO3	PO1, PO2, PO6, PO12
CO4	PO1, PO2, PO5, PO6, PO12
CO5	PO1, PO2, PO6, PO12

Text Books.

"**Real-Time Embedded Components and Systems",** Sam Siewert, John Pratt, Mercury Learning and Information, 2016.

REFERENCE BOOKS/WEBLINKS

1. James W S Liu, "**Real Time System**", Pearson education, 2008.
2. nptel.ac.in/courses

Sub Title : OPERATIONS RESEARCH		
Sub Code: 18EC745	**No. of Credits: 3 = 3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration: 3 Hours	**CIE +Assignment + SEE = 45 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course Learning Objectives: This course will enable students to:

1. To be able to understand Scope of Operations Research and TP Formulation
2. To be able to understand the Assignment Problem.
3. To be able to understand the Network Construction
4. To be able to classify the type Game Theory
5. To be able to understand the Queuing system and their characteristics

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction to Operations Research:** Basics definition, scope, objectives, phases, models and limitations of Operations Research. Transportation Problem: Formulation, solution, unbalanced Transportation problem. Finding basic feasible solutions – Northwest corner rule, least cost method and Vogel's approximation method. Optimality test.**Text1**	8	L1, L2, L3.L4
2	**Assignment model:** Formulation. Hungarian method for optimal solution. Solving unbalanced problem. Traveling salesman problem and assignment problem. **Text1**	8	L1, L2, L3.L4
3	**PERT-CPM Techniques:** Network construction, determining critical path, floats, scheduling by network, project duration, variance under probabilistic models, prediction of date of completion, crashing of simple networks. **Text1**	8	L1, L2, L3.L4
4	**Game Theory:** Formulation of games, Two person-Zero sum game, games with and without saddle point, Graphical solution (2x n, m x 2 game). **Text1**	8	L1, L2, L3.L4
5	**Queuing Theory:** Queuing system and their characteristics. The M/M/1 Queuing system, Steady state performance analyzing of M/M/ 1 and M/M/C queuing model. **Text1**	7	L1,L2,L3

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

***Course Outcomes**: The student shall be able to*

CO1: Identify the OR Definitions and Able to apply TP.

CO2. Ability to interpret and explain the Assignment Problem.

CO3. Creation of Network construction, determining critical path, floats and scheduling by network

CO4. Ability to Compare the type of 2x n, m x 2 game.

CO5. Design the Queuing system, Game Theory and their characteristics.

CO's	**Mapping with POs**	**Mapping with PSOs**
CO1	PO1,PO2,PO3,PO8,PO9,PO10	PSO1,PSO2,PS03
CO2	PO1,PO2,PO3,PO8,PO9,PO10	PSO1,PSO2,PS03
CO3	PO1,PO2,PO3,PO8,PO9,PO10	PSO1,PSO2, PS03
CO4	PO1,PO2,PO3,PO8,PO9,PO10	PSO1,PSO2, PS03
CO5	PO1,PO2,PO3,PO8,PO9,PO10	PSO1,PSO2,PS03

Text Book:	
1.	P. Sankara Iyer, "**Operations Research**", First Edition, Tata McGraw-Hill, ***2008***
2.	A.M. Natarajan, P. Balasubramani, A. Tamilarasi, "**Operations Research**", First Edition, Pearson Education, ***2005***

Reference Books:	
1.	P. K. Gupta and D. S. Hira, "**Operations Research**", Second Edition, S. Chand & co, ***2007***
2.	S D Sharma, "**Operations Research, Problems and Solutions**", Paperback 1, kedar Nath Publisher, India Ltd, ***2012***

Sub Title : **Adaptive Signal Processing**		
Sub Code: 18EC746	**No. of Credits:3=3: 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. understand the basic concept of adaptive filter and adaptive system
2. identify the geometrical significance of Eigenvectors and values
3. analyse the Simple, Newton's and Steepest Descent Gradient search method to search performance surface
4. study estimation of LMS algorithm
5. familiar with design of adaptive communication system, adaptive noise canceller and adaptive modeling in FIR digital filter synthesis

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**ADAPTIVE SYSTEMS:** Definition and characteristics, Areas of application, General properties, Open-and closed loop adaptation, Applications of closed-loop adaptation, Example of an adaptive system. (Text1)	6	L1,L2
2	**THE ADAPTIVE LINEAR COMBINER:** General description, Input signal and weight vectors, Desired response and error, the performance function, gradient and minimum mean-square error, Example of a performance surface **PROPERTIES OF THE QUADRATIC PERFORMANCE SURFACE**: Normal of the input correlation matrix, Eigen values and Eigen vectors of the input correlation matrix, an example with two weights, geometrical significance of eigenvectors and Eigen values.(Text1)	10	L1,L2,L3
3	**SEARCHING THE PERFORMANCE SURFACE:** Methods of searching the performance surface, Basic ideal of gradient search methods, a simple gradient search algorithm and its solution, Stability and rate of convergence, The learning curve, and Gradient search by Newton's method in multidimensional space, Gradient search by the method of steepest descent, Comparison of learning curves. (Text1)	10	L1,L2,L3
4	**THE LMS ALGORITHM**: Derivation of the LMS algorithm, convergence of the weight vector, an example of convergence, learning curve, noise in the weight-vector solution(Text1)	7	L1,L2,L3
5	**ADAPTIVE MODELING AND SYSTEM IDENTIFICATION:** Multipath communication channel, geophysical exploration, FIR digital filter synthesis. (Text1)	6	L1,L2

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3.Unit 4---digital teaching and learning.

Course Outcomes:

CO1: Understand the basic concept of adaptive filter and adaptive system

CO2: Understand the design of adaptive linear combiner and Identify the geometrical significance of Eigenvectors and values

CO3: Analyse the Simple, Newton's and Steepest descent Gradient search method to search performance surface.

CO4: Estimate the gradient component using Newton's, Steepest-descent methods and LMS algorithm

CO5: Design of adaptive communication system, adaptive noise canceller and adaptive modelling in FIR digital filter synthesis.

Cos	Mapping with POs
CO1	PO1, PO2, PO3, PO4
CO2	PO1, PO2, PO3, PO4
CO3	PO2, PO3, PO4
CO4	PO2, PO3, PO4
CO5	PO5,PO6

Text Book:

1. **Bernard Widrow and Samuel D. Stearns, "Adaptive Signal Processing", Edition, Pearson Education, Asia, 2009**
2. **Simon Haykin, "Adaptive filter Theory", 4th edition, Pearson Education Asia, 2008**

Reference Books:

1. **Alexander, Thomas S, "Adaptive Signal Processing: Theory and Applications", edition, Springer-Verlag New York, Inc. New York, NY, USA, 1986**
2. **T. Adali and Simon Haykin, "Adaptive Signal Processing: Next Generation Solutions", edition, Wiley India, 2012**
3. **Jophn R. Treichler C. Richard Johnson, Jr. and Michael G. Larimore, "Theory and Design of Adaptive Filters", edition, PHI, 2002**

Web Links.

http://www.nptelvideos.in/2012/12/adaptive-signal-processing.html
http://www.cs.tut.fi/~tabus/course/ASP/Lectures_ASP.html
http://www.signal.uu.se/Courses/CourseDirs/AdaptSignTF/Adapt04. html

Active learning Assignments (AL) : Preparation of power-point slides, which include videos, animations, pictures, graphics for better understanding theory and practical work – The faculty will allocate chapters/ parts of chapters to groups of students so that the entire syllabus to be covered. The power-point slides should be put up on the web-site of the College/ Institute, along with the names of the students of the group, the name of the faculty, Department and College on the first slide. The best three works should submit to ECE Department, Dr. AIT.

Sub Title : Internet of Things		
Sub Code: 18EC751	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE =40+ 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Assess the genesis and impact of IoT applications, architectures in real world.
2. Illustrate diverse methods of deploying smart objects and connect them to network.
3. Understanding IP as the IoT Network Layer.
4. Compare different Application protocols for IoT.
5. Infer the role of Data Analytics.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	What is IoT, Genesis of IoT, IoT and Digitization,IoT Impact, Convergence of IT and IoT, IoT Challenges, IoT Network Architecture and Design, Drivers Behind New Network Architectures, Comparing IoT Architectures, A Simplified IoT Architecture, The Core IoT Functional Stack, IoT Data Management and Compute Stack. TEXT-1	09	L1, L2, L3
2	Smart Objects: The "Things" in IoT, Sensors, Actuators, and Smart Objects, Sensor Networks, Connecting Smart Objects, Communications Criteria, IoT Access Technologies. TEXT 1	10	L1,L2,L3
3	IP as the IoT Network Layer, The Business Case for IP, The need for Optimization, Optimizing IP for IoT, Profiles and Compliances TEXT 1	06	L1,L2,L3,L4
4	Application Protocols for IoT, The Transport Layer, IoT Application Transport Methods. TEXT 1	06	L1,L2,L3,L4
5	Data and Analytics for IoT, An Introduction to Data Analytics for IoT, Machine Learning, Big Data Analytics Tools and Technology, Edge Streaming Analytics, Network Analytics, TEXT 1	08	L1,L2,L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Each Unit will have assignments that are evaluated for 5 marks.

Note 3.Unit 2 taught through Digital Learning.

Course Outcomes:

CO1. Interpret the impact and challenges posed by IoT networks leading to new architectural models.
CO2. Compare and contrast the deployment of smart objects and the technologies to connect them to network.
CO3. Appraise the role of IoT protocols for efficient network communication.
CO4. Analyse higher layer IoT Protocols.
CO5. Elaborate the need for Data Analytics

Cos	Mapping with POs

CO1	PO6
CO2	PO6
CO3	PO6
CO4	PO6, PO12
CO5	PO6, PO12

Text Book:	
1.	**David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry**,"IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things", 1st Edition, Pearson Education (Cisco Press Indian Reprint).

Reference Books:	
1.	**Srinivasa K G**, "Internet of Things",CENGAGE Leaning India, 2017
2.	**Vijay Madisetti and ArshdeepBahga**, "Internet of Things (A Hands-on-Approach)", 1st Edition, VPT, 2014. (ISBN: 978-8173719547)
3.	**Raj Kamal,** "Internet of Things: Architecture and Design Principles", 1st Edition, McGraw Hill Education, 2017. (ISBN: 978-9352605224)

Web Links:	
1.	https://swayam.gov.in/nd1_noc20_cs22
2.	*www.tutorialspoint.com › internet_of_things › internet...*

Sub Title: Cryptography		
Sub Code:18EC752	**No. of Credits:03=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 03**
Exam Duration: 3 hours	**CIE +Assignment + Group Activity + SEE = 40 + 5 +5+ 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To impart the basic concepts of network security and classical encryption, number theory, stream ciphers, block ciphers and authentication
2. To interpret the cryptographic algorithms like stream ciphers and block ciphers using classical encryption techniques
3. To apply the concept of classical encryption techniques to stream ciphers and block ciphers
4. To analyse the stream ciphers, block ciphers and authentication functions
5. To design the stream ciphers, block ciphers and authentication functions

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**Introduction:** Services, mechanisms and attacks, OSI security architecture, Model for network security. **Symmetric ciphers:** Symmetric Cipher Model, Substitution Techniques: Caesar Cipher, Mono Alphabetic Cipher, Playfair Cipher, Hill Cipher, polyalphabetic Cipher and One-Time Pad (OTP). Transposition Techniques, Rotor Machines, Steganography. TEXT 1 and TEXT 1	08	L1,L2
2	**Finite Fields:** Groups, Rings, Fields. Modular Arithmetic: Divisors, properties of modulo operator, modular arithmetic operations and properties. Euclid's Algorithm, Greatest Common Divisor (GCD), finding GCD. Finite Fields of the form GF (p): Finite fields of order p, finding multiplicative inverse in GF (p). TEXT 1	08	L1,L2
3	**Private Key Encryption:** Simplified DES, Block Cipher Principles, Data encryption standard (DES), Strength of DES, Block Cipher Design Principles and Block Cipher Modes of Operation, Evaluation Criteria for Advanced Encryption Standard, The AES Cipher. TEXT 1	08	L2,L3,L4
4	**Public Key Encryption:** Principles of Public-Key Cryptosystems, The RSA algorithm. Key Management, Diffie - Hellman Key Exchange. TEXT 1	07	L2,L3,L4
5	**Authentication Functions and Hash Functions:** Authentication functions, message authentication codes, hash functions, security of Hash functions and MACs. TEXT 1	08	L2,L3,L4

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 5 - Digital teaching and learning

Course Outcomes	
CO1	Define the basic concepts of network security, classical encryption, number theory, Private key, public key, authentication
CO2	Understand the structure of cryptographic algorithms and their applications.
CO3	Apply the concept of classical encryption techniques to existing standard algorithms.
CO4	Illustrate the significance of cryptographic algorithms and their applications.
CO5	Design the private key and public key, authentication functions for applications.

COs	**Mapping with POs**
CO1	PO1,PO2, PO4, PO6, PO8, P12
CO1	PO1,PO2, PO4, PO6, PO8, P12
CO2	PO1,PO2, PO4, PO6, PO8, P12
CO3	PO1,PO2, PO3,PO4, PO6, PO8, P12
CO4	PO1,PO2, PO3,PO4, PO6, PO8, P12
CO5	PO1,PO2, PO4, PO6, PO8, P12

Text Books:

1. William Stallings, "Cryptography and Network Security: Principles and Practice", Fifth Edition, Pearson, 2010

Reference Books:

1. Behrouz Forouzan, "Cryptography and Network Security", edition, TMH, 2007
2. Alfred J. Menezes, Paul C. Van Oorschot and Scott A. Vanstone, "Handbook of Applied Cryptography ", edition, CRC Press, Reprint 2001
3. Bruce Scheiner, "Applied cryptography: protocols, algorithms, and source code in C", 2nd edition, Wley India, 2008
4. Atul Kahate , "Cryptography and Network Security", 2nd edition, TMH, 2006

Web Links:

1. http://www.nptel.ac.in/courses/106105031/

Sub Title: Mobile Communication		
Sub Code:18EC753	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Assignment +Group Activity+ SEE = 40 + 5 +5+ 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Able to understand the basics of wireless communication used for mobile telephony.
2. Able to understand basic methodologies of cellular system design ·
3. Able to remember components and characteristics of 2.5G network, 3G network architecture. Discuss the various cyber security frame work.
4. Able to understand Spread Spectrum communication and CDMA technology.
5. Able to remember characteristics of emerging wireless technologies.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	Evolution of wireless communication system: History of wireless communication, advantages and disadvantages of wireless communications ,wireless network generations, comparison of wireless systems, evolution to next generation networks, application of wireless communications, potential market areas. TEXT 1	08	L1, L2
2	Principles of cellular Communication: Cellular terminologies, cell structure and cluster, frequency reuse concept, cluster size and system capacity method of locating co channel cells, frequency reuse distance, co- channel interference and reduction methods, A Basic Cellular system: Limitations of conventional mobile telephone system, TEXT 1	08	L1, L2
3	Global System for Mobile(GSM):GSM Network architecture, Signalling protocol Architecture, identifies in GSM system, GSM channels, frame structure, speech coding, authentication and security in GSM, services, TEXT1	08	L1, L2, L3
4	CDMA digital cellular standards (IS 95): General model of Spread spectrum digital communication system, Direct sequence Spread Spectrum, Frequency hopping Spread Spectrum, Architecture of CDMA system. 3G Digital cellular Technology: 2.5G TDMA evolution, GPRS Technology, EDGE Technology, UMTS Technology-CDMA: Comparison of W-CDMA and IS 95.TEXT1	07	L1, L2, L3
5	Emerging wireless Network Technologies: IEEE.802.11 technology, ETSI Hyper LAN Technology, IEEE.802.15 WPAN technology, IEEE.802.16 WMAN technology, Mobile AD-HOC network(MANETS), Wireless Sensor Networks (WSNs), Security	08	L1, L2, L3

	requirements of wireless Networks, IEEE.802.21 standard-An overview, Interoperability of Wireless Networks.TEXT1		

Note:

1. **Unit 1,2,3,4, and Unit 5 will have the internal choice**
2. **Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5**
3. **Group activity for a group of 4 or 5 students -5 marks**
4. **UNIT 1 - Digital teaching and learning**

Course Outcomes

CO1. Identify the telecommunication system and networks system, 3G cellular system components; list the components of wireless cellular network and different frequency band used in GSM and CDMA

CO2. Explain cellular systems, list the characteristics of 3G wireless mobile systems and network security ·

CO3. Explain the architecture of 3G and network Systems and the operation needed for call setup and call release in GSM and TDMA system and concept of CDMA,

CO4. Illustrate the cellular concept, cell sectoring and cell splitting, mobility management, CDMA channel concept, GSM frame concept

CO5. Discuss characteristics of Emerging wireless Network Technologies

COs	**Mapping with POs**
CO1	PO2,PO5,PO12
CO2	PO2,PO5,PO12
CO3	PO2,PO5,PO12
CO4	PO2,PO5,PO12
CO5	PO2,PO5,PO12

TEXT BOOKS:

1. T L Singal, "Wireless Communications: , Tata McGraw-Hill Education , Delmar Cengage Learning,2010.

REFERENCE BOOKS/WEB LINKS:

1. Garry J Mullet, "Introduction to Telecommunication Systems and Networks", India Edition, Delmar Cengage Learning, 2007

2. Upena Dalal, "Wireless communication", Oxford Higher Education, 6th impression,2013

Sub Title: BIO-MECHATRONICS		
Sub Code:18EC754	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Learn basic knowledge about Bio mechanics, Bio sensors and actuators, and bio- mechatronics devices.
2. Impart the bio assist devices.
3. Know the different types, bio imaging and processing.
4. Understand about bio mechatronics devices and their functions.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**Bio Mechanics : Cardiovascular biomechanics, Musculoskeletal and orthopedic biomechanics, human ergonomic, Rehabilitation Text1**	08	L1, L2
2	**Bio Sensors and Actuators : Introduction to Bio mechatronics, Electrodes - Types, - Measurement of blood pressure - Blood Gas analyzers: pH of blood, Smart actuators for biological applications Text1**	08	L1, L2
3	**Medical Measurements: Heart rate - Heart sound -Pulmonary function measurements -spirometer -finger-tip oximeter - ESR, GSR measurements Text1**	08	L1, L2, L3
4	**Wearable mechatronics devices: Wearable Artificial Kidney, Wireless capsule endoscope, Wearable Exoskeletal rehabilitation system, Wearable hand rehabilitation**	07	L1, L2, L3
5	**Sensory Assist Devices: Hearing aids – Implants, Optical Prosthetics, Visual Neuroprostheses – Sonar based systems, Respiratory aids, Tactile devices for visually challenged. Text1**	08	L1, L2, L3

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5
3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 1 - Digital teaching and learning

Course Outcomes

CO1. Demonstrate the basic knowledge about the Bio mechanics, Bio sensors and actuators, and bio- mechatronics devices.
CO2. Acquire the different bio imaging and processing.
CO3. Analyse the Signal processing with bio sensors and actuators.
CO4. Analyse modern medical measurement devices.
CO5. Understand the properties of bio assist devices.

COs	Mapping with POs
CO1	PO5,PO6
CO2	PO5,PO6
CO3	PO5,PO6,PO7,PO8,PO9
CO4	PO5,PO6,PO7,PO8,PO9
CO5	PO5,PO6,PO7,PO8,PO9

TEXT BOOKS:

1. Graham M. Brooker, "Introduction to Bio-Mechatronics", Sci Tech Publishing, 2012.

REFERENCE BOOKS/WEB LINKS:

1. Leslie Cromwell, Fred J. Weibell, Erich A. Pfeiffer, "Bio-Medical Instrumentation and Measurements", II edition, Pearson Education, 2009.
2. Raymond Tong Kaiyu . "Bio-mechatronics in Medicine and Healthcare" Pan Stanford Publishing, CRC Press, 2011

Sub Title: Introduction to Unmanned Aerial Vehicle (UAV)		
Sub Code: 18EC755	**No. of Credits: 3 = 3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 03**
Exam Duration: 3 Hours	**CIE +Assignment + SEE = 45 + 5 + 50 =100**	**Total No. of Contact Hours: 39**

Course objectives:

1. Understand the basic aviation history and UAV systems
2. Acquire the knowledge of basic aerodynamics, performance, stability and control.
3. Understand the mission and control of UAVs.
4. Understand the launch and recovery of UAVs.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction:** Aviation History and Overview of UAV systems. Classes and Missions of UAVs: Examples of UAV systems-very small, small, Medium and Large UAVs, Classes of UAV systems. Missions of UAV systems. Text 1	07	L1
2	**The Air Vehicle:** Basic Aerodynamics: Basic Aerodynamics equations, Aircraft polar, the real wing and Airplane, Induced drag, the boundary layer, Flapping wings. Total Air-Vehicle Drag Performance: Overview, Climbing flight, Range and Endurance – for propeller driven aircraft, range- a jet-propelled aircraft, Guiding Flight. Text 1	08	L2, L3
3	**Stability and Control:** Overview, Stability, longitudinal stability, lateral stability, dynamic stability, Aerodynamics control, pitch control, lateral control, Autopilots, sensor, controller, actuator, airframe control, inner and outer loops, Flight-Control Classification, Overall Modes of Operation, Sensors Supporting the Autopilot. Text 1	08	L2, L3
4	**Mission Planning and Control:** Overview, Physical configuration. Air Vehicle and Payload Control: Overview, Modes of control, Piloting the Air vehicle, Controlling the Payloads. Text 1	08	L2,L3
5	**Launch and Recovery:** UAV Launch Methods for Fixed-Wing Vehicles: Rail Launchers, Pneumatic Launchers, Hydraulic/Pneumatic Launchers. Recovery Systems: Conventional Landings, Vertical Net Systems, Parachute Recovery, Mid-Air Retrieval, Shipboard Recovery. Text 1	08	L1,L2

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1. Able to understand the UAV systems.

CO2. Able to interpret the mission planning and control of UAV.

CO3. Gain the knowledge of the basic aerodynamics and performance of UAVs

CO4. Capable of analysing the stability and control required for UAV.

CO5. Able to apply the knowledge for launch and recovery of UAVs.

Cos	**Mapping with POs**	**Mapping with PSOs**
CO1	PO1,PO2	PSO1,PSO2,PS03
CO2	PO1,PO2, PO3	PSO1,PSO2,PS03
CO3	PO1,PO2,PO3	PSO1,PSO2, PS03
CO4	PO1,PO2, PO3,PO6	PSO1,PSO2, PS03
CO5	PO1,PO2, PO3, PO6	PSO1,PSO2,PS03

Text Book:	
1.	Paul Gerin Fahlstrom , Thomas James Gleason, "Introduction To UAV Systems", 4th Edition, Wiley Publication, 2012 John Wiley & Sons, Ltd.

Reference Books:	
1.	Landen Rosen, "Unmanned Aerial Vehicle", Alpha Editions, 2015.
2.	Valavanis**,** K., Vachtsevanos, George J., Handbook of Unmanned Aerial Vehicles, Springer, 2015.

Web Links:	
1.	https://onlinecourses.nptel.ac.in/noc19_ae06/preview
2.	https://www.coursera.org/lecture/robotics-flight/unmanned-aerial-vehicles-V136S

Sub Title : Advanced Communication Lab		
Sub Code: 18ECL76	**No. of Credits: 01=0 : 0 : 1 (L-T-P)**	**No. of lecture hours/week: 02**
Exam Duration : 3 Hours	**CIE + SEE = 50 + 50 =100**	**Total No. of Contact Hours :30**

Course objectives:

1. Understand the circuit schematic and its working of ASK, FSK, PSK, DPSK and QPSK circuits.
2. Design and test of ASK, FSK, PSK, DPSK and QPSK circuits.
3. Analyzing various losses using OFC kit
4. Measurement of parameters like frequency, guide wavelength, power, VSWR and Attenuation.
5. Learn to measure directivity and gain of different antennas.
6. Demonstrate sampling theorem under different sampling conditions.

Experiment No	Laboratory Experiments	No of Hours	Blooms Taxonomy level.
Part A: Hardware Experiments			
1	ASK generation and detection using discrete components.	2	L1, L2, L3. L4
2	FSK generation and detection using discrete components.	2	L1, L2, L3. L4
3	PSK generation and detection using discrete components.	2	L1, L2, L3. L4
4	To prove sampling theorem, to study the effects of under sampling and oversampling.	2	L1, L2, L3. L4
5	DPSK generation and detection using kit.	2	L1, L2, L3. L4
6	QPSK generation and detection using kit	2	L1, L2, L3. L4
7	Establish Analog and Digital communication link using optical fiber and Measure the losses (coupling loss, bending loss, attenuation loss numerical aperture.)	2	L1, L2, L3. L4
8	Measurement of frequency, guide wavelength, power, VSWR and Attenuation in a microwave test bench.	2	L1, L2, L3. L4
9	Measurement of directivity and gain of micro strip patch antenna using printed dipole.	2	L1, L2, L3. L4
10	Measurement of directivity and gain of Yagi antenna (printed) using printed dipole.	3	L1, L2, L3. L4

Course Outcomes: After the completion of the Course the student are able to:

CO1. Understand the working of ASK, FSK, PSK, DPSK and QPSK circuits.
CO2. Design ASK, FSK, PSK, DPSK and QPSK circuits.
CO3. Analyse various losses using OFC kit and parameters like frequency, guide wavelength, power, VSWR and Attenuation.
CO4. Demonstrate the sampling theorem and measurement of antenna parameters.

Cos	Mapping with POs	Mapping with PSOs
CO1	PO1, Po4,PO8,Po12	PSO1,PSO2
CO2	PO1,PO2,PO3,PO4,PO8,PO12	PSO1,PSO2
CO3	PO1,PO2,PO3,PO4,PO5,Po5,PO12	PSO1,PSO2

Reference Books:	
1.	Digital Communication: Sam Shanmugam, WILEY INDIA,2008
2.	ANTENNA THEORY: ANALYSIS AND DESIGN, 3RD ED (With CD), John Wiley & Sons, 2009

Web Links:	
1.	www.nptel.in

Sub Title : COMPUTER COMMUNICATION NETWORK LAB		
Sub.Code: 18ECL77	**No. of Credits:01=0:0:1(L - T –P)**	**No. of Lecture Hours/Week : 03**
ExamDuration: 03Hrs	**CIE + SEE = 50 + 50 =100**	**Total No.of Contact Hours:13**

Course objectives:

1. students should be able to demonstrate the simulation of few protocols of data link layer and network layer.
2. students should be able to demonstrate the network communication between source and destination.
3. students should be able to demonstrate the detection and correction of error in data communication.
4. students should be able to demonstrate the data communication between the systems using different media.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	Write a C program to implement Bit Stuffing and deStuffing	03	L1,L6
2	Write a C program to simulate a character stuffing and destuffing for a given message.	03	L1,L6
3	Write a C program to compute a polynomial checksum for a given binary data frame	03	L1,L6
4	Write a C program to simulate a shortest path Algorithm.	03	L1,L6
5	Using TCP/IP Sockets, write a client-server program to make client to communicate with Server using socket programming techniques in python.	03	L1,L6
	PART-B		
6	**SERIAL COMMUNICATION USING** (i) RS232 (ii) MODEM COMMUNICATION (iii) FIBER OPTIC COMMUNICATION	03	L4,L5
7	**Configuring and Verifying LAYER 2 Switches:** Establish a communication between the HOSTS by connecting the Network Devices as given below, configure them and verify the same. Configuration includes HOSTNAME, BANNER, PASSWORD (CONSOLE, TELNET and ENABLE),MANAGEMENT IPand DEFAULT GATEWAY.	03	L3,L4,L5
8	**Configuring and Verifying VLAN:**Establish a communication between the hosts by connecting the network Devices as given below, configure them and verify the same. Configuration includes Switch port configuration and encapsulation methods.	03	L3,L4,L5
9	**Configuring and Verifying IP Routing:**Establish a communication between the hosts by connecting the network Devices as given below,	03	L3,L4,L5

	configure them and verify the same. Configuration includes: 1. Static Routing 2. Dynamic Routing (RIP/OSPF/EIGRP)		
10	**Configuring DHCP Server on a Router:** Configure DHCP server on a router to assign IP address dynamically to the hosts and verify the same **a. For One Broadcast Domain** **b. For Many Broadcast Domain**	03	L3,L4,L5
11	**PART-C [Simulation Case-Study]** Dr. AIT is granted a block of addresses starting from **192.168.100.0/24**. The Dr. AIT College committee decided to distribute these blocks of addresses to **THREE** Departments with each department receiving just **FOUR** Addresses. **1. Design the sub blocks and give the slash notation to each sub block.**	03	L3,L4,L5
12	**2. Simulate the above case using Cisco-packet Tracer.** Note: while simulating Consider the following Constraints: a. Establish a communication within the Departments. b. Only HOD's of each Department can communicate (Single user from each Department) with each other.	03	L3,L4,L5
13	Create topology to demonstrate port security using any application layer protocol.	03	L3,L4,L5

	Programme Outcomes (POs)
1	After the successful completion of this course the student should be able to conduct an experiment to simulate various protocols of data link and network layer.
2	After the successful completion of this course the student should be able to demonstrate the data communication between two systems using the communication kit.
3	After the successful completion of this course the student should be able to write the programs to verify the detection and correction of error.
4	After the successful completion of this course the student should be able to verify the algorithm to find shortest path.

	Relationship to the Program Outcomes(POs)	
	Course Outcomes (COs)	**Program Outcomes (POs)**
	CO1	PO4,PO5,PO9
	CO2	PO4,PO5,PO9
	CO3	PO4,PO5,PO9
	CO4	PO4,PO5,PO9
	CO5	PO4,PO5,PO9