Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

(Applicable to 2021 batch)

Scheme of Teaching and Examination for I /II Semester B.E., (Common to all B.E. Programmes) Academic Year:2022-23

Physics Cycle : I/II Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hours/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BS	21MAT101	Calculus and Linear Algebra	Mathematics	3	2	0	0	5	3	50	50	100	4
		21MAT201	Advanced Calculus and Numerical methods											
2	BS	21PHT102/ 21PHT202	Engineering Physics	Physics	3	0	0	0	3	3	50	50	100	3
3	ES	21EET103/ 21EET203	Basic Electrical Engineering	Electrical	2	2	0	0	4	3	50	50	100	3
4	ES	21CVT104/ 21CVT204	Elements of Civil Engineering & Mechanics	Civil	3	0	0	0	3	3	50	50	100	3
5	ES	21MED105/ 21MED205	Computer aided Engineering Drawing	Mechanical	2	0	2	0	4	3	50	50	100	3
6	BS	21PHL106/ 21PHL206	Engineering Physics Lab	Physics	0	0	2	0	2	3	50	50	100	1
7	ES	21EEL107/ 21EEL207	Basic Electrical lab	Electrical	0	0	2	0	2	3	50	50	100	1
8	HS	21HST108	Communicative English	Humanities	1	0	1*	0	2	2	50	50	100	1
		21HST208	Professional writing skills in English											
9	AE	21HST109	Health and Wellness	Humanities	1	0	1*	0	2	2	50	50	100	1
		21CVT209	Rural Development	Civil										
10	MC	21HSN110	Career Development skill-I	Humanities	1	0	1*	0	2	--	50	-	PP/NP	0
		21HSN210	Career Development skill-II											
									Total	29		500	450	900	20

Note: BS: Basic Science Course, ES: Engineering Science Course, HS: Humanities & Social Science Course,
AE: Ability Enhancement Course, MC: Mandatory Course, * No practical evaluation,
L: Lecture, T:Titorial, P:Practical/drawing, S:Self study, CIE: Continuous Internal Evaluation, SEE: Semester End Examination

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

Scheme of Teaching and Examination for I /II Semester B.E., (Common to all B.E. Programmes) Academic Year:2022-23

Chemistry Cycle: I/II Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BS	21MAT101	Calculus and Linear Algebra	Mathematics	3	2	0	0	5	3	50	50	100	4
		21MAT201	Advanced Calculus and Numerical methods											
2	BS	21CHT102/ 21CHT202	Engineering Chemistry	Chemistry	3	0	0	0	3	3	50	50	100	3
3	ES	21CST103/ 21CST203	Problem solving through Programming	Computer Science	2	2	0	0	4	3	50	50	100	3
4	ES	21ECT104/ 21ECT204	Basic Electronics and Communication Engineering	Electronics	3	0	0	0	3	3	50	50	100	3
5	ES	21MET105/ 21MET205	Elements of Mechanical Engineering	Mechanical	2	2	0	0	4	3	50	50	100	3
6	BS	21CHL106/ 21CHL206	Engineering Chemistry Laboratory	Chemistry	0	0	2	0	2	3	50	50	100	1
7	ES	21CSL107/ 21CSL207	Computer Programming Laboratory	Computer Science	0	0	2	0	2	3	50	50	100	1
8	HS	21HST108	Communicative English	Humanities	1	0	1*	0	2	2	50	50	100	1
		21HST208	Professional writing skills in English											
9	AE	21CVT109	Rural Development	Civil	1	0	1*	0	2	2	50	50	100	1
		21HST209	Health and Wellness	Humanities										
10	MC	21HSN110	Career Development skill-I	Humanities	1	0	1*	0	2	----	50	--	PP/NP	0
		21HSN210	Career Development skill-II											
								Total	30		500	450	900	20

Note: BS: Basic Science Course, ES: Engineering Science Course, HS: Humanities & Social Science Course, AE: Ability Enhancement Course, MC: Mandatory Course, * No practical evaluation,
L: Lecture, T:Titorial, P:Practical/drawing, S:Self study, CIE: Continuous Internal Evaluation, SEE: Semester End Examination

Note –At the end of the second-semester summer internship shall be carried out – based on inter/intra institutional activities credited in the third semester. University /Institutions may swap few courses between a FIRST and SECOND semester to balance the workload teaching and laboratory schedule

Summer Internship - I: All the students admitted shall have to undergo a mandatory summer internship of 03 weeks during the vacation of II semesters. Summer Internship shall include Inter / Intra Institutional activities. Internship A University Viva-voce examination shall be conducted during III semesters and the prescribed credit shall be included in III semesters. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

III Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BSC	21MAT301	Transform Calculus, Fourier Series and Numerical Techniques	Mathematics	2	2	0	0		03	50	50	100	3
2	IPCC	21ECT302	Digital System Design Using Verilog	ECE	3	0	2			03	50	50	100	4
3	IPCC	21ECT303	Basic Signal Processing	ECE	3	0	2			03	50	50	100	4
4	PCC	21ECT304	Analog Electronic Circuits	ECE	3	0	0	1		03	50	50	100	3
5	PCC	21ECL305	Analog & Digital Electronics Lab	ECE	0	0	2			03	50	50	100	1
6	UHV	21HST306	Social Connect and Responsibility		0	0	1			01	50	50	100	1
7	HSSC	21HST307	Samskrutika Kannada		1	0	0			01	50	50	100	1
		21HST307	Balake Kannada											
		OR												
		21HST308	Constitution of India and Professional Ethics											
8	AEC	21ECT309X	Ability Enhancement Course - III							01	50	50	100	1
9	HSSC	21HSN310	Professional Skills		1	0	0	1		02	50	----	PP/NP	0
Total											400	400	800	18
10	Scheduled activities from III to VIII semesters	21HSHS803	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE)(Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester. The activities shall be carried out between III semester to VIII semester (for 5 semesters). SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE and Yoga activities.									
		21HSN803	Physical Education (PE) (Sport and activities)	PE										
		21HSN803	Yoga	Yoga										

Course Prescribed to Lateral Entry Diploma Holders Admitted to III Semester B.E. Program

11		**21MAN311**	**Additional Mathematics-I**	**Maths**	**1**	**0**	**0**	**1**		**02**	**50**	**----**	**PP/NP**	**0**

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course. **L** –Lecture, **T** – Tutorial, **P**- Practical/ Drawing, **S** – Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD** Teaching Department, **PSB:** Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and 21KBK37/47 **Balake Kannada** is for non-Kannada speaking, reading, and writing students

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

21INT49Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internship of 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) Placement Training: These courses are prescribed for I to IV semesters respectively to the students of BE programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case any student fails to register for the said course/fails to secure the minimum 40% of the prescribed CIE marks, he/she shall be deemed to have secured an **NP (not pass)** grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.			
Ability Enhancement Course – III			
21ECL3091	LD Lab using Pspice / MultiSIM	**21ECL3093**	LIC Lab using Pspice / MultiSIM
21ECL3092	AEC Lab using Pspice / MultiSIM	**21ECL3094**	LabVIEW Programming Basics

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B.E. Electronics & Communication Engineering

Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

IV Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	BSC	21MAT401	Maths for Communication Engineers	Mathematics						03	50	50	100	3
2	IPCC	21ECT402	Digital Signal Processing	ECE	3	0	2			03	50	50	100	4
3	IPCC	21ECT403	Circuit analysis and control systems	ECE	3	0	2			03	50	50	100	4
4	PCC	21ECT404	Communication Theory	ECE	3	0	0	1		03	50	50	100	3
5	PCC	21ECL405	Communication Laboratory I	ECE	0	0	2			03	50	50	100	1
6	AEC	21ECT406	Biology For Engineers		0	0	1			02	50	50	100	2
7	HSSC	21HST407	Samskrutika Kannada		1	0	0			01	50	50	100	1
		21HST407	Balake Kannada											
		OR												
		21HST408	Constitution of India and Professional Ethics											
8	AEC	21ECT409X	Ability Enhancement Course - IV							01	50	50	100	1
9	HSSC	21HSN410	Professional Skills	HSS	1	0	1	0		02	50	----	PP/NP	0
10	UHV	21HSN412	Universal Human Values	Any Department	1	0	0	1		01	50	50	100	1
11	INT	21ECI413	Inter/Intra Institutional Internship	Evaluation By the appropriate authorities	Completed during the intervening period ofII and III semesters by students admitted to first year of BE./B.Tech and during the intervening period of III and IV semesters by Lateral entry students admitted to III semester.					03	100		100	2
									Total		550	450	1000	22
Course Prescribed to Lateral Entry Diploma Holders Admitted to III Semester B.E. Program														
12		21MAN411	Additional Mathematics-II	Maths	1	0	0	1		02	50	----	PP/NP	0

Note: BSC: Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course. **L** –Lecture, **T** – Tutorial, **P**- Practical/ Drawing, **S** – Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD** Teaching Department, **PSB:** Paper Setting department

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Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

Internship of 04 weeks during the intervening period of IV and V semesters; 21INT68Innovation/ Entrepreneurship/ Societal based Internship.

(1) All the students shall have to undergo a mandatory internship of 04 weeks during the intervening period of IV and V semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the VI semester grade card.The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be considered under F (fail) grade and shall have to complete during subsequently after satisfying the internship requirements.

(2) Innovation/ Entrepreneurship Internship shall be carried out at industry, State and Central Government /Non-government organizations (NGOs), micro, small and medium enterprise (MSME), Innovation centres or Incubation centres. Innovation need not be a single major breakthrough; it can also be a series of small or incremental changes. Innovation of any kind can also happen outside of the business world. Entrepreneurship internships offers a chance to gain hands on experience in the world of entrepreneurship and helps to learn what it takes to run a

small entrepreneurial business by performing intern duties with an established company. This experience can then be applied to future business endeavours. Start-ups and small companies are a preferred place to learn the business tack ticks for future entrepreneurs as learning how a small business operates will serve the intern well when he/she manages his/her own company. Entrepreneurship acts as a catalyst to open the minds to creativity and innovation. Entrepreneurship internship can be from several sectors, including technology, small and medium-sized, and the service sector.

(3) Societal or social internship. Urbanization is increasing on a global scale; and yet, half the world's population still resides in rural areas and is devoid of many things that urban population enjoy. Rural internship is a work-based activity in which students will have a chance to solve/reduce the problems of the rural place for better living. As proposed under the AICTE rural internship programme, activities under Societal or social internship, particularly in rural areas, shall be considered for 40 points under AICTE activity point programme.

Ability Enhancement Course – IV			
21ECL4091	Embedded C Basics	**21ECL4093**	Octave / Scilab for signals
21ECL4092	C++ Basics	**21ECL4094**	DAQ using LabVIEW

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B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

V Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	PCC	21ECT501	Digital Communication	ECE	3	0	0			3	50	50	100	3
2	IPCC	21ECT502	Microprocessor & Microcontrollers	ECE	3	0	2		3	3	50	50	100	4
3	PCC	21ECT503	Computer Communication Networks	ECE	3	0	0		3	3	50	50	100	3
4	PCC	21ECT504	Microwave Theory & Antennas	ECE	3	0	0		3	3	50	50	100	3
5	PCC	21ECL505	Communication Lab II	ECE	0	0	2		3	3	50	50	100	1
6	AEC	21RMT506	Research Methodology & Intellectual Property Rights	Any Department	2	0	0		2	2	50	50	100	2
7	HSSC	21CVT507	Environmental Studies	Civil/Chemistry	1	0	0			1	50	50	100	1
8	AEC	21ECL508x	Ability Enhancement Course-V	ECE						1/2	50	50	100	1
9	HSSC	21HSN509	Aptitude and Verbal ability skills		1	0	1	0		2	50	--	PP/NP	0
										Total	450	400	800	18

Ability Enhancement Course – V

21ECL5081	Computer Communication Networks Lab	**21ECL5083**	Antenna Design & Testing
21ECL5082	Communication Simulink Toolbox	**21ECL5084**	Microwaves toolbox

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B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

VI Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	HSSC	21ECT601	Technological Innovation Management and Entrepreneurship								50	50	100	03
2	IPCC	21ECT602	Computer Organization & ARM Microcontrollers	ECE	2	2			4	3	50	50	100	04
3	PCC	21ECT603	VLSI Design & Testing	ECE	3				3	3	50	50	100	03
4	PEC	21ECT604X	Professional Elective -I	ECE	3				3	3	50	50	100	03
5	OEC	21ECT605X	OpenElective-I	ECE	3				3	3	50	50	100	03
6	PCC	21ECL606	VLSI Laboratory	ECE			2		2		50	50	100	01
7	MP	21ECM607	Mini Project	ECE			2		2		50	50	100	02
8	INT	21ECI608	Innovation/Entrepreneurship /Societal Internship								50	50	100	03
9	HSSC	21HSN609	Analytical & Reasoning skills	Placement Cells	2	0	0-		02	--	50	--	PP/NP	00
								Total			500	450	900	22

Research/Industrial Internship - At the End of the sixth / Seventh semester (in two cycles to accommodate all the students of the University) Research/Industrial Internship shall be carried out – Based on industrial/Govt./NGO/MSME/Rural Internship/Innovation/Entrepreneurship. All the students admitted shall have to undergo a mandatory internship of 24 weeks during the vacation of VI/VII semesters. A University Viva-Voce examination shall be conducted during VII/VIII semester and the prescribed credit shall be included in VII/VIII semester. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements. Research internship Students have to take up research internships at Centers of Excellence (CoE) / Study Centers established in the same institute and /or out of the institute at reputed research organizations / Institutes. A research internship is intended to give you the flavour of current research going on on a particular topic/s. The internships serve this purpose. They help students get familiarized with the field, the skill needed the effort amount and kind of effort required for carrying out research in that field.

Industry internships: This is an extended period of work experience undertaken by university/Institute students looking to supplement their degree with professional development. The students are allowed to prepare themselves for the workplace and develop practical skills as well as academic ones. It also helps them learn to overcome

unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with "unexpected contingencies" helps students recognize, appreciate, and adapt to organization realities by tempering knowledge with practical constraints.

Mini-project work: Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini-project can be assigned to an individual student or a group having not more than 4 students. (or Mini Project is a laboratory-oriented course which will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications) CIE procedure for
Mini-project: (i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide. The CIE marks awarded for the Mini-project work, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the college. The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates. SEE for Mini-project: (i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester-end examination (SEE) conducted at the department. (ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester-end examination (SEE) conducted separately at the departments to which the student/s belongs
Open Elective Courses: Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives). Selection of an open elective shall not be allowed if, • The candidate has studied the same course during the previous semesters of the program. • The syllabus content of open electives is similar to that of the Departmental core courses or professional electives. • A similar course, under any category, is prescribed in the higher semesters of the program. • Registration to electives shall be documented under the guidance of the Programme Coordinator/ Advisor/Mentor

Professional Elective Courses-I		**Open Elective Courses-I**	
Subject Code	**Title**	**Subject Code**	**Title**
21ECT6041	Artificial Neural Networks (L:T:P :: 2:2:0)	**21ECT6051**	Communication Engineering (L:T:P :: 3:0:0)
21ECT6042	Cryptography (L:T:P :: 2:2:0)	**21ECT6052**	Microcontrollers (L:T:P :: 3:0:0)
21ECT6043	Python Programming (L:T:P :: 2:0:2)	**21ECT6053**	Basic VLSI Design (L:T:P :: 3:0:0)
21ECT6044	Micro Electro Mechanical Systems (L:T:P :: 3:0:0)	**21ECT6054**	Electronic Circuits with Verilog (L:T:P :: 2:0:2)
		21ECT6055	Sensors & Actuators (L:T:P :: 3:0:0)

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B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

VII Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	PCC	21ECT701	Advanced VLSI	ECE	3	0	0		3	3	50	50	100	3
2	PCC	21ECT702	Optical & Wireless Communication	ECE	2	0	0		3	3	50	50	100	2
3	PEC	21ECT703X	Professional elective Course-II	ECE	3	0	0		3	3	50	50	100	3
4	PEC	21ECT704X	Professional elective Course-III	ECE	3	0	0		3	3	50	50	100	3
5	OEC	21ECT705X	Open elective Course-II		3	0	0		3	3	50		100	3
6	Project	21ECP706	Project work	ECE						3	100	50	200	10
Total											350	450	700	24

Professional Elective Courses-II		Professional Elective Courses-III		Open Elective Courses-II	
Subject Code	Title	Subject Code	Title	Subject Code	Title
21ECT7031	Operating System	21ECT7041	IOT & wireless sensor networks	21ECT7051	Optical & Satellite Communication
21ECT7032	Digital Image Processing	21ECT7042	Network Security	21ECT7052	ARM Embedded Systems
21ECT7033	DSP Algorithms & Architecture	21ECT7043	Fabrication technology	21ECT7053	Basic Digital Image Processing
21ECT7034	Power Electronics	21ECT7044	Machine Learning with Python	21ECT7054	Cryptography
21ECT7035	Operational Research	21ECT7045	Multimedia Communication	21ECT7055	E-waste Management

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

VIII Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week				Examination				Credits
					L	T	P	S	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	Seminar	21ECS801	Technical Seminar		One contact hour /week for interaction between the faculty and students				--	100	---	100	01
2	Research Internship/ Industry Internship	21ECI802	Research/Industry Internship*		Two contact hours /week for interaction between the faculty and students.				3 (Batch wise)	100	100	200	15
3	NCMC	21EC803	National Service Scheme (NSS)	NSS	Completed during the intervening period of III semester to VIII semester.				--	50	50	100	--
		21EC803	Physical Education (PE) (Sports & Athletics)	PE									
		21EC803	Yoga	Yoga									
									Total	250	150	400	16

Note: (1) University /Institutions may swap 7th and 8th Semester Course work to accommodate industry/research internship at the end of sixth semester /at the end of seventh semester to balance the workload. (2) Credits earned for the course prescribed will be accounted in 8th semester

Dr Ambedkar Institute of Technology, Bengaluru-56
Department of Electronics and Communication Engineering
Scheme and Syllabus - CBCS – 2021 -2022

Course Title	**BASIC ELECTRONICS AND COMMUNICATION ENGINEERING**						
Course Code	**21ECT104/204**						
Category	Engineering Science Course (ES)						
Scheme and Credits	No. of Hours/Week					Total teaching hours	Credits
	L	T	P	SS	Total		
	02	02	00	00	03	52	03
CIE Marks: 50	**SEE Marks: 50**		**Total Max. marks=100**		**Duration of SEE: 03 Hours**		

COURSE OBJECTIVES:

1. Preparation: To prepare students with fundamental knowledge/ overview in the field of Electronics and Communication Engineering.
2. Core Competence: To equip students with a basic foundation in electronic engineering fundamentals required for comprehending the operation and application of electronic circuits, logic design, embedded systems and communication systems.
3. Professionalism & Learning Environment: To inculcate in first year engineering students an ethical and a professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context and life- long learning needed for a successful professional career.

UNIT I **11 hours**

Electronic Circuits: Rectifiers, Reservoir and smoothing circuits, Full-wave rectifiers, Bi-phase rectifier circuits, Bridge rectifier circuits, Voltage regulators, Output resistance and voltage regulation, Voltage multipliers, Power Supplies–Block diagram, (No Derivations, Numericals on Rectifiers included).

Amplifiers: Types of amplifiers, Class of operation, Input and output resistance, Frequency response, Bandwidth, Phase shift, Negative feedback.

Operational amplifiers: Operational amplifier parameters, Operational amplifier characteristics, Operational amplifier configurations, Operational amplifier circuits, Multi-stage amplifiers.

Oscillators: Positive feedback, Conditions for oscillation, Ladder network oscillator, Wein bridge oscillator. (No Derivations, Numericals on Op-amp included). **Text 1**

Self-study component: BJT types, comparison of BJT, FET & FinFET.

UNIT II **11 hours**

Logic Circuits: Boolean Algebra, Logic gates, Realization of Boolean Expressions using basic gates and their truth table.

Half Adder and Full Adder, Multiplexer and decoder. Shift registers and its types – operation and truth table, Counters and asynchronous counters. Bistables, R-S Bistables, D-type Bistables, J-K Bistables. **Text 4**

Data representation, Data types, Data storage, A microcontroller system.

Sensors and Interfacing: Instrumentation and control systems, Transducers, Sensors. **Text 1**

Actuators, LED, 7-Segment LED Display, Optocoupler, Stepper Motor, Relay, Piezo Buzzer, Push Button Switch, Keyboard. **Text 2**

Self-study component: Actuator types, LCD, Touch screen displays

UNIT III **10 hours**

Embedded Systems: Definition, Embedded systems vs general computing systems, Classification of Embedded Systems, Major application areas of Embedded Systems, Elements of an Embedded System, Core of the Embedded System, Microprocessor vs Microcontroller, RISC vs CISC, Harvard vs Von-Neumann, Big- Endian vs Little-Endian, Memory, Program storage memory (ROM), RAM, Embedded firmware, other system components. **Text 2**

Communication Interface: UART, Parallel Interface, USB, Bluetooth, Wi-Fi, GPRS. **Text 2**

Self-study component: Block diagrams of the architectures of RISC, CISC, Harvard and Von-Neumann.

UNIT IV **10 hours**

Analog and Digital Communication: Modern communication system scheme, Information source and input transducer, Transmitter, Channel – Hardware and Software, Noise, Receiver, Multiplexing, Types of communication systems. **Text 3**

Types of modulation (only concepts) – AM, FM, Phase Modulation, Pulse Modulation, PAM, PWM, PPM, PCM. Concept of Radio wave propagation. Concepts of Sampling theorem, Nyquist rate, Digital Modulation Schemes– ASK, FSK, PSK

Self-study component: Evolution of Wireless Network Communication Technologies (1G, 2G, 3G and4G, 5G).

UNIT V **10 hours**

Data Transmission: Asynchronous Transmission, Synchronous Communication, Data Compression, Encryption.

Radio Waves, Antennas, Satellite Communication, Microwave Communication, Optical Fiber Communication (OFC): Block diagram of OFC, Advantages of OFC, Applications of OFC. **Text 4**

Cellular Wireless Networks - Introduction, cellular telephone system, cellular concept and frequency reuse. **Text 3**

Self-study component: **Co-ordination number, Atomic packing factor (APF) for simple cubic, body centered and face centered cubic structure. Applications of nanomaterials: Medical and Electronics.**

TEACHING LEARNING PROCESS: Chalk and Talk, power point presentation, animations, videos

COURSE OUTCOMES: On completion of the course, student should be able to:

CO1: Describe the concepts of electronic circuits encompassing power supplies, amplifiers and oscillators.

CO2: Explain the concepts of digital logic circuits, sensors, actuators and I/O subsystems.

CO3: Discuss the characteristics of embedded systems and types of communication interface.

CO4: Describe the fundamental concepts of analog communication, digital communication and radio wave propagation.

CO5: discuss the techniques of data transmission, different modes of communication, wired and wireless communication systems.

TEXT BOOKS

1. Mike Tooley, 'Electronic Circuits, Fundamentals & Applications', 4thEdition, Elsevier, 2015. DOI https://doi.org/10.4324/9781315737980. eBook ISBN9781315737980
2. K V Shibu, 'Introduction to Embedded Systems', 2nd Edition, McGraw Hill Education (India),Private Limited, 2016.
3. S L Kakani and Priyanka Punglia, 'Communication Systems', New Age International Publisher, 2017. https://elib4u.ipublishcentral.com/pdfreader/communication-systems
4. D P Kothari, I J Nagrath, 'Basic Electronics', 2nd edition, McGraw Hill Education (India), PrivateLimited, 2018.

REFERENCE BOOK

1. Mitchel E. Schultz, 'Grob's Basic Electronics', 11th Edition, McGraw-Hill, 2011.

ONLINE RESOURCES

1. https://onlinecourses.nptel.ac.in/noc21_ee55/preview

MODERN TOOLS:

1. PSPICE

MAPPING of COs with POs

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1		1			2	1	1		3
CO2	3	2	1					2	1	1		3
CO3	3							2	1	1		3
CO4	3							2	1	1		3
CO5	3							2	1	1		3
Strength of correlation: Low-1, Medium- 2, High-3												

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

B.E: Electronics & Communication Engineering

NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2022 – 23)

SEMESTER - III

TRANSFORM CALCULUS, FOURIER SERIES AND NUMERICAL TECHNIQUES			
Course Code	**21MAT301**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course objectives: The goal of the course Transform Calculus, Fourier series and Numerical techniques 21MAT 31 is

- To have an insight into solving ordinary differential equations by using Laplace transform techniques
- Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis.
- To enable the students to study Fourier Transforms and concepts of infinite Fourier Sine and Cosine transforms and to learn the method of solving difference equations by the z-transform method.
- To develop proficiency in solving ordinary and partial differential equations arising in engineering applications, using numerical methods

Teaching-Learning Process (General Instructions):

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied mathematical skills.
2. State the need for Mathematics with Engineering Studies and Provide real-life examples.
3. Support and guide the students for self–study.
4. You will also be responsible for assigning homework, gradingassignments and quizzes, and documenting students' progress.
5. Encourage the students for group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision of topics (post-lectureactivity).
   - As additional examples (post-lectureactivity).
   - As an additional material of challenging topics (pre-and post-lecture activity).
   - As a model solution for some exercises (post-lecture activity).

Module-1: Laplace Transform

Definition and Laplace transforms of elementary functions (statements only). Problems on Laplace's Transform of $e^{at}f(t)$, $t^n f(t)$, $\frac{f(t)}{t}$. Laplace transforms of Periodic functions (statement only) and unit-step function – problems.

Inverse Laplace transforms definition and problems, Convolution theorem to find the inverse Laplace transforms (without Proof) problems. Laplace transforms of derivatives, solution of differential equations. **(8 Hours)**

Self-study: Solution of simultaneous first-order differential equations.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation **(RBT Levels: L1, L2 and L3)**

Module-2: Fourier Series

Introduction to infinite series, convergence and divergence. Periodic functions, Dirichlet's condition. Fourier series of periodic functions with period 2π and arbitrary period. Half range Fourier series. Practical harmonic analysis.

Self-study: Convergence of series by D'Alembert's Ratio test and, Cauchy's root test.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation **(RBT Levels: L1, L2 and L3)**

Module-3: Infinite Fourier Transforms and Z-Transforms

Infinite Fourier transforms definition, Fourier sine and cosine transforms. Inverse Fourier transforms, Inverse Fourier cosine and sine transforms. Problems.

Difference equations, z-transform-definition, Standard z-transforms, Damping and shifting rules, Problems. Inverse z-transform and applications to solve difference equations.

Self Study: Initial value and final value theorems, problems.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation **(RBT Levels: L1, L2 and L3)**

Module-4: Numerical Solution of Partial Differential Equations

Classifications of second-order partial differential equations, finite difference approximations to derivatives, Solution of Laplace's equation using standard five-point formula. Solution of heat equation by Schmidt explicit formula and Crank- Nicholson method, Solution of the Wave equation. Problems.

Self Study: Solution of Poisson equations using standard five-point formula.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation **(RBT Levels: L1, L2 and L3)**

Module-5: Numerical Solution of Second-Order ODEs and Calculus of Variations

Second-order differential equations - Runge-Kutta method and Milne's predictor and corrector method. (No derivations of formulae).

Calculus of Variations: Functionals, Euler's equation, Problems on extremals of functional. Geodesics on a plane, Variational problems.

Self Study: Hanging chain problem.**(RBT Levels: L1, L2 and L3)**

Course outcomes: After successfully completing the course, the students will be able :

1. To solve ordinary differential equations using Laplace transform.
2. Demonstrate the Fourier series to study the behaviour of periodic functions and their applications in system communications, digital signal processing and field theory.
3. To use Fourier transforms to analyze problems involving continuous-time signals and to apply Z-Transform techniques to solve difference equations
4. To solve mathematical models represented by initial or boundary value problems involving partial differential equations

Determine the extremals of functionals using calculus of variations and solve problems arising in dynamics of rigid bodies and vibrational analysis.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures notless than 35% (18 Marks out of 50)in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together **Continuous Internal Evaluation:**

Three Unit Tests each of **20 Marks**

(duration 01 hour)First test at the end of

5th week of the semester
Second test at the end of the 10th
week of the semesterThird test at the
end of the 15th week of the semester
Two assignments each of **10 Marks**
First assignment at the end of 4th week of
the semester Second assignment at the end
of 9th week of the semester
Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks**
(**duration 01 hours**)
At the end of the 13th week of the semester
The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be
scaled down to 50 marks
(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).
CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:
Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**
The question paper will have ten questions. Each question is set for 20 marks.
There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub- questions), **should have a mix of topics** under that module.
The students have to answer 5 full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books:

1. **B. S. Grewal**: "Higher Engineering Mathematics", Khanna publishers, 44th Ed.2018
2. **E. Kreyszig**:"Advanced Engineering Mathematics", John Wiley & Sons, 10th Ed. (Reprint), 2016.

Reference Books

1. **V. Ramana:** "Higher Engineering Mathematics" McGraw-Hill Education, 11th Ed.
2. **Srimanta Pal & Subodh C. Bhunia:** "Engineering Mathematics" Oxford University Press, 3rd Reprint,2016.
3. **N.P Bali and Manish Goyal**: "A textbook of Engineering Mathematics" Laxmi Publications, Latestedition.
4. **C. Ray Wylie, Louis C. Barrett:** "Advanced Engineering Mathematics" McGraw – Hill BookCo.Newyork, Latest ed.
5. **Gupta C.B, Sing S.R and Mukesh Kumar:** "Engineering Mathematic for Semester I and II", Mc- GrawHill Education(India) Pvt. Ltd 2015.
6. **H.K.Dass and Er. Rajnish Verma:** "Higher Engineering Mathematics" S.Chand Publication (2014).
7. **James Stewart: "**Calculus" Cengage publications, 7th edition, 4th Reprint 2019.

Web links and Video Lectures (e-Resources):

- http://.ac.in/courses.php?disciplineID=111
- http://www.class-central.com/subject/math(MOOCs)
- http://academicearth.org/
- http://www.bookstreet.in.

- VTU e-Shikshana Program
- VTU EDUSAT Program

Activity-Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes
- Assignments
- Seminars

Sub Title: Digital System Design Using Verilog		
Sub Code:21ECT302	**No. of Credits:4=3:0:2:0 (L: T: P: S)**	**No. of lecture hours/week: 4**
Exam Duration:3 hrs	**CIE +Assignment + Group Activity + SEE =45 + 5 + 5+50 =100**	**Total No. of Contact Hours :52**

Course objectives: This course will enable students to:

1. To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
2. To impart the concepts of designing and analyzing combinational logic circuits.
3. To impart design methods and analysis of sequential logic circuits.
4. To impart the concepts of Verilog HDL-data flow and behavioral models for thedesign of digital systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.

Give Programming Assignments.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Principles of Combinational Logic**: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps- up to 4 variables, Quine-McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms. (Section 3.1 to 3.5 of Text 1).	08	L1, L2, L3
2	**Logic Design with MSI Components and Programmable Logic Devices**: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section 5.1 to 5.7 of Text 2)	08	L1, L2, L3

3	**Flip-Flops and its Applications**: The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, JK, D and SRflip-flops. (Section 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text 2)	08	L1, L2, L3
4	**Introduction to Verilog**: Typical Design Flow, Data types, Modules, Ports. **Verilog Data flow description:** Continuous assignments, Delays, Expressions, Operators, and operands, operator types, Examples (Section1.3, 3.2, 6.1 to 6.5 of Text 3)	08	L1, L2, L3
5	**Verilog Behavioral description:** Procedural Assignments, Conditional statements, Multiway branching, Loops, Examples. (Section 7.2, 7.4, 7.5, 7.6 and 7.9 of Text 3) **Verilog Structural description**: Gate types, Examples. (Section 5,1 of Text 3)	08	L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Using suitable simulation software, demonstrate the operation of the following circuits:

Sl.No	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program.
2	To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description: 8:1 mux, 8:3 encoder, Priority encoder
6	To realize using Verilog Behavioral description: 1:8 Demux, 3:8 decoder, 2-bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a) JK type b) SR type c) T type and d) D type
8	To realize Counters - up/down (BCD and binary) using Verilog Behavioral description.

Demonstration Experiments (For CIE only – not to be included for SEE)

Use FPGA/CPLD kits for downloading Verilog codes and check the output for interfacing experiments.

9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface a Relay or ADC to the FPGA/CPLD and demonstrate its working.
11	Verilog programs to interface DAC to the FPGA/CPLD for Waveform generation.
12	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From unit 1 and 2, Assignment2 from units 3,4 and 5
3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 1 - Digital teaching and learning

Course Outcomes

CO1 Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.

CO2 Analyze and design for combinational logic circuits.

CO3 Analyze the concepts of Flip Flops (SR, D, T and JK) and to design the synchronous sequential circuits using Flip Flops.

CO4 Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

CO5

COs	**Mapping with POs**
CO1	PO1, PO2, PO3, PO4
CO2	PO1, PO2, PO3, PO4,
CO3	PO2, PO3, PO4, PO5, PO12
CO4	PO2, PO3, PO4, PO5, PO12
CO5	

Text Book:

1. **Digital Logic Applications and Design** by John M Yarbrough, Thomson Learning, 2001.
2. **Digital Principles and Design by Donald D Givone**, McGraw Hill, 2002.
3. **Verilog HDL – A guide to Digital Design and Synthesis** by Samir Palnitkar**,** Pearson, 2003

Reference Books:

1. **Fundamentals of logic design**, by Charles H Roth Jr., Cengage Learning
2. **Logic Design,** by Sudhakar Samuel, Pearson/ Sanguine, 2007
3. **Fundamentals of HDL,** by Cyril P R, Pearson/Sanguine 2010

MOOCS:

1. Electronic Design Automation http://nptel.ac.in/courses/106105083/
2. Digital system design with PLDs and FPGA shttp://nptel.ac.in/courses/117108040/ Fundamentals of HDL

Sub Title: Basic Signal Processing		
Sub Code: 21ECT303	**No. of Credits:4=3: 0: 2 (L-T-P)**	**No. of lecture hours/week: 04**
Exam Duration:3 Hours	**CIE +Group Activity + Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Understanding the fundamental knowledge/ overview in the field of Signal Processing.
2. Familiarizing the concepts of vector spaces and orthogonality with a qualitative insight into applications in communications.
3. Understanding the mathematical description of discrete time signals and systems, and analyzing the signals in time domain using convolution sum,
4. To understand classifying signals into different categories based on their properties, and analyzing Linear Time Invariant (LTI) systems in time and transform domains.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Vector Spaces:** Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis and dimension, Dimensions of the four subspaces, Rank-Nullity Theorem, Linear Transformations Orthogonality: Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram-Schmidt Orthogonalization procedure **(Refer Chapters 2 and 3 of Text 1)**	08	L1, L2, L3.
2	**Eigen values and Eigen vectors:** Review of Eigen values and Diagonalization of a Matrix, Special Matrices (Positive Definite Symmetric) and their properties, Singular Value Decomposition. **(Refer Chapter 5, Text 1)**	06	L1, L2,L3
3	**Introduction and Classification of signals:** Definition of signal and systems with examples, Elementary signals/Functions: Exponential, sinusoidal, step, impulse and ramp functions Basic Operations on signals: Amplitude scaling, addition, multiplication, time scaling, time shift and time reversal. Expression of triangular, rectangular and other waveforms in terms of elementary signals System Classification and properties: Linear-nonlinear, Time variant -invariant, causal-noncausal, static-dynamic, stable-unstable, invertible. **(Refer Chapters 1 of Text 2) [Only for Discrete Signals & Systems]**	08	L1,L2,L3
4	**Time domain representation of LTI System**: Impulse response, convolution sum. Computation of convolution sum using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular. LTI system Properties in terms of impulse response: System interconnection, Memory less, Causal, Stable, Invertible and Deconvolution and step response **(Refer Chapters 2 of Text 2) [Only for Discrete Signals & Systems]**	09	L1,L2,L3
5	**The Z-Transforms**: Z transform, properties of the region of convergence, properties of the Z-transform, Inverse Z-transform by partial fraction, Causality and stability, Transform analysis of LTI systems. **(Refer Chapters 2 of Text 7)**	08	L1,L2,L3

PRACTICAL COMPONENT OF IPCC	
1	Program to create and modify a vector (array). b. Program to create and modify a matrix.
2	Programs on basic operations on matrix.
3	Program to solve system of linear equations.
4	Program for Gram-Schmidt orthogonalization.
5	Program to find Eigen value and Eigen vector.
6	Program to find Singular value decomposition.
7	Program to generate discrete waveforms.
8	Program to perform basic operation on signals
9	Program to perform convolution of two given sequences.
10	a. Program to perform verification of commutative property of convolution. b. Program to perform verification of distributive property of convolution. c. Program to perform verification of associative property of convolution.
11	Program to compute step response from the given impulse response.
12	Programs to find Z-transform and inverse Z-transform of a sequence.

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3. The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component

Course Outcomes: After the completion of the Course the student can:

CO1. Understand the basics of Linear Algebra
CO2. Analyze different types of signals and systems
CO3. Analyze the properties of discrete time signals & systems
CO4. Analyze discrete time signals & systems using Z transform
CO5.

Cos	Mapping with POs	Mapping with PSOs
CO1	PO1,PO2,PO3, PO4,PO5	PSO1,PSO2,PS03
CO2	PO1,PO2,PO3, PO4,PO5	PSO1,PSO2,PS03
CO3	PO1,PO2,PO3, PO4,PO5	PSO1,PSO2, PS03
CO4	PO1,PO2,PO3, PO4,PO5	PSO1,PSO2, PS03
CO5	PO1,PO2,PO3,PO4,PO5	PSO1,PSO2, PS03

Text Book:	
1.	Gilbert Strang, **"Linear Algebra and its Applications"**, Cengage Learning, 4th Edition, 2006, ISBN 97809802327
2.	Simon Haykin and Barry Van Veen, **"Signals and Systems"**, 2nd Edition, 2008, Wiley India. ISBN9971-51- 239-4.
Reference Books:	
1.	Michael Roberts, **"Fundamentals of Signals & Systems"**,2nd edition, Tata McGraw-Hill, 2010, ISBN978-0- 07-070221-9.
2.	Alan V Oppenheim, Alan S WiIIsky and S Hamid Nawab, **"Signals and Systems"** Pearson Education Asia / PHI, 2"" edition, 1997. Indian Reprint 2002.
3.	H P Hsu, R Ranjan, **"Signals and Systems",** Schaum's outlines, TMH, 2006.
4.	B P Lathi, "**Linear Systems and Signals**", Oxford University Press, 2005.
5.	S UdayaKumar, "**Signals and Systems**", 7th Edition Pristine Publishing House.
6.	Ganesh Rao and Satish Tunga, "**Signals and Systems**", Pearson/Sanguine.

Web Links:	
1.	Video lectures on Signals and Systems by Alan V Oppenheim Lecture 1, Introduction | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube Lecture Lecture 2, Signals and Systems: Part 1 | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube
2.	NPTEL video lectures signals and system: https://www.youtube.com/watch?v=7Z3LE5uM-6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ_9kfoqZyx
3.	Video lectures on Linear Algebra by Gilbert Strang https://www.youtube.com/watch?v=ZK3O402wf1c&list=PL49CF3715CB9EF31D&index=1

Sub Title: Analog Electronic Circuits		
Sub Code: 21ECT304	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 03**
Exam Duration: 3 Hours	**CIE +Group Activity + Assignment +SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives: This course will enable students to

1. Explain various BJT parameters, connections and configurations**.**
2. Design and demonstrate the diode circuits and transistor amplifiers.
3. Explain various types of FET biasing and demonstrate the use of FET amplifiers.
4. Analyze Power amplifier circuits in different modes of operation.
5. Construct Feedback and Oscillator circuits using FET.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor. Small signal operation and Models: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model, The T model. MOSFETs: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor. Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model. [Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.7), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.7)]	08	L1, L2, L3.
2	MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, Source follower. MOSFET internal capacitances and High frequency model: The gate capacitive effect, Junction capacitances, High frequency model. Frequency response of the CS amplifier: The three frequency bands, high frequency response, Low frequency response. Oscillators: FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) [Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]	08	L1, L2,L3

3	Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). Output Stages and Power Amplifiers: Introduction, Classification of output stages, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. [Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]	08	L1,L2,L3
4	Op-Amp Circuits: Op-amp DC and AC Amplifiers, DAC - Weighted resistor and R-2R ladder, ADC- Successive approximation type, Small Signal half wave rectifier, Absolute value output circuit, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. 555 Timer and its applications: Monostable and Astable Multivibrators. [Text 2: 6.2, 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2,8.13 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3,9.4.3(a)]	08	L1,L2,L3,L4
5	Overview of Power Electronic Systems: Power Electronic Systems, Power Electronic Converters and Applications. Thyristors: Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-off Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A without design consideration. Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit. [Text 3: 1.3, 1.5,1.6, 2.2, 2.3, 2.4,2.6, 2.7,2.9, 2.10, 3.2, 3.5.1, 3.5.2, 3.6.1, 3.6.3,3.6.4]	07	L1,L2,L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3. Unit 1- Digital Teaching and Learning

Course Outcomes: After the completion of the Course the student can:

CO1.Understand the characteristics of BJTs and FETs for switching and amplifier circuits.

CO2. Design and analyze FET amplifiers and oscillators with different circuit configurations and biasing conditions.

CO3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators.

CO4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.

Cos	Mapping with POs	Mapping with PSOs
CO1	PO1 PO2 PO3 PO5	PSO1 PSO2
CO2	PO1 PO2 PO3	PSO1 PSO2
CO3	PO1 PO2 PO3	PSO1 PSO2
CO4	PO1 PO2 PO3	PSO1 PSO2
CO5	PO1 PO2 PO3	PSO1 PSO2

Text Book:	
1.	1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6th Edition, Oxford,2015. ISBN:978-0-19-808913-1
2.	2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education,2018. ISBN: 978-93-325-4991-3
3.	3. Electronic Principles, Albert Malvino, David J Bates, 7th Edition, McGraw Hill Education (India)Private Limited, 2017, ISBN:978-0-07-063424-4

Web Links:	
1.	www.nptel.in
2.	. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C.Halkias, McGraw-Hill, 2015.
3.	Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

Analog and Digital Electronics Lab			
Course Code	**21ECL305**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Study the static characteristics of SCR and test the RC triggering circuit.
- Design and test the combinational and sequential logic circuits for their functionalities.
- Use the suitable ICs based on the specifications and functions.

Sl.No.	Experiments
1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator and iii) RC Phase shift oscillator
3	Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator
4	Obtain the static characteristics of SCR and test SCR Controlled HWR and FWR using RC triggering circuit.
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor & Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.
8	Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192

9	Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod-16
10	Pseudorandom sequence generator using IC7495
11	Test the precision rectifiers using opamp: i) Half wave rectifier ii) Full wave rectifier
12	Design and test Monostable and Astable Multivibrator using 555 Timer

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Design and analyze the BJT/FET amplifier and oscillator circuits.
2. Design and test Opamp circuits to realize the mathematical computations, DAC and precision rectifiers.
3. Design and test the combinational logic circuits for the given specifications.
4. Test the sequential logic circuits for the given functionality.
5. Demonstrate the basic electronic circuit experiments using SCR and 555 timer.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Fundamentals of Electronic Devices and Circuits Lab Manual, David A Bell, 5th Edition, 2009, Oxford University Press.
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition.

III Semester –Ability Enhancement courses

LD (Logic Design) Lab using Pspice / MultiSIM			
Course Code	**21ECT3081**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

- Impart the concepts of De Morgan's Theorem, SOP, POS forms.
- Impart the concepts of designing and analyzing combinational logic circuits.
- Impart the concepts of analysis of sequential logic circuits.
- Analyze and design any given synchronous sequential circuits.

Sl.No	Experiments
1	Implementation of De Morgan's theorem and SOP/POS expressions using Pspice/Multisim.
2	Implementation of Half Adder, Full Adder, Half Subtractor and Full Subtractor using Pspice/ Multisim.
3	Design and implementation of 4-bit Parallel Adder/ Subtractor using IC 7483 and BCD to Excess-3 code conversion and vice-versa using Pspice/Multisim.
4	Design and implement of IC 7485 5-bit magnitude comparator using Pspice/Multisim.
5	To Realize Adder & Subtractor using IC 74153 (4:1 MUX) and 4-variable function using IC74151 (8:1MUX) using Pspice/Multisim.
6	To realize Adder and Subtractor using IC 74139/ 74155N (Demux/Decoder) and Binary to Gray code conversion & vice versa using 74139/ 74155N using Pspice/Multisim.
7	SR, Master-Slave JK, D & T flip-flops using NAND Gates using Pspice/Multisim.
8	Design and realize the Synchronous counters (up/down decade/binary) using Pspice/Multisim.
9	Realize the shift registers and their modes (SISO, PISO, PIPO, SIPO) using 7474/7495 using Pspice/Multisim.
10	Design Pseudo Random Sequence generator using 7495 using Pspice/Multisim.
11	Design Serial Adder with Accumulator and simulate using Pspice/Multisim.
12	Design using Pspice/Multisim Mod-N Counters.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Demonstrate the truth table of various expressions and combinational circuits using logic gates.
2. Design various combinational circuits such as adders, subtractors, comparators, multiplexers and code converters.
3. Construct flips-flops, counters and shift registers.
4. Design and implement synchronous counters.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student

shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

- Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001
- Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.

AEC (Analog Electronic Circuits) Lab			
Course Code	**21ECT3082**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	2

Course objectives:

- To provide practical exposure to the students on designing, setting up, executing and debugging various electronic circuits using simulation software.
- To give the knowledge and practical exposure on simple applications of analog electronic circuits.

Sl.No	Experiments using Pspice/MultiSIM software
1	Experiments to realize diode clipping (single, double ended) circuits.
2	Experiments to realize diode clamping (positive, negative) circuits.
3	Experiments to realize Full wave rectifier without filter (and set-up to measure the ripple factor, Vp-p, Vrms, etc.).
4	Design and conduct an experiment on Series Voltage Regulator using Zener diode to determine line/load regulation characteristics.
5	Realize BJT Darlington Emitter follower without bootstrapping and determine the gain, input and output impedances (other configurations of emitter follower can also be considered).
6	Set-up and study the working of complementary symmetry class B push pull power amplifier (other power amplifiers can also be suitably considered) and calculate the efficiency.
7	Design and set-up the oscillator circuits (Hartley, Colpitts, etc. using BJT/FET) and determine the frequency of oscillation.
8	Design and set-up the crystal oscillator and determine the frequency of oscillation.
9	Experiment to realize Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.
10	Experiments to realize Transfer and drain characteristics of a MOSFET.
11	Experiments to realize UJT triggering circuit for Controlled Full wave Rectifier.
12	Design and simulation of Regulated power supply.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Understand the circuit schematic and its working.
2. Study the characteristics of different electronic devices.
3. Design and test simple electronic circuits as per the specifications using discrete electronic components.
4. Compute the parameters from the characteristics of active devices.
5. Familiarize with EDA software which can be used for electronic circuit simulation.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book.

Suggested Learning Resources:

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.
2. Muhammed H Rashid, "Introduction to PSpice using OrCAD for circuits and electronics", 3rd Edition, Prentice Hall, 2003.

III Semester

<table>
<tr><th colspan="4">LIC (Linear Integrated Circuits) Lab using Pspice / MultiSIM</th></tr>
<tr><td colspan="2">Course Code</td><td>21ECT3083</td><td>CIE Marks</td><td>50</td></tr>
<tr><td colspan="2">Teaching Hours/Week (L:T:P: S)</td><td>0:0:2:0</td><td>SEE Marks</td><td>50</td></tr>
<tr><td colspan="2">Credits</td><td>1</td><td>Exam Hours</td><td>100</td></tr>
<tr><td colspan="4">Course objectives:
To apply operational amplifiers in linear and nonlinear applications.
To acquire the basic knowledge of special function ICs.
To use Multisim/Pspice software for circuit design and simulation</td></tr>
<tr><td>Sl.No</td><td colspan="3">Experiments using Pspice / MultiSIM
Every experiment has to be designed, circuit to be drawn / constructed and executed in the specified software. Results are also to be noted and inferred.</td></tr>
<tr><td></td><td colspan="3">Note: Standard design procedure to be adopted.</td></tr>
<tr><td>1</td><td colspan="3">To realize using op-amp an Inverting Amplifier and Non-Inverting Amplifier</td></tr>
<tr><td>2</td><td colspan="3">To realize using op-amps i) Summing Amplifier ii)Difference amplifier</td></tr>
<tr><td>3</td><td colspan="3">To realize using op-amps an Instrumentation Amplifier</td></tr>
<tr><td>4</td><td colspan="3">To realize using op-amps i) Differentiator ii)Integrator</td></tr>
<tr><td>5</td><td colspan="3">To realize using op-amps a Full wave Precision Rectifier</td></tr>
<tr><td>6</td><td colspan="3">To realize using op-amps
Inverting and Non-Inverting Zero Crossing Detectors
Positive and Negative Voltage level detectors</td></tr>
<tr><td>7</td><td colspan="3">To realize using op-amp an Inverting Schmitt Trigger</td></tr>
<tr><td>8</td><td colspan="3">To realize using op-amp an Astable Multivibrator</td></tr>
<tr><td>9</td><td colspan="3">To design and implement using op-amps
Butterworth I & II order Low Pass Filter
Butterworth I & II order High Pass Filter</td></tr>
<tr><td>10</td><td colspan="3">To design and implement using op-amp a RC Phase Shift Oscillator</td></tr>
<tr><td>11</td><td colspan="3">To design and implement Mono-stable Multivibrator using 555 timer</td></tr>
<tr><td>12</td><td colspan="3">To design and implement 4 - bit R-2R Digital to Analog Converter</td></tr>
<tr><td colspan="4">Course outcomes (Course Skill Set):
After studying this course, students will be able to;
Sketch/draw circuit schematics, construct circuits, analyze and troubleshoot circuits containing op-amps, resistors, diodes, capacitors and independent sources.
Relate to the manufacturer's data sheets of IC 555 timer and IC μa741 op-amp.
Realize and verify the operation of analog integrated circuits like Amplifiers, Precision Rectifiers, Comparators and Waveform generators.
Design and implement analog integrated circuits like Oscillators, Active filters, Timer circuits, Data converters and compare the experimental results with theoretical values.</td></tr>
</table>

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018.

III Semester

LabVIEW Programming Basics			
Course Code	**21ECT3084**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

- Aware of various front panel controls and indicators.
- Connect and manipulate nodes and wires in the block diagram.
- Locate various toolbars and pull-down menus for the purpose of implementing specific functions.
- Locate and utilize the context help window.
- Familiar with LabVIEW and different applications using it.
- Run a Virtual Instrument (VI).

Sl.No	**VI Programs (using LabVIEW software) to realize the following:**
1	Basic arithmetic operations: addition, subtraction, multiplication and division
2	Boolean operations: AND, OR, XOR, NOT and NAND
3	Sum of 'n' numbers using 'for' loop
4	Factorial of a given number using 'for' loop
5	Determine square of a given number
6	Factorial of a given number using 'while 'loop
7	Sorting even numbers using 'while' loop in an array
8	Finding the array maximum and array minimum
	Demonstration Experiments (For CIE)
9	Build a Virtual Instrument that simulates a heating and cooling system. The system must be able to be controlled manually or automatically.
10	Build a Virtual Instrument that simulates a Basic Calculator (using formula node).
11	Build a Virtual Instrument that simulates a Water Level Detector.
12	Demonstrate how to create a basic VI which calculates the area and perimeter of a circle.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Use Lab VIEW to create data acquisition, analysis and display operations
2. Create user interfaces with charts, graph and buttons
3. Use the programming structures and data types that exist in Lab VIEW
4. Use various editing and debugging techniques

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.

The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI, 2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGraw Hill, Second Edition, 2011.

IV Semester

<table>
<tr><th colspan="4">Maths for Communication Engineers</th></tr>
<tr><td>Course Code</td><td>21MAT401</td><td>CIE Marks</td><td>50</td></tr>
<tr><td>Teaching Hours/Week (L:T:P:S)</td><td>3:0:0:1</td><td>SEE Marks</td><td>50</td></tr>
<tr><td>Total Hours of Pedagogy</td><td>40</td><td>Total Marks</td><td>100</td></tr>
<tr><td>Credits</td><td>3</td><td>Exam Hours</td><td>3</td></tr>
<tr><td colspan="4">Course objectives:
To facilitate the students in understanding the Concepts of Electric and Magnetic Fields through Mathematical representations.
To enable the students in using the concepts of Field theory to arrive at important Mathematical relations associated with Electromagnetic waves.
To provide a foundation in Random variables and Random Processes which find application in Communication.</td></tr>
<tr><td colspan="4">Teaching-Learning Process (General Instructions)
The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:
Explain the importance of Mathematics in Communication links and Prerequisites of the course.
Prepare handouts of related problems and encourage the doubts.
Prepare assignment questions related to theory and problems.
Prepare concept-based quiz questions.
Encourage short videos available on web related to important topics of Digital Signal Processing.
Encourage Students to create a forum wherein they can discuss theoretical concepts and problems.</td></tr>
<tr><td colspan="4">Prerequisites:
[i] Vector Analysis – Scalars and Vectors, Vector Algebra, Rectangular, Cylindrical and Spherical Coordinate system, Vector components and Unit vectors, Scalar and Vector fields, Dot product, cross product, Vector differentiation, Vector integration [Revise Module-2 of 21MAT21 course]
[ii] Probability Basics- Why Probability? Axioms and Properties of Probability, Finding Probability Values, Conditional Probabilities and Independence, Independence among n events, Partitions</td></tr>
<tr><td colspan="4">Module-1: Static Electric Field and Flux Density</td></tr>
<tr><td colspan="4">Coulomb's Law and Electric Field Intensity: The Experimental law of Coulomb, Electric Field Intensity, Field of a line charge
Electric Flux Density and Gauss-Divergence Theorem: Electric Flux Density, Gauss' Law, Application of Gauss' Law for a Differential Volume Element, Divergence, Maxwell's First Equation, Divergence Theorem (From Text-1)</td></tr>
<tr><td>Teaching-Learning Process</td><td colspan="3">Chalk and talk method/Power point presentation
Self-Study: Electric Field of a Sheet of Charge
RBT Level: L1, L2, L3</td></tr>
<tr><td colspan="4">Module-2: Electric Potential, Current Density and Steady Magnetic Field</td></tr>
<tr><td colspan="4">Electric Potential: Energy Expended in moving a point charge in an Electric field, The Line Integral, Definition of Potential Difference and Potential, Potential field of a point charge, Potential Gradient
Current Density: Current and Current Density, Current Continuity Equation
Steady Magnetic field: Biot-Savart's Law, Ampere's Circuital Law (Statement, Illustration and Mathematical representation), Curl, Stokes' Theorem, Magnetic Flux and Flux density (From Text-1)</td></tr>
</table>

Teaching-Learning Process	Chalk and talk method/Power point presentation **Self-Study:** Conductor Properties and Boundary Conditions, Scalar and Vector Magnetic Potential **RBT Level:** L1, L2, L3

Module-3: Time Varying Fields, Maxwell's Equations and Uniform Plane Wave

Time Varying Fields and Maxwell's Equations: Faraday's Law, Displacement Current, Maxwell's Equations in Point Form, Maxwell's Equations in Integral Form
Uniform Plane Wave: Wave Propagation in Free Space, Wave Propagation in Dielectrics, Poynting's Theorem and Wave Power, Propagation in Good Conductors: Skin Depth (From Text-1)

Teaching-Learning Process	Chalk and talk method/Power point presentation **Self-Study:** Reflection of Uniform Plane Waves at Normal Incidence, Standing Wave Ratio **RBT Level:** L1, L2, L3

Module-4: Single Random Variables

Single Random Variables: Definition of Random Variables, Cumulative Distribution Function, Continuous and Discrete Random Variables, Expectations, Characteristic Functions, Functions of Single Random Variables, Conditioned Random Variables (From Text-2)

Teaching-Learning Process	Chalk and talk method/Power point presentation **Self-Study:** Multiple Random Variables **RBT Level:** L1, L2, L3

Module-5: Random Processes

Random Processes: Ensemble, PDF, Independence, Expectations, Stationarity, Correlation Functions (ACF, CCF, Addition and Multiplication), Ergodic Random Processes, Power Spectral Densities (Wiener Khinchin, Addition and Multiplication of RPs, Cross Spectral Densities), Linear Systems (Output Mean, Cross-Correlation and Autocorrelation of Input and Output), Noise (From Text-2)

Teaching-Learning Process	Chalk and talk method/Power point presentation **Self-Study:** Matched Filters **RBT Level:** L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Recall the basic laws and definitions (with mathematical representations) in Electric and Magnetic fields.
2. Apply the basic laws of Electric and Magnetic fields to arrive at Divergence Theorem, Current continuity Equation, Curl, Stokes' theorem.
3. Apply Electric and Magnetic field concepts to arrive at Maxwell's equations, Electromagnetic wave equations and Poynting's theorem (Important concepts related to Communication link).
4. Recall the definitions related to Random variables and Random Processes.
5. Model the Random events in the Communication set-up and determine useful statistical parameters.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester

2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Books:

1. W H Hayt and J A Buck, "Engineering Electromagnetics", Mc Graw Education, 8th Edition, 2014.
2. Richard H Williams, "Probability, Statistics, and Random Processes for Engineers", Cengage Learning, Second Indian Reprint, 2019.

Reference Books:

1. Mathew N O Sadiku, "Elements of Electromagnetics", Oxford University Press, 4th edition, 2007.
2. Joseph A Edminister, "Electromagnetics", Schaum's Outlines, Revised 2nd Edition, 2017.
3. E C Jordan and K G Balmain, "Electromagnetic Waves and Radiating Systems ", Pearson, 2nd Edition, 2015.
4. Hwei P Hsu, "Theory and Problems of Probability, Random Variables and Random Processes", Schaum's Outlines, Mc Graw Hill, 2017.
5. K N Hari Bhat, K Anitha Sheela and Jayant Ganguly, "Probability Theory and Stochastic Processes for Engineers", Cengage Learning, 2019.

Web links and Video Lectures (e-Resources)

- https://nptel.ac.in/courses/108106073
- https://archive.nptel.ac.in/courses/117/105/117105085

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Form multiple teams in the class and suggest them to prepare charts/models/animations or conduct an interactive quiz based on concepts of the course.

Sub Title : Digital Signal Processing		
Sub Code: 21ECT402	**No. of Credits: 4=3 : 0 : 2 (L-T-P)**	**No. of lecture hours/week : 05**
Exam Duration :3 Hours	**CIE +Group Activity Assignment +SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. **Preparation:** To prepare students with fundamental knowledge/ overview in the field of Digital Signal Processing.
2. **Core Competence:** To equip students with a basic foundation of Signal Processing by delivering the basics of Discrete Fourier Transforms & their properties, design of filters and overview of digital signal processors.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level
1	**Discrete Fourier Transforms (DFT):** Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation. 1. **Properties of the DFT:** Periodicity, Linearity and Symmetry properties, circular time shift & circular frequency shift property, Multiplication of two DFTs and Circular Convolution [Text 1]	09	L1, L2, L3.
2	**Linear filtering methods based on the DFT:** Use of DFT in Linear Filtering, Filtering of Long data Sequences. **Fast-Fourier-Transform (FFT) algorithms:** Efficient Computation of the DFT: Radix-2 FFT algorithms: DIT-FFT and DIF-FFT for the computation of DFT and IDFT [Text 1]	09	L1, L2,L3
3	**Design of FIR Filters:** Characteristics of practical frequency-selective filters, Symmetric and Anti- symmetric FIR filters, Design of Linear-phase FIR (low pass and High pass) filters using windows - Rectangular, Hamming, Hanning and Bartlett windows. **Structure for FIR Systems:** Direct form, Cascade form and Lattice structures [Text1] [Text 2]	11	L1,L2,L3
4	**IIR Filter Design:** Infinite Impulse response filter format, Bilinear Transformation Design method: Analog Filters using Low pass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth (Lowpass and Highpass) Filter Design using BLT. **Realization of IIR Filters:** Direct form I and II [Text 2]	11	L1,L2,L3
5	**Digital Signal Processors:** DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, FIR and IIR filter implementations in Fixed point systems. [Text 2]	12	L1,L2,L3

PRACTICAL COMPONENT OF IPCC
List of Programs to be implemented & executed using any programming languages like C++/Python/Java/Scilab / MATLAB/CC Studio (but not limited to) 1. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum. 2. Computation of circular convolution of two given sequences and verification of commutative, distributive and associative property of convolution. 3. Computation of linear convolution of two sequences using DFT and IDFT. 4. Computation of circular convolution of two given sequences using DFT and IDFT 5. Verification of Linearity property, circular time shift property & circular frequency shift property of DFT. 6. Design and implementation of IIR (Butterworth) low pass filter to meet given specifications. 7. Design and implementation of IIR (Butterworth) high pass filter to meet given specifications. 8. Design and implementation of low pass FIR filter to meet given specifications. 9. Design and implementation of high pass FIR filter to meet given specifications. 10. To compute N- Point DFT of a given sequence using DSK 6713 simulator 11. To compute linear convolution of two given sequences using DSK 6713 simulator 12. To compute circular convolution of two given sequences using DSK 6713 simulator

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Determine response of LTI systems using time domain and DFT techniques
2. Compute DFT of real and complex discrete time signals
3. Compute DFT using FFT algorithms
4. Design FIR and IIR Digital Filters
5. Design of Digital Filters and processing of digital signals using DSP processor

Note 1: Unit 1, 2, 3, 4 and Unit 5 will have internal choice.
Note 2: Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2 Assignment - 2 from units 3, 4 and 5.
Note 3: Teaching-Learning Process: Chalk and Talk, YouTube videos, Programming assignments
Note 4: The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated only by CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.

Cos	Mapping with POs	Mapping with PSOs
CO1	PO1,PO2,PO3	PSO1,PSO2,PS03
CO2	PO1,PO2,PO4,PO8,PO9,PO12	PSO1,PSO2,PS03
CO3	PO1,PO2,PO3,PO4,PO5,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03
CO4	PO1,PO2,PO3,PO4,PO5,PO6,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03
CO5	PO1,PO2,PO3,PO4,PO5,PO6,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03

Text Books:	
1.	Proakis & Manolakis, "Digital Signal Processing - Principles Algorithms & Applications", 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2.	Li Tan, Jean Jiang, "Digital Signal processing - Fundamentals and Applications", Academic Press, 2013, ISBN: 978-0-12-415893.

Reference Books:	
1.	Sanjit K Mitra, “Digital Signal Processing, A Computer Based Approach”, 4th Edition, McGraw Hill Education, 2013.
2.	Oppenheim & Schaffer, “Discrete Time Signal Processing", PHI, 2003.
3.	D Ganesh Rao and Vineeth P Gejji, “Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

Web Links:	
1.	By Prof. S. C. Dutta Roy, IIT Delhi https://nptel.ac.in/courses/117102060
2.	MIT OpenCourseWare https://youtu.be/rkvEM5Y3N60

Subject Title : Circuit analysis and control systems

Sub.Code: 21ECT403	**No. of Credits:4=2:1:1 (L - T– P)**	**No. of Lecture Hours/Week : 06**
Exam Duration:03 Hrs	**CIE+Assignment +SEE=45+5+50=100**	**Total No.of Contact Hours:78**

Course Learning Objectives:

From this course, the students can learn

1 Network analysis techniques and theorems for solving the electrical circuits

2 Applying Laplace transforms to analyse electrical circuits and two port network concepts.

3 The feedback control systems and modelling of the control systems in DEs and Transfer function approach.

4 The time response of control systems and examining the stability of control systems.

5 Analysis of control systems using root-locus and bode-plots.

6 State variable modeling of control systems.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Basic Circuit Concepts:** Ideal and Practical sources, Network reduction using Source transformations, Source Shifting and Star Delta transformation, duality of networks, Loop and Nodal analysis with linearly dependent and independent sources for both DC and AC networks, Concepts of super node and super mesh analysis, Numerical examples. **Network Theorems:** Thevenin's Theorem, Norton's Theorem, Superposition Theorem, Reciprocity Theorem, Maximum Power transfer theorem. Numerical examples *TEXT 1.*	10	L1,L2,L3.L4
2	**Laplace Transforms:** Introduction, Properties and theorems of Laplace Transforms, DC response of electrical circuits with and without initial conditions. **Two port network parameters:** Definitions of Z,Y,T and h- parameters, modeling of two port network parameters, Conditions for Symmetry and Reciprocity, series, parallel and Cascade Connection of Two Port Networks. *TEXT 1.*	10	L1,L2,L3.L4
3	**Introduction to Control systems:** Introduction**,** Types of Control systems, Effect of feedback systems and requirements of good control systems: **Mathematical Modeling of Control Systems:** Modeling of mechanical systems (Rotational and Translational excluding Lever and Gear trains systems). Transfer functions (Multivariable systems), Modeling of Electrical systems (Current and voltage analogy) Electromechanical Systems and its Analogous systems and DC Motors (Armature and Field controlled). **Block diagrams:** Block diagram of a closed loop systems and its reduction techniques, Transfer Functions (Multivariable Systems), Applications of Block diagram **Signal Flow Graphs:** Mason's gain formula, Basic properties of Signal flow graph, Transfer Functions-(Multivariable systems), Construction of Signal	10	L1,L2,L3.L4

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	flow graph for closed loop control systems, and Applications of Signal Flow Graphs. *TEXT 2.*		
4	**Time Response of feedback control systems:** Time response of control systems**,** Standard test signals, Unit step response of First and Second order Systems. Time response specifications and its derivations, Time response specifications of second order systems, steady state errors and Error constants. Types of control systems(Steady state error for Type 0,1 and 2 systems) **Stability analysis:** Concepts of stability, Necessary conditions for Stability, Routh stability criterion, Difficulties in the formulation of the Routh table, Relative stability analysis *TEXT 2.*	10	L1,L2,L3.L4
5	**Root Locus:** Introduction, Root locus concepts, Construction of Root loci, Rules for the construction of Root-Locus (negative feedback systems), Numerical examples. **Frequency responses analysis:** Introduction, Frequency domain specifications (No derivations, Numerical examples), Correlation between time and frequency response for second order systems. Bode plots, General procedure for constructing the Bode plots (Basic factors), Calculation of transfer function from Magnitude plot, Computation of Gain and Phase Margins from Bode plot, Gain adjustment in Bode Plot. **State Space Analysis:** Introduction, Concept of State, State variables & State model, State space representation for dynamic systems (Phase variables and Canonical Variables), Solution of state equations. *TEXT2.*	12	L1,L2,L3.L4

Note 1: Unit 3 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

After successful completion of this course, the students will be able to

CO1: Apply Network analysis techniques and network theorems to solve electrical circuits.
CO2: Analyze electrical circuits using Laplace transforms and explain two port network parameters.
CO3: Obtain mathematical model (both DE and TF approach) and analogous systems for the given systems.
CO4: Explain time response of control systems and examine stability using RH criterion
CO5: Analyze the stability of control systems using Root-Locus and Bode-plots method, and obtain the state space models for the given systems.

Text Books.

1 Charles K Alexander and Mathew N O Sadiku, "Fundamentals of Electric Circuits", 3rd edition, Tata McGraw-Hill, 2009.

2 J.Nagarath and M.Gopal, "Control Systems Engineering", 5th Edition, New Age International (P) Limited Publishers, 2005

Reference Text Books.

1 K.Ogata, "Modern Control Engineering", 4th Edition, Pearson Education Asia/PHI, 2002.
2 Benjamin C. Kuo, "Automatic Control Systems" , 9th Edition, John Wiley India Pvt. Ltd., 2008
3 Joseph J Distefano III et al., "Feedback and Control System", 2nd Edition, Schaum's Outlines, TMH, 2007.
4 Roy Choudhury, "Networks and systems", 2nd edition, New Age International Publications, 2006
5 M.E. Van Valkenberg, "Network analysis", 3rd edition, Prentice Hall of india Publishers, 2000

Web Links.

1 https://www.electrical4u.com/mathematical-modelling-of-various-system/.
2 https://www.tutorialspoint.com/control_systems/control_systems_time_response_analysis.htm.
3 www.facstaff.bucknell.edu/mastascu/econtrolhtml/rootlocus/rlocus1a.html.
4 lpsa.swarthmore.edu/Bode/BodeExamples.html.
5 https://www.calvin.edu/~pribeiro/courses/engr332/Handouts/nyquist-margins.htm.
6 nptel.ac.in/courses/108103008/25.

COs	POs	PSOs
CO1	PO1, PO2, PO3, PO5	PSO1, PSO2
CO2	PO1, PO2, PO3, PO5	PSO1, PSO2
CO3	PO1, PO2, PO3, PO5	PSO1, PSO2
CO4	PO1, PO2, PO3, PO5	PSO1, PSO2
CO5	PO1, PO2, PO3, PO5	PSO1, PSO2

Practical Component

Sl. No.	Experiments
1	Verification of Superposition theorem using PSPICE
2	Verification of Thevenin's theorem using PSPICE
3	Verification of Norton's theorem using PSPICE
4	Determination of time response of second order systems using PSPICE.
5	Draw root locus using MATLAB
6	Draw BODE PLOTs using MATLAB
7	Study the effect of PI controller using MATLAB
8	Study the effect of PD controller using MATLAB
9	Study the effect of PID controller using MATLAB
10	Study of speed characteristics of DC motors using MATLAB.

******

Sub Title : Communication Theory		
Sub Code: 21ECT404	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity +Assignment +SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand and analyse concepts of Analog Modulation schemes viz; AM, FM., Low passsampling and Quantization as a random process.
2. Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.
3. Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.
4. Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at a receiver.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**AMPLITUDE MODULATION:** Introduction, Amplitude Modulation: Time & Frequency Domaindescription, switching modulator, Envelop detector. **DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION:** Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. **SINGLE SIDE–BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION:** SSB Modulation, VSB Modulation, Frequency Translation, Frequency Division Multiplexing. [Text1: 3.1 to 3.8]	09	L1, L2, L3.
2	**ANGLE MODULATION:** Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM,Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase–Locked Loop: Nonlinear model of PLL, Linear model of PLL. The Super Heterodyne Receiver [Text1: 4.1 to 4.6]	08	L1, L2,L3
3	**NOISE**: Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth. **NOISE IN ANALOG MODULATION**: Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Pre-emphasis and De-emphasis in FM (Text1: 5.10, 6.1 to 6.6)	08	L1,L2,L3
4	**SAMPLING AND QUANTIZATION:** Introduction, Why Digitize Analog Sources? The Low Pass Sampling Process, Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves. (Text1: 7.1 to 7.7)	07	L1,L2,L3
5	**SAMPLING AND QUANTIZATION (Contd):** The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation (Text1: 7.8 to 7.10), Application examples - (a) Video + MPEG (Text1:7.11) and (b) Vocoders (refer Section 6.8 of Reference Book 1)	07	L1,L2,L3

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

At the end of the course the student will be able to:

CO1. Able to understand and analyze modulation and demodulation techniques for AM, DSBSC, SSB-SC andVSB-SC.

CO2. Able to understand and analyze modulation and demodulation techniques for Angle Modulation.

CO3. Able to characterize the influence of channel noise on analog modulated signals.

CO4. Able to understand and analyze Sampling of Low pass signals, pulse amplitude modulation, pulse position modulation

CO5. Able to understand and analyze PCM, Quantization and Delta Modulation. Illustration of digital formattingrepresentations used for Multiplexers, Vocoders and Video transmission.

Cos	Mapping with POs	Mapping with PSOs
CO1	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12	PSO1,PSO2
CO2	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12	PSO1,PSO2
CO3	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12	PSO1,PSO2
CO4	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12	PSO1,PSO2
CO5	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12	PSO1,PSO2

Text Book:

1. Simon Haykins & Moher, **"Communication Systems"**, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books:

1. B P Lathi and Zhi Ding, **"Modern Digital and Analog Communication Systems"**, Oxford University Press., 4th edition, 2010, ISBN: 97801980738002
2. S *y* India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3. H Taub & D L Schilling, **"Principles of Communication Systems"**, TMH, 2011.

Web Links: www.nptel.in

Communication Laboratory I			
Course Code	**21ECL405**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Model an analog communication system signal transmission and reception.
- Realize the electronic circuits to perform analog and pulse modulations and demodulations.
- Verify the sampling theorem and relate the signal and its spectrum before and after sampling.
- Understand the process of PCM and delta modulations.
- Understand the PLL operation.

Sl.No.	Experiments
1	Design of active second order Butterworth low pass and high pass filters.
2	Amplitude Modulation and Demodulation of (a) Standard AM and (b) DSBSC (LM741 and LF398 ICs can be used)
3	Frequency modulation and demodulation
4	Design and test Time Division Multiplexing and Demultiplexing of two bandlimited signals.
5	Design and test i) Pulse sampling, flat top sampling and reconstruction. ii) Pulse amplitude modulation and demodulation.
6	Design and test BJT/FET Mixer
7	Pulse Code Modulation and demodulation
8	Phase locked loop Synthesis
9	Illustration of (a) AM modulation and demodulation and display the signal and its spectrum. (b) DSB-SC modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)
10	Illustration of FM modulation and demodulation and display the signal and its spectrum. (Use MATLAB/SCILAB)
11	Illustrate the process of sampling and reconstruction of low pass signals. Display the signals and its spectrums of both analog and sampled signals. (Use MATLAB/SCILAB).
12	Illustration of Delta Modulation and the effects of step size selection in the design of DM encoder. (Use MATLAB/SCILAB)

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Demonstrate the AM and FM modulation and demodulation by representing the signals in time and frequency domain.
2. Design and test the sampling, Multiplexing and PAM with relevant circuits.
3. Demonstrate the basic circuitry and operations used in AM and FM receivers.
4. Illustrate the operation of PCM and delta modulations for different input conditions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.
(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours.

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Louis E Frenzel, Principles of Electronic Communication Systems, McGraw Hill Education (India) Private Limited, 2016.
2. B P Lathi, Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press, 2015.

Embedded C Basics			
Course Code	**21ECT4081**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

- Understand the basic programming of Microprocessor and microcontroller.
- To develop the microcontroller-based programs for various applications.

Sl.No	Experiments
	Conduct the following experiments by writing C Program using Keil microvision simulator (any 8051 microcontroller can be chosen as the target).
1	Write a 8051 C program to multiply two 16 bit binary numbers.
2	Write a 8051 C program to find the sum of first 10 integer numbers.
3	Write a 8051 C program to find factorial of a given number.
4	Write a 8051 C program to add an array of 16 bit numbers and store the 32 bit result in internal RAM
5	Write a 8051 C program to find the square of a number (1 to 10) using look-up table.
6	Write a 8051 C program to find the largest/smallest number in an array of 32 numbers
7	Write a 8051 C program to arrange a series of 32 bit numbers in ascending/descending order
8	Write a 8051 C program to count the number of ones and zeros in two consecutive memory locations.
9	Write a 8051 C program to scan a series of 32 bit numbers to find how many are negative.
10	Write a 8051 C program to display "Hello World" message (either in simulation mode or interface an LCD display).
11	Write a 8051 C program to convert the hexadecimal data 0xCFh to decimal and display the digits on ports P0, P1 and P2 (port window in simulator).

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Write C programs in 8051 for solving simple problems that manipulate input data using different instructions of 8051 C.
2. Develop testing and experimental procedures on 8051 Microcontroller, analyze their operation under different cases.
3. Develop programs for 8051 Microcontroller to implement real world problems.
4. Design and Develop Mini projects

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.

Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.

Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).

Weightage to be given for neatness and submission of record/write-up on time.

Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.

In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

The suitable rubrics can be designed to evaluate each student's performance and learning ability.

Rubrics suggested in Annexure-II of Regulation book

The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

"The 8051 Microcontroller: Hardware, Software and Applications", V Udayashankara and M S Mallikarjuna Swamy, McGraw Hill Education, 1st edition, 2017.

IV Semester

C++ Basics			
Course Code	**21ECT4082**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

- Understand object-oriented programming concepts, and apply them in solving problems.
- To create, debug and run simple C++ programs.
- Introduce the concepts of functions, friend functions, inheritance, polymorphism and function overloading.
- Introduce the concepts of exception handling and multithreading.

Sl.No	Experiments
1	Write a C++ program to find largest, smallest & second largest of three numbers using inline functions MAX & Min.
2	Write a C++ program to calculate the volume of different geometric shapes like cube, cylinder and sphere using function overloading concept.
3	Define a STUDENT class with USN, Name & Marks in 3 tests of a subject. Declare an array of 10 STUDENT objects. Using appropriate functions, find the average of the two better marks for each student. Print the USN, Name & the average marks of all the students.
4	Write a C++ program to create class called MATRIX using two-dimensional array of integers, by overloading the operator == which checks the compatibility of two matrices to be added and subtracted. Perform the addition and subtraction by overloading + and – operators respectively. Display the results by overloading the operator <<. If (m1 == m2) then m3 = m1 + m2 and m4 = m1 – m2 else display error
5	Demonstrate simple inheritance concept by creating a base class FATHER with data members: *First Name, Surname, DOB & bank Balance* and creating a derived class SON, which inherits: Surname & Bank Balance feature from base class but provides its own feature: First Name & DOB. Create & initialize F1 & S1 objects with appropriate constructors & display the FATHER & SON details.
6	Write a C++ program to define class name FATHER & SON that holds the income respectively. Calculate & display total income of a family using Friend function.
7	Write a C++ program to accept the student detail such as name & 3 different marks by get_data() method & display the name & average of marks using display() method. Define a friend function for calculating the average marks using the method mark_avg().
8	Write a C++ program to explain virtual function (Polymorphism) by creating a base class polygon which has virtual function areas two classes rectangle & triangle derived from polygon & they have area to calculate & return the area of rectangle & triangle respectively.
9	Design, develop and execute a program in C++ based on the following requirements: An EMPLOYEE class containing data members & members functions: i) Data members: employee number (an integer), Employee_ Name (a string of characters), Basic_ Salary (in integer), All_ Allowances (an integer), Net_Salary (an integer). (ii) Member functions: To read the data of an employee, to calculate Net_Salary & to print the values of all the data members. (All_Allowances = 123% of Basic, Income Tax (IT) =30% of gross salary (=basic_ Salary_All_Allowances_IT).
10	Write a C++ program with different class related through multiple inheritance & demonstrate the use of different access specified by means of members variables & members functions.

11	Write a C++ program to create three objects for a class named count object with data members such as roll_no & Name. Create a members function set_data ( ) for setting the data values & display ( ) member function to display which object has invoked it using „this" pointer.
12	Write a C++ program to implement exception handling with minimum 5 exceptions classes including two built in exceptions.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Write C++ program to solve simple and complex problems
2. Apply and implement major object-oriented concepts like message passing, function overloading, operator overloading and inheritance to solve real-world problems.
3. Use major C++ features such as Templates for data type independent designs and File I/O to deal with large data set.
4. Analyze, design and develop solutions to real-world problems applying OOP concepts of C++

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Object oriented programming in TURBO C++, Robert Lafore, Galgotia Publications, 2002
2. The Complete Reference C++, Herbert Schildt, 4th Edition, Tata McGraw Hill, 2003.
3. Object Oriented Programming with C++, E Balaguruswamy, 4th Edition, Tata McGraw Hill, 2006.

IV Semester

Octave / Scilab for Signals			
Course Code	**21ECT4083**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

1. **Preparation**: To prepare students with fundamental knowledge/ overview in the field of signals and processing.
2. **Core Competence**: To equip students with a basic foundation in electronic engineering and mathematics fundamentals required for comprehending the operation and application of signal processing.
3. **Professionalism & Learning Environment**: To inculcate in students an ethical and professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context, and life-long learning needed for a successful professional career.

Sl.No	Experiments
1	Verify the Sampling theorem.
2	Determine linear convolution, Circular convolution and Correlation of two given sequences. Verify the result using theoretical computations.
3	Determine the linear convolution of two given point sequences using FFT algorithm. Verify the result using theoretical computations.
4	Determine the correlation using FFT algorithm. Verify the result using theoretical computations.
5	Determine the spectrum of the given sequence using FFT. Verify the result using theoretical computations.
6	Design and test FIR filter using Windowing method (Hamming, Hanning and Rectangular window) for the given order and cut-off frequency.
7	Design and test IIR Butterworth 1^{st} and 2^{nd} order low & high pass filter.
8	Design and test IIR Chebyshev 1^{st} and 2^{nd} order low & high pass filter.
9	Generation of an AM – Suppressed Carrier Wave & visualization of the time domain and frequency domain plots.
10	Generation and visualization of standard test signals (both continuous and discrete time).
11	Generation and visualization of audio signal (pre-recorded) and generation of echo.
12	Generation and visualization of the STFT of a chirp (and other related) signal.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Demonstrate the DSP concepts on signal generation and sampling using Scilab/Octave
- Design and verify the computation of discrete signals using Scilab/Octave.
- Demonstrate and verify the application of FFT/DFT algorithm for a given signal using Scilab/Octave.
- Design and demonstrate programs to evaluate different types of low and high pass FIR filters using Scilab/Octave.
- Design, demonstrate and visualize different real world signals using Scilab/Octave programs.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.

Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.

Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).

Weightage to be given for neatness and submission of record/write-up on time.

Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.

In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

The suitable rubrics can be designed to evaluate each student's performance and learning ability.

Rubrics suggested in Annexure-II of Regulation book

The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

Digital Signal Processing Using MATLAB, John G Proakis and Vinay K Ingle, Cengage Learning, 2011

IV Semester

DAQ using LabVIEW			
Course Code	**21ECT4084**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	100

Course objectives:

- Process the knowledge of loop constructs.
- Fundamentals of graphical programming and use LabVIEW modules
- Implement 'Timing' functions.
- Input algebraic formulas via 'Formula Nodes' and 'Expression Nodes'.

Sl.No	Experiments
1	Data acquisition using LabVIEW for temperature measurement with thermocouple.
2	Data acquisition using LabVIEW for temperature measurement with AD590.
3	Data acquisition using LabVIEW for temperature measurement with RTD.
4	Data acquisition using LabVIEW for temperature measurement with Thermistor.
5	Creation of a CRO using LabVIEW and measurement of frequency and amplitude from external source.
6	Create function generator using LabVIEW and display the amplitude and frequency on CRO (externally connected)
7	Demonstrate amplitude modulation considering modulating and carrier wave from external source.
8	Interface LEDs to DAQ output and implement counter.
9	Data acquisition using LabVIEW for load / strain measurement using suitable transducers.
10	Demonstrate binary to grey code converter (& vice versa) using DAQ card.
11	Data acquisition using LabVIEW for distance/humidity measurement using suitable transducers.
12	Reading audio input with Microphones and output using DAQ card.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Build temperature indicating instruments using LabVIEW (NI DAQ)
2. Interface peripheral devices/instruments to LabVIEW
3. Build LabVIEW modules to sense and process audio inputs
4. Apply programming structures, data types, and the analysis and signal processing algorithms in LabVIEW
5. Debug and troubleshoot applications

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.

The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI, 2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGraw Hill, Second Edition, 2011.

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

V Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	PCC	21ECT501	Digital Communication	ECE	3	0	0			3	50	50	100	3
2	IPCC	21ECT502	Microprocessor & Microcontrollers	ECE	3	0	2		3	3	50	50	100	4
3	PCC	21ECT503	Computer Communication Networks	ECE	3	0	0		3	3	50	50	100	3
4	PCC	21ECT504	Microwave Theory & Antennas	ECE	3	0	0		3	3	50	50	100	3
5	PCC	21ECL505	Communication Lab II	ECE	0	0	2		3	3	50	50	100	1
6	AEC	21ECT506	Research Methodology & Intellectual Property Rights	Any Department	2	0	0		2	2	50	50	100	2
7	HSSC	21CV507	Environmental Studies	Civil/Chemistry	1	0	0			1	50	50	100	1
8	AEC	21ECT508	Ability Enhancement Course-V	ECE						1/2	50	50	100	1
9	HSSC	21HSN509	Aptitude and Verbal ability skills		1	0	1	0		2	50	--	PP/NP	0
										Total	450	400	800	18

Ability Enhancement Course - V

21ECL5081	Computer Communication Networks Lab	**21ECL5083**	Antenna Design & Testing
21ECL5082	Communication Simulink Toolbox	**21ECL5084**	Microwaves toolbox

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

VI Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	HSSC	21ECT601	Technological Innovation Management and Entrepreneurship								50	50	100	03
2	IPPC	21ECT602	Computer Organization & ARM Microcontrollers	ECE	2	2			4	3	50	50	100	04
3	PCC	21ECT603	VLSI Design & Testing	ECE	3				3	3	50	50	100	03
4	PEC	21ECE604X	Professional Elective -I	ECE	3				3	3	50	50	100	03
5	OEC	21ECE605X	OpenElective-I	ECE	3				3	3	50	50	100	03
6	PCC	21ECL606	VLSI Laboratory	ECE			2		2		50	50	100	01
7	MP	21ECM607	Mini Project	ECE			2		2		50	50	100	03
8	INT	21ECI608	Innovation/Entrepreneurship /Societal Internship								50	50	100	03
9	HSSC	21HSN609	Analytical & Reasoning skills	Placement Cells	2	0	0-		02	--	50	--	PP/NP	00
								Total			500	450	900	22

Research/Industrial Internship - At the End of the sixth / Seventh semester (in two cycles to accommodate all the students of the University) Research/Industrial Internship shall be carried out – Based on industrial/Govt./NGO/MSME/Rural Internship/Innovation/Entrepreneurship. All the students admitted shall have to undergo a mandatory internship of 24 weeks during the vacation of VI/VII semesters. A University Viva-Voce examination shall be conducted during VII/VIII semester and the prescribed credit shall be included in VII/VIII semester. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements. Research internship Students have to take up research internships at Centers of Excellence (CoE) / Study Centers established in the same institute and /or out of the institute at reputed research organizations / Institutes. A research internship is intended to give you the flavour of current research going on on a particular topic/s. The internships serve this purpose. They help students get familiarized with the field, the skill needed the effort amount and kind of effort required for carrying out research in that field.

Industry internships: This is an extended period of work experience undertaken by university/Institute students looking to supplement their degree with professional development. The students are allowed to prepare themselves for the workplace and develop practical skills as well as academic ones. It also helps them learn to overcome

unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with "unexpected contingencies" helps students recognize, appreciate, and adapt to organization realities by tempering knowledge with practical constraints.

Mini-project work: Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini-project can be assigned to an individual student or a group having not more than 4 students. (or Mini Project is a laboratory-oriented course which will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications) CIE procedure for
Mini-project: (i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide. The CIE marks awarded for the Mini-project work, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.
(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the college. The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batch mates. SEE for Mini-project: (i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester-end examination (SEE) conducted at the department. (ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester-end examination (SEE) conducted separately at the departments to which the student/s belongs
Open Elective Courses: Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives). Selection of an open elective shall not be allowed if, • The candidate has studied the same course during the previous semesters of the program. • The syllabus content of open electives is similar to that of the Departmental core courses or professional electives. • A similar course, under any category, is prescribed in the higher semesters of the program. • Registration to electives shall be documented under the guidance of the Programme Coordinator/ Advisor/Mentor

Professional Elective Courses-I		**Open Elective Courses-I**	
Subject Code	**Title**	**Subject Code**	**Title**
21ECE6041	Artificial Neural Networks (L:T:P :: 2:2:0)	**21ECE6051**	Communication Engineering (L:T:P :: 3:0:0)
21ECE6042	Cryptography (L:T:P :: 2:2:0)	**21ECE6052**	Microcontrollers (L:T:P :: 3:0:0)
21ECE6043	Python Programming (L:T:P :: 2:0:2)	**21ECE6053**	Basic VLSI Design (L:T:P :: 3:0:0)
21ECE6044	Micro Electro Mechanical Systems (L:T:P :: 3:0:0)	**21ECE6054**	Electronic Circuits with Verilog (L:T:P :: 2:0:2)
		21ECE6055	Sensors & Actuators (L:T:P :: 3:0:0)

V Semester

DIGITAL COMMUNICATION			
Course Code:	21ECT501	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:2	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	3	**Exam Hours:**	3

Course objectives:

1. Understand the mathematical representation of signal, symbol, and noise.
2. Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
3. Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
4. Compute performance parameters and mitigate channel induced impediments in corrupted channel conditions.

Module-1

Bandpass Signal to Equivalent Low pass:

Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low pass representation of bandpass systems, Complex representation of band pass signals and systems (Text 1: 2.8, 2.9, 2.10, 2.11, 2.12, 2.13).

Line codes: Unipolar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities (Text 1: Ch 6.10). Overview of HDB3, B3ZS, B6ZS (Ref.1: 7.2)

Teaching Learning Method:	Lectures, Interactive (Q & A discussion), Activity/Assignment based
RBT Level:	L1, L2, L3

Module-2

Signaling over AWGN Channels-

Introduction, Geometric representation of signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver.

(Text 1:7.1, 7.2, 7.3, 7.4)

Teaching Learning Method:	Lectures, Interactive (Q&A discussion), Activity/Assignment based
RBT Level:	L1, L2, L3, L4

Module-3

Digital Modulation Techniques:

Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M ary PSK, M-ary QAM. (Relevant topics in Text 1of 7.6, 7.7).

Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability (Relevant topics in Text 1of 7.8).

Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivation of probability of error equation) (Text 1: 7.11, 7.12. 7.13).

Teaching Learning Method:	Lectures, Interactive (Q&A discussion), Activity/Assignment based
RBT Level:	L1, L2, L3, L4

Module-4

Communication through Band Limited Channels:

Digital Transmission through Band limited channels: Digital PAM Transmission through Band limited Channels, Signal design for Band limited Channels: Design of band limited signals for zero lSI-The Nyquist Criterion (statement only), Design of band limited signals with controlled lSI-Partial Response signals, Probability of error for detection of Digital PAM: Probability of error for detection of Digital PAM with Zero lSI, Symbol-by-Symbol detection of data with controlled lSI (Text 2: 9.1, 9.2, 9.3.1, 9.3.2). Channel Equalization: Linear Equalizers (ZFE, MMSE), (Text 2: 9.4.2).

Teaching Learning Method:	Lectures, Interactive (Q&A discussion), Activity/Assignment based
RBT Level:	L1, L2, L3, L4

Module-5

Principles of Spread Spectrum:

Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95 (Text 2: 11.3.1, 11.3.2, 11.3.3, 11.3.4, 11.3.5, 11.4.2).

Teaching Learning Method:	Lectures, Interactive (Q&A discussion), Activity/Assignment based
RBT Level:	L1,L2,L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Understand the representation of bandpass signals into its' equivalent low pass signals and properties of various line code formats and their usage.

CO2. Analyse and compute the performance parameters of two different receiver architectures when low-pass and band pass symbol sets defined over symbol period are transmitted over noisy and noiseless bandlimited channel.

CO3. Generate and Evaluate different M-ary symbol sets on performance parameters at the receiver side under ideal and corrupted bandlimited channels.

CO4. Demonstrate the digital transmission of bandpass signals through bandlimited channels incorporating signal design processed at the receiver to meet specified performance criteria.

CO5. Understand the principles of spread spectrum communications to identify its application to recent communication systems in use today.

Suggested Learning Resources:

Text Books:

1: Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0—47 1-64735-5.

2: John G Proakis and Masoud Salehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN 978-8—131-70573-5.

3: B.P.Lathi and Zhi Ding, "Modern Digital and Analog communication Systems", Oxford University Press, 4th Edition, 2010, ISBN: 978-0- 198-07380-2.

Reference Books

1: Ian A Glover and Peter M Grant, "Digital Communications", Pearson Education, Third Edition, 2010, ISBN 978-0-273-71830-7.

2: Bernard Sklar and Ray, "Digital Communications - Fundamentals and Applications", Pearson Education, Third Edition, 2014, ISBN: 978-81-317-2092-9.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity 1: Presentation on various topics

Activity 2: Small projects on applications of digital communication
Activity 3: Group discussion on various topics of digital communication

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	1			1	1	2		1		2	2	2	2
CO2	3	3	2	2		2	1	2		2		3	3	3	3
CO3	3	3	2	2		2	2	2		3		3	3	3	3
CO4	3	3	2	2		2	2	2		3		3	3	3	3
CO5	2	1	1	1		2	2	2		3		3	2	2	3

High-3, Medium-2, Low-1

V Semester

MICROPROCESSOR & MICROCONTROLLER			
Course Code:	21ECT502	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	52	**Total Marks:**	100
Credits:	04	**Exam Hours:**	03

Course objectives:

i. To illustrate the architecture of 8051 Micro controller.

ii. To understand the Special Function Registers, addressing modes and memory organization.

iii. To introduce Assembly language programming of 8051 Micro controller.

iv. To understand the RISC V microprocessors and Instruction Set Architecture.

Module-1	**08 hrs**

Introduction to microprocessors and microcontrollers: RISC & CISC CPU Architectures, Harvard & Von- Neumann CPU architecture.

8051 Microcontroller: The 8051 Architecture, Pin diagram of 8051, Memory organization, External Memory interfacing. Classification of Instruction, Addressing modes: Immediate addressing, Register addressing, Direct addressing, Indirect addressing, relative addressing, Absolute addressing, bit direct addressing. **(TEXT 1 and TEXT 2)**

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, l3

Module-2	**07 hrs**

8051 Instructions and Programming: 8051 instructions, Data transfer instructions,Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instructions. 8051 programming: Assembler directives, Assembly language programs and Time delay calculations. Stack operations.

Introduction to Embedded C: C data types, logical operations, programming 8051 using embedded C

(**TEXT 2 and TEXT 3**)

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3

Module-3	**09 hrs**

Timers/counters: 8051 timers/counters, delay program, counter programming 8051 timers to generate delay and counting operation using assembly and C language. Data communication, Basics of Serial Data Communication, 8051 Serial Communication, Programming in assembly and C.

Serial Communication: Data communication, Basics of Serial Data Communication, 8051 Serial Communication, Programming in assembly and C.

8051 interrupts and interfacing: Interrupts and Basics of interrupts, 8051 Interfacing and Applications: Basics of I/O concepts, I/O Port Operation, Interfacing 8051 to DAC,LED/LCD. **(TEXT 3)**

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3

Module-4	**08 hrs**

RISC-V Microprocessors: Introduction, Modular vs. Incremental ISAs, ISA Design 101 **RV32I: RISC-V Base Integer ISA:** Introduction, RV32I Instruction formats, RV32I Registers, RV32I Integer Computation, RV32I Loads and Stores, RV32I Conditional Branch, RV32I Unconditional Jump, RV32I Miscellaneous, Comparing RV32I, ARM-32, MIPS-32, and x86-32 using Insertion Sort. **RISC-V Assembly Language:** Introduction, Calling convention, Assembly, Linker, Static vs. Dynamic Linking, Loader.	
Teaching Learning Method:	Chalk and Talk, Power point presentations, Programming assignments
RBT Level:	L1, L2, L3

Module-5	**08 hrs**
RV32M: Multiply and Divide- Introduction **RV32F and RV32D: Single- and Double-Precision Floating Point**- Introduction, Floating-Point Registers, Floating-Point Loads, Stores, and Arithmetic, Floating-Point Converts and Moves, Miscellaneous Floating-Point Instructions, Comparing RV32FD, ARM-32, MIPS-32, and x86-32 using DAXPY. **RV32C: Compressed Instructions-** Introduction, **RV32A: Atomic Instructions-** Introduction, **RV32V: Vector**- Introduction	
Teaching Learning Method:	Chalk and Talk, Power point presentations, Programming assignments
RBT Level:	L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Conduct the following experiments by writing Assembly Language Program (ALP) using ARM Cortex M3 Registers using an evaluation board/simulator and the required software tool

Sl. No.	**Experiments**	**12 hrs**
1	**Data transfer programs-** **i]** WALP to transfer data between internal and external memories **ii]** WALP to exchange data between internal and external memories	
2	**Arithmetic operation programs-** **i]** WALP to add 10 bytes of data **ii]** WALP to add multi bytes of data **iii]** WALP to find the square and cube of an 8 bit binary number	

3	**Logical operation programs-**
	i] Let X, Y, Z refer to the contents of the memory location 30h,31h,and 32h respectively, write an ALP to perform the following logical operations;
	If X=00 perform the operation Y OR Z.
	If X=01 perform the operation Y AND Z.
	If X=02 perform the operation Y XOR Z.
	ii] WALP to compare the bytes of data present at the memory location 21h and 22h and represent the result of comparison through the bits whose addresses are 00h and 01h.
	If (21h)<(22h)then clear the bit at 01h and also set the bit at 00h.
	If (21h)>(22h)then set the bit at 01h and also clear the bit at 00h.
	If (21h)=(22h)then set the bit at 01h and also set the bit at 00h.
	iii] WALP to stimulate the Boolean expression **Eg:** Y=A+BC.	

4	i] **Parity Program-** WALP to count the number of 1's in a byte which is be accepted from the port 0 and displays the result on the port1. **ii] Palindrome Program-** WALP to check whether the gives byte is a valid bit palindrome,accep byte from the port0 and display aah if valid else 00H in port1.
5	**Timer program-** WALP to generate the output value AAH and 55H alternatively at the Port 0 for every 2 sec.
6	**Counter program-** WALP to count the number of inputs to the counter_0 by configuring the timer as a counter in mode_1 and display the count in ports.
7	**Design and implementation of RISC V Processor Subsystem using Verilog:** a) Floating Point Addition & Subtraction. b) Floating Point Multiplication. c) Operand Logic.
Demonstration Experiments (For CIE only not for SEE) Conduct the following experiments on an 8051 MC using evaluation version of Embedded 'C' & Keil µvision-3 tool/compiler.	
08	**Demonstrate the serial communication-**WALP to transfer the characters serially.
09	**Demonstrate the interfacing of DAC programs-**WALP to generate the wave forms i] Square wave ii] Triangle wave **iii]** Ramp wave (Both positive and negative)
10	**Demonstrate the interfacing of LED programs-** WALP to display the count (UP/DOWN/LED BLINKING)

Course outcomes:

At the end of the course the student will be able to:

CO1: understand the features and architecture of 8051 Microcontroller.

CO2: program 8051 microcontroller using assembly language and embedded C.

CO3: configure timers/counters of 8051 and understand serial communication and interrupts of 8051.

CO4: understand need of RISC V microprocessors and basics of RV32I.

CO5: understand basics of RV32M, RV32F, RV32D, RV32C, RV32A, RV32V.

Suggested Learning Resources:

Text Books:

1. **Yu-cheng Liu, Glenn A.Gibson,** "Microcomputer Systems: The 8086/8088 Family Architecture, Programming, and Design"

2. **Kenneth J. Ayala,** "The 8051 Microcontroller Architecture, Programming & Applications", 2e Penram International, 1996 / Thomson Learning 2005.

3. **Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay,** "The 8051 Microcontroller and Embedded Systems – using assembly and C", PHI, 2006 / Pearson, 2006.

4. **The RISC-V Reader: An Open Architecture** Atlas Beta Edition, 0.0.1, David Patterson and Andrew Waterman, October 4, 2017

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Programming Assignments / Mini Projects can be given to improve programming skills

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3					2	2	2				2	1	3	1
CO2	3	3	3			2		2	1			2	1	3	1
CO3	3	3	3		3	2		2	1			2	1	3	1
CO4	3	2	3		3	2		2	1			2	1	3	1
CO5	3	2	2		2	2		2	1				1	3	1

High-3, Medium-2, Low-1

V Semester

COMPUTER COMMUNICATION NETWORKS			
Course Code:	21ECT503	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:1	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	3	**Exam Hours:**	03

Course objectives:
This course will enable students to:
1. Provide Insight into the basics of networking, OSI reference and TCP/IP model.
2. Study of access links, protocols, error detection and correction techniques in the data link layer.
3. Understanding of routing algorithms, addressing techniques of the network layer.
4. Understand Protocol techniques of the transport layer.
5. Identify Services, Protocols, directory service and Security of the application layer

Module-1	**08 hrs**
Introduction: Data communication, Networks, Network types. **Network Models:** TCP/IP Protocol Suite, The OSI Model, Connecting devices. (1.1, 1.2, 1.3.1-1.3.4, 2.2, 2.3, 17.1.1-17.1.3 of Text)	
Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of OSI and TCP-IP protocol suites, Example of ARP and RARP.
RBT Level:	L1, L2, L3
Module-2	**08 hrs**
Data-Link Layer: Introduction, Link Layer addressing. **Error Detection and Correction:** Introduction, Cyclic Redundancy Check, Checksum. **Media Access Control:** Random Access, Controlled Access, Channelization, Virtual LAN. **Wired LANs**: Ethernet Protocol, Standard Ethernet. (9.1, 9.2.1, 9.2.2, 10.1, 10.3.1, 10.4.1, 10.4.2, 12.1, 12.2, 12.3, 13.1,13.2.1, 13.2.2,17.1, 17.2 of Text)	
Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animations showing Framing, CSMA, Connecting devices, Problems on ALOHA, CSMA, Framing and Standard Ethernet.
RBT Level:	L1, L2, L3
Module-3	**08 hrs**
Network Layer: Network Layer services, Packet Switching, IPV4 Addresses, IPv6 addressing and Protocol. **Network Layer Protocols:** Internet Protocol (IP). **Unicast Routing:** Routing Algorithms. (18.1, 18.2, 18.4, 19.1, 20.1, 20.2 ,22.1 ,22.2 of Text)	
Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation of DHCP, routing protocols, Numericals on Addressing,
RBT Level:	L1, L2, L3
Module-4	**08 hrs**
Transport Layer: Introduction, Transport Layer Protocols. **Transport-Layer Protocols in the Internet:** Port numbers, User Datagram Protocol, Transmission Control Protocol. 23.1, 23.2, 24.1.2 - 24.3.5 of Text)	
Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation/Implementation of Flow control protocols and TCP using

RBT Level:	simulators. L1, L2, L3
Module-5	**08 hrs**
Application Layer: Introduction, **Standard Client – Server Protocols**: World Wide Web and HTTP, Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS, Network Security. (25.1, 26.1.2, 26.2, 26.3, 26.6 ,31.1 of Text)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, PowerPoint Presentation, YouTube videos, Animation/Implementation of HTTP, FTP, DNS using network simulators. L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Define the network components, layers, addressing, topology, and connectivity and network types for data transmission.

CO2. Distinguish the basic network configurations and standards associated with each network.

CO3. Describe the layering architecture of computer networks and distinguish between the OSI reference model and TCP/IP protocol suite.

CO4. Identify the protocols and functions associated with the transport layer services.

CO5.Construct a network model and determine the routing of packets using different routing algorithms and identify the concepts of Network security.

Suggested Learning Resources:

Text Books:

1: Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

Reference Books

1: James J Kurose, Keith W Ross, "Computer Networks", Pearson Education.

2: Wayne Tomasi, "Introduction to Data Communication and Networking", Pearson India, 1st edition.

3: Andrew Tannenbaum, "Computer Networks", Prentice Hall.

4: William Stallings, "Data and Computer Communications", Prentice Hall

Web Links:

https://nptel.ac.in/courses/106105183.

TCP/IP Tutorial and Technical Overview, (IBM Redbook) - Download From http://www.redbooks.ibm.com/abstracts/gg243376.html

TCP/IP Guide, Charles M Kozierok, Available Online - http://www.tcpipguide.com/ Request for Comments (RFC) - IETF - http://www.ietf.org/rfc.html

https://cosmolearning.org/courses/computer-networks-524/video-lectures/

https://www.eecis.udel.edu/~bohacek/videoLectures/ComputerNetworking/ComputerNetworking_v2.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity 1: Implementation of simple networks and various networking protocols and algorithms using simulators like NCTUns / CISCO packet tracer and measurement of various parameters using WireShark

Activity 2: Implementation of simple networks and various networking protocols and algorithms in

C/C++/Python

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	-	**3**	**3**	**3**	-	-	-	-	**3**	**3**	-	-	-	-	-
CO2	-	**3**	**3**	**3**	**3**	-	-	-	**3**	**3**	-	-	**1**	-	-
CO3	-	**3**	**3**	**3**	**3**	-	-	-	**3**	**3**	-	**3**	-	**1**	-
CO4	-	**3**	**3**	**3**	**3**	-	-	-	**3**	**3**	-	**3**	**2**	-	-
CO5	-	**3**	**3**	**3**	**3**	-	-	-	**3**	**3**	-	**3**	**2**	**2**	-

High-3, Medium-2, Low-1

V Semester

MICROWAVE THEORY AND ANTENNA			
Course Code:	21ECT504	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03 Hrs

Course objectives:

1. Understanding the basics of microwave and waveguides.
2. Understanding the concepts of microwave networks, microwave passive devices and semiconductor devices.
3. Understanding microwave tubes, microwave design principles and antenna basics.
4. Understanding the importance of point sources, arrays and radiations from wires.
5. To understand different types of antennas like aperture, reflector, broadband and Microstrip antennas.

Module-1	**08 hrs**

Introduction to Microwaves -History of Microwaves, Microwave Frequency bands, applications of Microwaves, Losses associated with microwave transmission, Concept of Impedance in Microwave transmission.

Waveguides-Rectangular waveguide, Introduction to Circular waveguide (No derivations and Numerical examples), Strip line, Micro strip line. **TEXT 1,2**

Teaching Learning Method:	Chalk and Talk, YouTube videos
RBT Level:	L1, L2

Module-2	**08 hrs**

Microwave Network Analysis - Network parameters for microwave circuits, Scattering Parameters. Microwave Passive devices and semiconductor Devices - Microwave passive devices - Directional Coupler, Power Divider, Magic Tee, Attenuator. Microwave Semiconductor Devices - Gunn Diodes, IMPATT diodes, PIN diodes. **TEXT 1,2**

Teaching Learning Method:	Lecture-based learning and Group learning
RBT Level:	L1, L2

Module-3	**08 hrs**

Microwave Tubes: Klystron- two cavity klystron amplifier and reflex klystron (klystron oscillator) Antenna Basics - Physical concept of radiation, near and far field regions, basic antenna parameters: radiation patterns, beam area, radiation Intensity, beam efficiency, reciprocity, directivity and gain, antenna apertures, effective height, bandwidth ,radiation efficiency, radio communication Link and antenna field zones. **TEXT 1,2,3.4**

Teaching Learning Method:	Lecture-based learning and Group learning
RBT Level:	L1, L2

Module-4	**08 hrs**

Radiations from wires: Short electric dipole, resistance of dipole, Half wave dipole antenna, folded dipole antennas.

Point Sources & their arrays - Arrays, Point source, Power theorem and its application, Examples of power patterns, Field patterns, Phase patterns, Array of isotropic point sources different cases, non-isotropic sources, principle of pattern multiplication, linear arrays of n elements of equal amplitude & spacing, broad side, end fire arrays. **TEXT 3,4**

Teaching Learning Method:	Lecture-based learning and Group learning
RBT Level:	L1, L2, L3

Module-5	**08 hrs**

Aperture and Reflector Antennas- Huygens' principle, Babinet's principle, Radiation from sectoral and pyramidal horns: design concepts, prime-focus parabolic reflector and cassegrain antennas.
Broadband Antennas- Log-periodic and Yagi-Uda antennas, frequency independent antennas, broadcast antennas. Micro strip Antennas- Basic characteristics of micro strip antennas, feeding methods. **TEXT 3,4**

Teaching Learning Method:	Lecture-based learning and Group learning
RBT Level:	L1, L2, L4

Course outcomes:

At the end of the course the student will be able to:

CO1. Identify the microwave frequency band, its applications and different types of waveguides
CO2. Analyse microwave networks, microwave passive devices and semiconductor devices.
CO3. Apply microwave design principle, microwave tubes and antenna basics.
CO4. Be able to analyse the radiation patterns from different types of wires, point sources and their arrays.
CO5. Illustrate and design antennas like aperture, reflector, and broadband. Microstrip antenna.

Suggested Learning Resources:

Text Books:

1. Collin RE. Foundations for microwave engineering. John Wiley & Sons; 2007.
2. Annapurna Das, Sisir K Das, Microwave Engineering, TMH Publication, 2001
3. J.D. Kraus, Antennas and wave propagation, McGraw Hill, 4th ediation 2010.
4. C.A. Balanis, Antenna Theory - Analysis and Design, John Wiley, 1982.

Reference Books

1. Microwave Devices and circuits- Liao / Pearson Education. 1992
2. M.Kulkarni., "Microwave devices and Radar Engg."Umesh Publications, 2011
3. R.E. Collin, Antennas and Radio Wave Propagation, McGraw Hill, 1985.
4. I.J. Bahl and P. Bhartia, Micro Strip Antennas, Artech House, 1980.

Web Links:

1. www.nptel.in
2. https://www.academia.edu/12559664/Collin_Foundations_for_Microwave_Engineering
3. https://www.academia.edu/13759443/Basic_Antennas_Understanding_Practical_Antennas_and_Design_Joel_R_Hallas_2009
4. www.youtube/microwave , www.youtube/antennas

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1: Creating physical modules

2: Exploring new technologies and presenting

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	1												2	
CO2	3	3	2											2	
CO3	3	2	3	2			1					1	2	2	
CO4	3	3	2	2			1					1	2	2	

CO5	3	3	2	2			**1**					**1**	**2**	**2**	

High-3, Medium-2, Low-1

V Semester

COMMUNICATION LAB II			
Course Code	**21ECL505**	**CIE Marks**	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	**SEE Marks**	50
Credits	01	**Exam Hours**	03

Course objectives:

This laboratory course enables students to

- Design and demonstrate communication circuits for different digital modulation techniques.
- To simulate Source coding Algorithms using C/C++/ MATLAB code.
- To simulate Error correcting and detecting codes using C/C++/ MATLAB code.
- Simulate the networking concepts and protocols using C/C++/ Network simulation tool.
- Understand entropies and mutual information of different communication channels.

Sl.No.	**Experiments**
	Implement the following using discrete components
1	FSK generation and detection
2	PSK generation and detection
3	DPSK Transmitter and receiver
4	QPSK Transmitter and Receiver
	Implement the following in C/C++/MATLAB/Scilab/Python or any other Suitable software
5	Write a program to encode binary data using Huffman code and decode it.
6	Write a program to encode binary data using a (7,4) Hamming code and decode it.
7	Write a program to encode binary data using a ((3,1,2)/suitably designed) Convolution code and decode it.
8	For a given data, use CRC-CCITT polynomial to obtain the CRC code. Verify the program for the cases a) Without error b) With error
	Implement the following algorithms in C/C++/MATLAB/Network simulator
9	Write a program for congestion control using leaky bucket algorithm.
10	Write a program for distance vector algorithm to find suitable path for transmission.
11	Write a program for flow control using sliding window protocols.
12	Configure a simple network (Bus/star) topology using simulation software **OR** Configure a simple network (Ring/Mesh) topology using simulation software.
	Demonstration Experiments (For CIE)
13	Configure and simulate simple Wireless Local Area network.
14	Simulate the BER performance of (2, 1, 3) binary convolutional code with generator sequences g(1) =(1 0 1 1) and g(2) =(1 1 1 1) on AWGN channel. Use QPSK modulation scheme. Channel decoding is to be performed through Viterbi decoding. Plot the bit error rate versus SNR (dB), i.e. $P_{e,b}$ versus E_b/N_0. Consider binary input vector of size 3 lakh bits. Also find the coding gain.
15	Simulate the BER performance of (7, 4) Hamming code on AWGN channel. Use QPSK modulation scheme. Channel decoding is to be performed through maximum-likelihood decoding. Plot the bit error rate versus SNR (dB), i.e. $P_{e,b}$ versus E_b/N_0. Consider binary input vector of size 5 lakh bits. Use the following parity check matrix for the (7, 4) Hamming code. Also

	find the coding gain. $H = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 0 & 1 \end{bmatrix}$
16	Simulate the BER performance of rate 1/3 Turbo code. Turbo encoder uses two recursive systematic encoders with $G(D) = [1, \frac{1+D^4}{1+D+D^2+D^3+D^4}]$ and pseudo-random interleaver. Use QPSK modulation scheme. Channel decoding is to be performed through maximum a-posteriori (MAP) decoding algorithm. Plot the bit error rate versus SNR (dB), i.e. $P_{e,b}$ versus E_b/N_0. Consider binary input vector of size of around 3 lakh bits and the block length as 10384 bits. Also find the coding gain.

Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

1. Design and test the digital modulation circuits and display the waveforms.
2. To Implement the source coding algorithm using C/C++/ MATLAB code.
3. To Implement the Error Control coding algorithms using C/C++/ MATLAB code.
4. Illustrate the operations of networking concepts and protocols using C programming and network simulators.

Suggested Learning Resources:

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. K Sam Shanmugam, "Digital and analog communication systems", John Wiley India Pvt. Ltd, 1996.
3. Forouzan, "Data Communications and Networking", 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	2					1	1	1		1	3	3	
CO2	3	3	2					1	1	1		1	3	3	
CO3	3	3	2					1	1	1		1	3	3	
CO4	3	3	2					1	1	1		1	3	3	

` **High-3, Medium-2, Low-1**

V Semester

COMPUTER COMMUNICATION NETWORKS LAB			
Course Code:	21ECL5081	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	0:0:1:0(L - T –P)	**SEE Marks:**	50
Total Hours of Pedagogy:	12	**Total Marks:**	100
Credits:	1	**Exam Hours:**	03

Course objectives:

This course will enable students to:

1. Demonstrate the simulation of few protocols of data link layer and network layer.
2. Demonstrate the network communication between source and destination.
3. Demonstrate the detection and correction of error in data communication.
4. Simulate the configuration and verification of networking devices.

	Syllabus Contents
1	Write a C program to implement Bit Stuffing and DeStuffing. **RBT Level: L2, L3**
2	Write a C program to simulate a Character Stuffing and Destuffing for a given message. **RBT Level: L2, L3**
3	Write a C program to compute a Polynomial Checksum for a given binary data frame. **RBT Level: L2, L3**
4	Write a C program to simulate a Shortest Path Algorithm. **RBT Level: L2, L3**
5	Using TCP/IP Sockets, write a client-server program to make client to communicate with Server using socket programming techniques in python. **RBT Level: L2, L3**
6	Using TCP/IP Sockets, write to program to develop server and client file sharing system using Socket Programming in python. **RBT Level: L2, L3**
	Part B
7	**Configuring and Verifying LAYER 2 Switches**: For a given number of HOSTS, create a network by connecting Networking Devices, Configure and verify the same. Configuration includes HOSTNAME, BANNER, PASSWORD (CONSOLE, TELNET and ENABLE), MANAGEMENT IP and DEFAULT GATEWAY **RBT Level: L2, L3**
8	**Configuring and Verifying VLAN**: Create a network for a given number of HOSTS and Establish a communication between the hosts by connecting Switches, configure them and verify the same. Configuration includes Switch port configuration and encapsulation methods. **RBT Level: L2, L3**
9	**Configuring and Verifying IP Routing**: Using IP routing ,Establish a communication between the hosts by connecting the Network Devices, configure them and verify the same among different networks. Configuration includes: 1. Static Routing 2. Dynamic Routing (RIP/OSPF/EIGRP) **RBT Level: L2, L3**

10	**Configuring DHCP Server on a Router**: Configure DHCP server on a router to assign IP address dynamically to the hosts and verify the same. a. For One Broadcast Domain b. For Many Broadcast Domain **RBT Level: L2, L3**
11	**Configure a mail server**: Configure mail server using Packet tracer. **RBT Level: L2, L3**
12	Demonstration of Serial Communication using (i) RS232 (ii) MODEM COMMUNICATION (iii) FIBER OPTIC COMMUNICATION **RBT Level: L2**
	PART-C
13	[Simulation Case-Study] Dr. AIT is granted a block of addresses starting from 192.168.100.0/24. The Dr. AIT College committee decided to distribute these blocks of addresses to THREE Departments with each department receiving just FOUR Addresses. 1. Design the sub blocks and give the slash notation to each sub block
14	2. Simulate the above case using Cisco-packet Tracer. Note: while simulating Consider the following Constraints: a. Establish a communication within the Departments. b. Only HOD's of each Department can communicate (Single user from each Department) with each other.
15	Configure port security on the interface of the switch for the network topology.

Course outcomes:

At the end of the course the student will be able to:

CO1.Conduct an experiment to simulate various protocols of data link and network layer.

CO2.Configure and verify VLAN and switches.

CO3.Write the program to verify the detection and correction of error.

CO4.Demonstrate the data communication between two systems using the communication kit.

CO5.Write the program to transfer file and establish connection between two devices .

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	-	2	-	3	3	-	-	-	3	3	-	3	2	3	-
CO2	-	2	-	3	3	-	-	-	3	3	-	3	2	3	-
CO3	-	2	-	3	3	-	-	-	3	3	-	3	2	3	-
CO4	-	2	-	3	3	-	-	-	3	3	-	3	2	3	-
CO5	-	2	-	3	3	-	-	-	3	3	-	3	2	3	-

High-3, Medium-2, Low-1

V Semester

COMMUNICATION SIMULINK TOOLBOX			
Course Code:	21ECL5082	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	0:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	13	**Total Marks:**	100
Credits:	01	**Exam Hours:**	03

Course objectives:

- To impart knowledge of simulation software in digital communications
- To develop skills required to build and analyze the performance of various simulated communication systems under different conditions

Sl. No	Experiments
1	Modulation & demodulation of a random binary data stream using 16 – QAM.
2	Bit error rate (BER) improvement using Pulse Shaping on 16 – QAM signal. (Use forward error correction (FEC) coding.)
3	Perform OFDM modulation and obtain time domain and frequency domain plots to show a low rate signal, a high-rate signal, and a frequency selective multipath channel response.
4	(a) Simulate basic OFDM with no cyclic prefix. (b) Perform Equalization, Convolution, and Cyclic Prefix Addition on basic OFDM.
5	OFDM with FFT Based Oversampling - Modify an OFDM+ Cyclic Prefix signal to efficiently output an oversampled waveform from the OFDM modulator.
6	Simulate a basic communication system in which the signal is first QPSK modulated and then subjected to Orthogonal Frequency Division Multiplexing (OFDM).
7	Obtain the scatter plots & eye diagrams of a QPSK signal to visualize the signal behaviour in presence of AWGN.
8	(a) Generate a multiband signal using the Communications Toolbox. (b) Random noise generation using Simulink & display histogram plots of Gaussian, Rayleigh, Rician, and Uniform noise.
9	QPSK Transmitter and Receiver in Simulink.
10	Multipath Fading Channel in Simulink – For example: Simulate QPSK transmission over a • multipath Rayleigh fading channel and • a multipath Rician fading channel.
11	Adjacent and Co-Channel Interference using Simulink. • Use PSK-modulated signals to show the effects of adjacent and co-channel interference on a transmitted signal.
12	Modulation Classification with Deep Learning • Predict Modulation Type Using CNN

Course outcomes:

At the end of the course the student will be able to:

1. Perform sampling, aliasing, filtering, and quadrature modulation through simulation.
2. Plot signal space representation of digital modulation techniques.
3. Design and implement a pulse shape and matched filter to avoid inter-symbol interference and maximize receiver SNR.
4. Demonstrate advanced wireless communication techniques like Multipath fading, CCI etc. and model the same using MATLAB / Simulink

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1															
CO2															
CO3															
CO4															

High-3, Medium-2, Low-1

V Semester

ANTENNA DESIGN & TESTING			
Course Code:	21ECL5083	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	0:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	13	**Total Marks:**	100
Credits:	01	**Exam Hours:**	03

Course objectives:

1. To understand the various antenna parameters.
2. Conduct experiments to study the Radiation pattern of Antennas.
3. Design different types of antenna arrays and study the pattern characteristics (MATLAB)
4. Design of MMIC antennas like Patch Antenna and study the characteristics.

Sl. No	**Experiments**
1	To obtain the radiation pattern of a Yagi-Uda Antenna array and calculate its directivity
2	To obtain the radiation pattern of a Dipole Antenna array and calculate its directivity.
3	To calculate the aperture of a Dipole Antenna.
4	To obtain the near and far fields of a given antenna and compare the fields.
5	To obtain the Radiation pattern of a microstrip antenna.
6	To obtain the resonant frequency of a Yagi-Uda /Dipole antenna.
7	To obtain the bandwidth of a given Antenna.
8	Plot 2-D and 3-D radiation pattern of omnidirectional antenna using MATLAB.
9	Design and implementation of a broadside array using MATLAB.
10	Design and implementation of an endfire array using MATLAB.
	Demonstration Experiments (For CIE)
11	Design of a Patch Antenna using HFSS Software.
12	Design of a dipole Antenna using HFSS Software.

Course outcomes:
At the end of the course the student will be able to:

1. Analyze the radiation pattern and characteristics of antenna
2. Ability to design various antenna
3. Ability to use different software tools to study antenna characteristics
4. Analyze radiation pattern of linear array antennas

Suggested Learning Resources:

1. Antennas and Wave Propagation -John D Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition,
2. McGraw Hill Education, 2013.
3. https://www.mathworks.com/help/antenna/
4. Help and demo files of the HFSS and MATLAB software

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	2											2	2	
CO2	3	3	3										3	3	
CO3	2	2	2	2	3								2	2	
CO4	2	2	2	2									2	2	

High-3, Medium-2, Low-1

V Semester

MICROWAVES TOOLBOX			
Course Code:	21ECL5084	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	0:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	13	**Total Marks:**	100
Credits:	01	**Exam Hours:**	03

Course objectives:

- Identification of microwave components/devices.
- Study basic principles of operation of microwave devices/ components

Sl. No	Experiments
1	V- I Characteristics of Gunn-diode.
2	Study of characteristics of Magic Tee
3	Coupling and Isolation characteristics of microstrip directional coupler.
4	Determination of power division of microstrip power divider.
5	Determination of resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
6	Measurement of frequency, guide wavelength, power and attenuation in a microwave Test bench.
7	Study of characteristics of E plane Tee / H plane Tee.
8	To measure unknown impedance using Smith chart through test bench setup.
9	Measurement of VSWR and reflection coefficient and attenuation in a microwave test bench Setup.
10	Study propagation of wave using rectangular waveguide using MATLAB.
11	Study of impedance matching using MATLAB.
12	To calculate phase and group velocity using MATLAB.

Course outcomes:

At the end of the course the student will be able to:

1. Demonstrate the characteristics of microwave sources.
2. Demonstrate the characteristics of directional coupler
3. Study of microwave measurement procedure.
4. Apply MATLAB toolbox for study of microwaves phenomena.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	**3**	**3**	**2**									**2**	**2**	**2**	
CO2	**3**	**3**	**3**	**3**		**2**						**1**	**2**	**2**	
CO3	**2**	**2**	**2**	**2**	**3**								**2**	**2**	
CO4	**2**	**2**	**2**	**2**									**2**	**2**	

High-3, Medium-2, Low-1

VI Semester

TECHNOLOGICAL INNOVATION MANAGEMENT AND ENTREPRENEURSHIP			
Course Code:	21ECT601	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	52	**Total Marks:**	100
Credits:	04	**Exam Hours:**	03

Course objectives:

1. Understand basic skills of Management.
2. Understand the need for Entrepreneurs and their skills.
3. Identify the Management functions and Social responsibilities.
4. Understand the Ideation Process, creation of Business Model.

Module-1	**08 hrs**

Management: Nature and Functions of Management- Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession
(Selected topics of Chapter 1, Text 1).
Planning: Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making-Meaning, Types and Steps in Decision Making
(Selected topics from Chapters 4 & S, Text 1). L1,L2

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2

Module-2	**07 hrs**

Organizing and Staffing: Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalisation, Committees-Meaning, Types of Committees; Centralization Vs Decentralization of Authority and Responsibility; Staff"mg-Need and Importance, Recruitment and Selection Process
(Selected topics from Chapters 7, 8 & 11, Text 1).
Directing and Controlling: Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication - Meaning, Importance and Purposes of Communication; Leadership-Meaning, Characteristics, Behavioural Approach of Leadership.
(Selected topics from Chapters 15to 18and 9, Text 1).

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2

Module-3	**08 hrs**

Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance
(Selected topics from Chapter 3, Text 1).
Entrepreneurship: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship
(Selected topics from Chapter 2, Text 2).

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2

Module-4	**08 hrs**

Family Business: Role and Importance of Family Business, Contributions of Family Business in India, Stages of Development of a Family Business, Characteristics of a Family-owned Business in India, Various types of family businesses
(Selected topics from Chapter 4, (Page 71-75) Text 2).
Idea Generation and Feasibility Analysis- Idea Generation; Creativity and Innovation; Identification of Business Opportunities; Market Entry Strategies; Marketing Feasibility.
(Selected topics from Chapter 6(Page No. 111-117) & Chapter 7(Page No. 140-142), Text 2)

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	L1, L2

Module-5	**08 hrs**

Business model- Meaning, designing, analyzing and improvising; Business Plan - Meaning, Scope and Need; Financial, Marketing, Human Resource and Production/Service Plan; Business plan Formats; Project report preparation and presentation; Why some Business Plan fails?
(Selected topics from Chapter 8 (Page No 159-164, Text 2)

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2

Course outcomes:

At the end of the course the student will be able to:

CO 1. Understand the fundamental concepts of Management and Entrepre- neurship and opportunities in order to setup a business

CO 2. Identify the various organizations' architecture

CO 3. Describe the functions of Managers, Entrepreneurs and their social responsibilities

CO 4. Understand the components in developing a business plan

CO 5. Recognize the various sources of funding and institutions supporting entrepreneurs.

Suggested Learning Resources:

Text Books:

1. Principles of Management - P.C Tripathi, P.N Reddy, McGraw Hill Education, fYhEdition, 2017. ISBN-13:978-93-5260-5354.

2. Entrepreneurship Development Small Business Enterprises- Poomima MCharantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.

3. Dynamics ofEntrepreneurial Development and Management byVasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.

4. Robert D. Hisrich, Mathew J. Manimala, Michael PPeters and DeanA. Shepherd, "Entrepreneurship", S1h Edition, Tata Mc-Graw HillPublishing Co.Ltd.- New Delhi, 2012

Reference Books:

1. Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, I01h Edition 2016. ISBN- 978-93-392-2286-4.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3

High-3, Medium-2, Low-1

VI Semester

COMPUTER ORGANIZATION & ARM MICROCONTROLLERS			
Course Code:	21ECT602	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	52	**Total Marks:**	100
Credits:	04	**Exam Hours:**	03

Course objectives:

1. to explain the basic organization of a computer system.
2. to understand functioning of different sub systems, such as processor, Input/output, and memory.
3. to describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.
4. to Program ARM Cortex M3 for different applications.
5. to analyse the Thumb instruction set and different C-Programming concepts.

Module-1	**08 hrs**
Basic Structure of Computers: Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. **Input/Output Organization:** Accessing I/O Devices, Interrupts – Interrupt Hardware, Direct Memory Access, Buses, Interface Circuits, Standard I/O Interfaces – PCI Bus, SCSI Bus, USB. **Text 1**	
Teaching Learning Method: Chalk and Talk, PowerPoint Presentation, YouTube videos **RBT Level:** L1, L2	
Module-2	**08 hrs**
Memory System: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Replacement Algorithms, Performance Considerations. **Basic Processing Unit**: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hard-wired Control, Micro programmed Control. Basic concepts of pipelining, **Text 1**	
Teaching Learning Method: Chalk and Talk, PowerPoint Presentation, YouTube videos **RBT Level:** L1, L2	
Module-3	**08 hrs**
ARM Embedded Systems: Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions. **Text 2**	
Teaching Learning Method: Chalk and Talk, PowerPoint Presentation, YouTube videos **RBT Level:** L1, L2	
Module-4	**08 hrs**
Introduction to the ARM Instruction set: Introduction, Data processing instructions, Load – Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional Execution. **Text 2**	
Teaching Learning Method: Chalk and Talk, Power point presentations, Programming assignments **RBT Level:** L1, L2, L3	
Module-5	**08 hrs**

Introduction to the THUMB instruction set: Introduction, THUMB register usage, ARM – THUMB interworking, Other branch instructions, Data processing instructions, Stack instructions, Software interrupt instructions.

Efficient C Programming: Overview of C Compilers and optimization, Basic C Data types, C looping structures. **Text 2**

Teaching Learning Method:	Chalk and Talk, Power point presentations, Programming assignments
RBT Level:	**RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC

Conduct the following experiments by writing Assembly Language Program (ALP) using ARM Cortex M3 Registers using an evaluation board/simulator and the required software tool

Sl. No.	Experiments	12 hrs
1.	Write an ALP to find the sum of first 10 integer numbers.	
2.	Write an ALP to calculate the value of the polynomial function.	
3.	Write an ALP to store data in desired Memory location.	
4.	Write a C program to Output the message using UART of LPC1768.	
5.	Write a C Program to interface LED using LPC 1768.	
6.	Write a C Program to interface Relay using LPC 1768.	
7.	Write a C Program for DC motor/Stepper motor rotation using LPC 1768.	
8.	Write a C Program to interface a DAC and generate Triangular and Square waveforms.	
9.	Write a C program to demonstrate the use of an External interrupt in LPC 1768	

Demonstration Experiments (For CIE only not for SEE)

Conduct the following experiments on an ARM CORTEX M3 evaluation board using evaluation version of Embedded 'C' & Keil µvision-4 tool/compiler.

10.	Write a C program to interface a Real Time Clock (RTC) of LPC 1768.
11.	Write a program to read on-chip ADC value and display it on UART terminal using LPC 1768
12.	Write a C program to interface Keypad using LPC 1768.

Course outcomes:

At the end of the course the student will be able to:

CO 1: Understand the basic structure and Input output organization of a computer system.

CO 2: Explain functioning of different sub systems, such as processor, Input/output, and memory.

CO 3: Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.

CO 4: Apply the instruction set to Program ARM Cortex M3 for different applications.

CO5: Analyse Thumb Instruction set and C-Programming Concepts to Program ARM Cortex M3.

Suggested Learning Resources:

Text Books:

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5th Edition, Tata McGraw Hill, 2002. (Listed topics only from Chapters 1, 2, 4, 5, 8).

2. Andrew N Sloss, Dominic System and Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publisher, 1st Edition, 2008

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Programming Assignments / Mini Projects can be given to improve programming skills

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2												3	
CO2	3	2												3	
CO3	3	2												3	
CO4	3	2	2		2		1		1					3	
CO5	3	2	2		2		1		1					3	

High-3, Medium-2, Low-1

VI Semester

VLSI DESIGN AND TESTING			
Course Code:	21ECT603	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	3

Course objectives:

1. Impart knowledge of MOS transistor theory and CMOS technology
2. Learn the operation principles and analysis of inverter circuits.
3. Infer the operation of Semiconductor memory circuits.
4. Demonstrate the concept of CMOS testing.

Module-1	**8 Hrs**
Introduction: A Brief History, MOS Transistors, CMOS Logic (1.1 to 1.4 of TEXT1) **MOS Transistor Theory:** Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (2.1, 2.2, 2.4 and 2.5 of TEXT1).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on transistor working Self-study topics: MOSFET Scaling and Small-Geometry Effects RBT Level: L1, L2, L3
Module-2	**08 Hrs**
Fabrication: CMOS Fabrication and Layout, Introduction, CMOS Technologies, Layout Design Rules, (1.5 and 3.1 to 3.3 of TEXT1). **Delay:** Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths (4.1 to 4.5 of TEXT1, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation, YouTube videos, Videos on fabrication Self-study topics: Layouts of complex design using Euler's method RBT Level: L1, L2, L3
Module-3	**08 Hrs**
Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM) (10.1 to 10.6 of TEXT2)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, PowerPoint Presentation, YouTube videos on Standard cell memory Design Self-study topics: Memory array design RBT Level: L1, L2, L3
Module-4	**08 Hrs**
Faults in digital circuits: Failures and faults, Modelling of faults, **Temporary faults Test generation for combinational logic circuits**: Fault diagnosis of digital circuits, test generation techniques for combinational circuits, Detection of multiple faults in combinational logic circuits. (1.1 to 1.3, 2.1 to 2.3 of TEXT3)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, PowerPoint Presentation, YouTube videos, videos on testing algorithms for test generation Self-study topics: Testable combinational logic circuits RBT Level: L1, L2, L3

Module-5	07 Hrs

Test generation for sequential circuits: Testing of sequential circuits as iterative combinational circuits, state table verification, test generation based on circuits structure, functional fault models, test generation based on functional fault models.

Design of testable sequential circuits: Controllability and Observability, Adhoc design rules, design of diagnosable sequential circuits, The scan path technique, LSSD, Random Access scan technique, partial scan. (4.1 to 4.5, 5.1 to 5.7 of TEXT3)

Teaching Learning Method:	Chalk and talk method/Power point presentation, YouTube videos
RBT Level:	Self-study topics: Memory testing techniques RBT Level: L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.

CO2. Draw the basic gates using the stick and layout diagram with the knowledge of physical design aspects.

CO3. Interpret memory elements along with timing considerations.

CO4. Interpret testing and testability issues in combinational logic design.

CO5. Interpret testing and testability issues in Sequential logic design.

Suggested Learning Resources:

Text Books:

1: "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education. 2015

2: "CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill, 2019.

3: "Digital Circuit Testing and Testability", Lala Parag K, New York, Academic Press, 1997

Reference Books:

1: "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

2: "Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits", Vishwani D Agarwal, Springer, 2002.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1: Model displayed for clear understanding of fabrication process of MOS transistor

2: Practise session can be held to understand the significance of various layers in MOS process, with the help of coloured layouts

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	3		2								1	1	1
CO2	3	3	2										1	1	1
CO3	3	2	1										1	1	1
CO4	3	3	2										1	1	1
CO5	3	2	3										1	1	1

High-3, Medium-2, Low-1

VI Semester

ARTIFICIAL NEURAL NETWORK			
Course Code:	21ECT6041	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	3

Course objectives:

1. To provide a strong foundation of fundamental concepts and structures in Neural Networks.
2. To understand the Analysis of different techniques and algorithms in Neural Networks.
3. To study the concepts of setting parameters and multilayered Networks.
4. To understand the concepts of Prediction, Polynomial Neural Networks.
5. To analyze the Optimization techniques in Neural Networks
6. To enable the student to apply these techniques in applications which involve neural models.

Module-1	**08 hrs**
Introduction, Fundamental concepts and models of Artificial Neural Network, Biological Neural Networks, structure and function of single neuron, neural network architectures, modelling of neural network, Neural learning process.	
Teaching Learning Method: **RBT Level:**	L1, L2

Module-2	**09 hrs**
Supervised Learning for single layer network: Perceptron, linear separability, Perceptron Training Algorithm, Delta rule. Supervised Learning for Multi- layer network: multilevel discrimination, preliminaries, Back propagation, setting parameter values.	
Teaching Learning Method: **RBT Level:**	L1, L2

Module-3	**08 hrs**
Prediction networks: Introduction, Recurrent network, Radial Basis Functions, Polynomial networks: Higher order network, Sigma–pi network, Function link architecture, Pi-sigma network	
Teaching Learning Method: **RBT Level:**	L1, L2

Module-4	**08 hrs**
Unsupervised learning: Winner take all networks. Hamming networks, Maxnet, Simple competitive learning, Hebb rule, Optimization Methods: Hop filed networks, Travelling Sales person problem, Iterated Gradient Descent	
Teaching Learning Method: **RBT Level:**	L1, L2

Module-5	**06 hrs**
Introduction to Neural Network Algorithms- Support Vector Machine, Generative Adversarial Network, Convolutional Neural Network, Machine learning, Deep learning **Case studies on neural network modelling:** Facial Recognition, Stock Market Prediction Weather Forecasting, Voice Recognition	

Teaching Learning Method:	
RBT Level:	L2, L3, L4

Course outcomes:

At the end of the course the student will be able to:

CO1. Understand the basic concepts of Neural Networks.

CO2. Analysis and development of different techniques in neural networks.

CO3. Analysis the concepts of Prediction Networks.

CO4. Understand and analysis of the concepts of Polynomial networks in Artificial

CO5. Use different optimization, machine learning technique for different model and enveloping the application.

Suggested Learning Resources:

Text Books:

1. Kishan Mehrotra, C. K. Mohan, Sanjay Ranka,Penram, "Elements of Artificial Neural Networks", 2007.
2. J. Zurada, Jaico, "Introduction to Artificial Neural Systems", *2003.*
3. Neural Networks A Classroom Approach- Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition 2019
4. Mohamad H Hassoun " Fundamentals of Artificial Neural Networks, PHI 2019 edition

Reference Books

1. Simon Hayking, "Neural Networks: A Comprehensive Foundation",2nd Edition, PHI.
2. Laurene Fausett, "Fundamentals of Neural Networks: Architecture, Algorithms and Applications", Person Education, 2004.

Web Links: nptl.iitm.ac.in

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity 1: Project on Voice recognition system

Activity 2: Stock Market Prediction

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	2	2	1	-	-	2	-	-	-	3	3	3	2
CO2	3	3	2	2	1	-	-	2	-	-	-	3	3	3	2
CO3	3	2	2	2	1	-	-	2	-	-	-	3	3	3	2
CO4	3	3	2	2	2	-	-	2	-	-	-	3	3	3	2
CO5	3	1	1	2	1	-	-	2	-	-	-	3	3	3	2

High-3, Medium-2, Low-1

VI Semester

CRYPTOGRAPHY			
Course Code:	21ECT6042	**CIE Marks:**	40+5+5
Teaching Hours/Week (L:T:P:S):	3: 0: 0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	3	**Exam Hours:**	03

Course objectives:

This course will enable students to:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Information Security with knowledge of mathematical concepts required for cryptography.
- Core Competence: To equip students with a basic foundation of Cryptography by delivering the basics of symmetric key and public key cryptography and design of pseudo random sequence generation technique

Module-1	**08 hrs**
Basic Concepts of Number Theory and Finite Fields: Divisibility and The Division Algorithm Euclidean algorithm, Modular arithmetic, Groups, Rings and Fields, Finite fields of the form GF(p), Polynomial Arithmetic, Finite Fields of the Form GF(2m) (Text 1: Chapter 3)	
Teaching Learning Method:	Chalk and Talk, YouTube videos, Flipped Class Technique Programming on implementation of Euclidean algorithm, multiplicative inverse, Finite fields of the form GF(p), construction of finite field over GF(2m).
RBT Level:	L1, L2, L3
Module-2	**08 hrs**
Introduction: Computer Security Concepts, A Model for Network Security (Text 1: Chapter 1) **Classical Encryption Techniques**: Symmetric cipher model, Substitution techniques, Transposition techniques (Text 1: Chapter 1)	
Teaching Learning Method:	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Programming on Substitution and Transposition techniques. Self-study topics: Security Mechanisms, Services and Attacks.
RBT Level:	L1, L2, L3
Module-3	**08 hrs**
Block Ciphers: Traditional Block Cipher structure, Data encryption standard (DES) (Text 1: Chapter 2: Section1, 2) The AES Cipher. (Text 1: Chapter 4: Section 2, 3, 4) **More on Number Theory**: Prime Numbers, Fermat's and Euler's theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 5)	
Teaching Learning Method:	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of SDES using programming languages like C++/Python/Java/Scilab. Self-study topics: DES S-Box- Linear and differential attacks
RBT Level:	L1, L2, L3
Module-4	**08 hrs**

ASYMMETRIC CIPHERS: Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 1, 3, 4)	
Teaching Learning Method:	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of Asymmetric key algorithms using programming languages like C++/Python/Java/Scilab. Numerical examples on Elliptic Curve Cryptography
RBT Level:	L1, L2, L

Module-5	**08 hrs**

Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16)	
Teaching Learning Method:	Chalk and Talk, YouTube videos, Flipped Class Technique and PPTs. Implementation of simple stream ciphers using programming languages like C++/Python/Java/Scilab.
RBT Level:	L1, L2, L3

Course outcomes:

At the end of the course, the student will be able to:

At the end of the course the student will be able to:

1. Explain traditional cryptographic algorithms of encryption and decryption process.
2. Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the data.
3. Apply concepts of modern algebra in cryptography algorithms.
4. Design pseudo random sequence generation algorithms for stream cipher systems.

Suggested Learning Resources:

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.

Reference Books:

1. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003

Weblink:

https://nptel.ac.in/courses/106105031

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1															
CO2															
CO3															
CO4															
CO5															

High-3, Medium-2, Low-1

VI Semester

PYTHON PROGRAMMING			
Course Code:	21ECT6043	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	3	**Exam Hours:**	03

Course objectives:

1. To acquire the fundamentals of Python programming language.
2. To attain an understanding of functions and collection types.
3. To familiarize the concepts of sequence types, data structures, and error handling in Python.
4. To realize the concepts of object-oriented in Python.
5. To get familiarised with the concepts of file handling and regular expressions.

Module-1	**08 hrs**

Introduction: Introducing Python, Setting Up Python in Windows, introducing IDLE.

Parts of Python programming: Identifiers, Variables, Keywords, statements and expressions, variables, operators, datatypes-Built-in datatypes, sequences in Python, indentation, comments, Input and Output statements.

Control Flow - if, if-elif-else, while loop, for loop, infinite loop, break, continue, return, and pass statements.

Teaching Learning Method:	Chalk and Talk, Power Point Presentation
RBT Level:	L1, L2, L3

Module-2	**08 hrs**

Functions - Defining Functions, Calling Functions, positional Arguments, Keyword Arguments, Default Arguments, Variable-length arguments, Recursive Functions, Anonymous Functions, and Function Decorators.

Strings and Lists: Creation, Basic operations, built-in methods, del statement.

Teaching Learning Method:	Chalk and Talk, Power Point Presentation
RBT Level:	L1, L2, L3

Module-3	**08 hrs**

Tuples, and Dictionaries: Creating Tuples, Accessing the Tuple Elements, Basic Operations on Tuples, Operations on Dictionaries, Dictionary methods, using foe loop with dictionaries, converting lists into dictionaries, Converting Strings into Dictionary,

Data Structures in Python: Linked Lists, Stacks, Queues, Deques. Programming Examples.

Exceptions: Errors in a Python Program, Exception Handling, The Except Block, User Defined Exceptions.

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-4	**08 hrs**

Object Oriented Programming in Python: Features of Object -Oriented Programming System (OOPS), Creating a class, The Self Variable, constructor, Types of variables, Namespaces, Types of Methods, passing members of one class to another class, Inner classes.

Inheritance and Polymorphism: Constructors in Inheritance, overriding Super class constructors and methods, The super() method, Types of Inheritance: Single/Multiple, Method Resolution order, Polymorphism, Operator Overloading, Method overloading, Method Overriding. Programming Examples	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-5	**08 hrs**
Files in Python: Types of files, Opening and closing file, Working with Text files, Working with Binary Files, with statements, Pickle in Python, The seek() and tell() methods, Random accessing Binary files, zipping, and unzipping Files, reading and writing to CSV files. **Regular Expressions**: Regular Expression, Sequence Characters in Regular Expression, Quantifiers in Regular Expression, Special Characters in Regular Expression, Using Regular Expression on Files, Retrieving Information from a HTML File.	
Teaching Learning Method:	Chalk and Talk, Power Point Presentation
RBT Level:	L1, L2, L3

Course outcomes:

At the end of the course, the student will be able to:

CO1. Apply the knowledge of Python scripting elements, Python constructs, datatypes, to solve engineering problems.

CO2. Identify the problem to apply the concepts of control structures, functions and error handling to solve them using the Python programming language

CO3. Apply the knowledge of Python and use the language scripting elements to manage the data, build the data structures, and handle errors.

CO4. Designing the solution to real-world problems through object-oriented concepts such as Inheritance, Polymorphism, and operator overloading.

CO5. Demonstrating the concepts of file handling and regular expressions

Suggested Learning Resources:

Text Books:

1: Core Python Programming: Dr. R. Nageshwara Rao, Dream Tech Press,2018

2: Introduction to Python Programming, Gowrishankar S, Veena A, CRC Press,2019

Reference Books:

1: Think Python, Allen Downey, Green Tea Press.

2: Core Python Programming, W.Chun, Pearson.

3: Introduction to Python, Kenneth A. Lambert, Cengage

4: Learning Python, Mark Lutz, Orielly

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity 1: Group activity for a group of 4 or 5 students -5 marks

Activity 2: Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	1	1	1				1					2		
CO2	2	2	3	1	2			1					2		
CO3	2	3	3	2	2			1					2		
CO4	2	3	3	1	2			1					2		
CO5	1	3	2	1	2			1					2		

High-3, Medium-2, Low-1

VI Semester

MICRO ELECTRO MECHANICAL SYSTEMS			
Course Code:	21ECT6044	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3: 0: 0:1	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

1. **Preparation**: To prepare students with fundamental knowledge/ overview in the field of Micro Electro Mechanical Systems.
2. **Core Competence**: To equip students with a basic foundation in electronic engineering, mechanical engineering, electrical engineering, chemistry, physics and mathematics fundamentals required for comprehending the operation and application of MEMS circuits, design.
3. **Professionalism & Learning Environment:** To inculcate in students an ethical and professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context, and life-long learning needed for a successful professional career.

Module 1	**08 hrs**

Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization, Applications and Markets.

Text1:**1.1,1.2,1.3,1.4,1.5,1.6,1.7,1.8,1.9**

Teaching Learning Method:	Chalk and talk method, Animation of MEMS products and applications.
RBT Level:	L1, L2, L3

Module 2	**08 hrs**

Working Principles of Microsystems: Introduction, Microsensors, Micro actuation, MEMS with Micro actuators, Micro accelerometers, Microfluidics.Text**1: 2.1,2.2,2.3,2.4,2.5,2.6**

Engineering Science for Microsystems Design and Fabrication: Introduction, Atomic Structure of Matter, Ions and Ionization Molecular Theory of Matter and Intermolecular Forces, Plasma Physics, Electrochemistry.**Text1: 3.1,3.2,3.3, 3.4, 3.7,3.8**

Teaching Learning Method:	Power Point Presentation, You Tube videos, Animations of MEMS Microsensors, Micro actuators, Micro accelerometers and Microfluidics, molecules, Ions and matter
RBT Level:	L1, L2, L3

Module 3	**08 hrs**

Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.**Text1:4.1,4.2,4.3,4.4,4.5,4.6,4.7**

Teaching Learning Method:	Chalk and talk method, Power Point Presentations and supporting You Tube Videos Solve numerical related to Thin Plates, and Vibration. Self-study topics: solve numerical related to the topics
RBT Level:	L1,L2, L3

Module 4	**08 hrs**

Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling in Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer. **Text1:6.1,6.2,6.3,6.4,6.5,6.6,6.7,6.8**	
Teaching Learning Method:	Chalk and Talk Method, You Tube Videos, Solve numerical related to scaling in Geometry Self-study topics: solve numerical of the topics
RBT Level:	L1, L2, L3

Module 5	**08 hrs**
Overview of Micromanufacturing: Introduction, Bulk Micro manufacturing, Surface Micro machining, The LIGA Process, Summary on Micro manufacturing. **Text1:9.1,9.2,9.3,9.4,9.5** **Microsystem Packaging**: Introduction, Overview of Mechanical Packaging of Microelectronics, Microsystem Packaging. **Text1:11.1,11.2,11.3**	
Teaching Learning Method:	Power Point Presentation, YouTube videos, Animation of MEMS micro manufacturing Supporting animation videos on packaging.
RBT Level:	L1, L2, L3

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Appreciate the technologies related to Micro Electro- Mechanical Systems.
2. Understand design and fabrication processes involved with MEMS devices.
3. Analyze the MEMS devices and develop suitable mathematical models
4. Understand design of scaling factors in MEMS devices.
5. Know various application areas, mechanical packaging for MEMS devices.

Suggested Learning Resources:

Text Book:

1. Tai-Ran Hsu, MEMS and Microsystems: DesignandManufacture,1st Ed, Tata Mc Graw Hill.

Reference Books:

1. Hans H Gatzen, Volker Saile, JurgLeuthold, Microand Nano Fabrication: Tool sand Processes, Springer, 2015.
2. DilipKumar Bhattacharya, Brajesh Kumar Kaushik, Microelectromechanical Systems (MEMS), Cengage Learning.
3. Chang Liu, Foundations of MEMS, Pearson Ed.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1: Develop mini projects and Final year projects using MEMS components to address the real-world problems

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2											2	3	
CO2	3	3	3		2								3	3	
CO3	3	3	3	2									1	3	
CO4		3	3				2						1	3	
CO5													1	2	

High-3, Medium-2, Low-1

VI Semester

COMMUNICATION ENGINEERING			
Course Code:	**21ECT6051**	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	**3:0:0:0**	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

1. Describe essential elements of an electronic communication system.
2. Understand Amplitude, Frequency & Phase modulations, and Amplitude demodulation.
3. Define the sampling theorem and methods to generate pulse modulations.
4. Learn the various methods of digital modulation techniques and compare the different schemes.
5. Introduce the basic concepts of information theory and coding
6. Understand the basic concepts of wireless and cellular communications.

Module-1	**08 Hrs**
Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, Signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation (Text 1: 1.1 to 1.10)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power Point Presentation Self-study topics: Classification of Signals and systems RBT Level: L1, L2, L3

Module-2	**08 Hrs**
Amplitude Modulation Techniques: Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM, (TEXT 1: 4.1, 4.2, 4.4, 4.6) **Angle Modulation Techniques**: Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation (TEXT1: 5.1, 5.2, 5.5)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method/Power point presentation Self-study topics: DSBSC, SSB and VSB modulation techniques and comparison. RBT Level: L1, L2, L3

Module-3	**08 Hrs**
Sampling Theorem and Pulse Modulation Techniques: Digital Versus Analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals (TEXT 1: 7.2 to 7.8)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method Self-study topics: Differential PCM and Delta Modulation RBT Level: L1, L2, L3

Module-4	**08 Hrs**
Digital Modulation Techniques: Types of digital Modulation, ASK, FSK, PSK, QPSK. (TEXT 1: 9.1 to 9.5) **Information Theory, Source and Channel Coding:** Information, Entropy and its properties, Shannon,-Hartley Theorem, Objectives of source coding, Source coding technique, Shannon source coding theorem, Channel coding theorem, Error Control and Coding. [Text1: 10.1,10.2, 10.11.2, 11.1 to 11.3, 11.8, 11.9, 11.12]	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power Point Presentation.

	Self-study topics: Quadrature Amplitude Modulation, Comparison of Digital Modulation techniques. RBT Level: L1, L2, L3

Module-5	**07 Hrs**

Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next generation networks, Applications of wireless communication (TEXT 2: 1.1 to 1.7)

Principles of Cellular Communications: Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequency reuse distance (TEXT 2: 4.1 to 4.7)

Teaching Learning Method:	Chalk and talk method/Power point presentation
RBT Level:	Self-study topics: Basic propagation mechanisms, Multipath fading. RBT Level: L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Describe the scheme and concepts of radiation and propagation of communication signals through air.

CO2. Understand the AM and FM modulation techniques and represent the signal in time and frequency domain relations.

CO3. Understand the process of sampling and quantization of signals and describe different methods to generate digital signals.

CO4. Describe the basic digital modulation techniques, channel capacity, source coding technique and the channel coding.

CO5. Compare the different wireless communication systems and describe the structure of cellular Communication.

Suggested Learning Resources:

Text Books:

1: T L Singal, Analog and Digital Communications, McGraw Hill Education (India) Private Limited, 2012, 0-07-107269-1

2: T L Singal, Wireless Communications, McGraw Hill Education (India) Private Limited, 2016, ISBN:0-07-068178-3.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Wherever necessary MatLab/Labview tools must be used.

1.Write Matlab Code for the following circuits, observe the waveform

i. AM, FM, QPSK, BPSK, TDM, PWM etc Generation and Demodulation.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	3		2			1	1	1			1	1	1
CO2	3	3	3		3			1	1				1	1	1
CO3	3	3	3		1			1	1				1	1	1
CO4	3	3	3		1			1	1				1	1	1
CO5	3	3	3										1	1	1

High-3, Medium-2, Low-1

VI Semester

MICROCONTROLLERS			
Course Code:	21ECT6052	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

This course will enable students to:

• Understand the difference between a microprocessor and a microcontroller and embedded microcontrollers.
• Familiarize the basic architecture of 8051 micro controller.
• Program 8051microprocessor using Assembly Level Language and C.
• Understand the interrupt system of 8051 and the use of interrupts.
• Understand the operation and use of inbuilt Timers/Counters and the Serial port of 8051.
• Interface 8051 to external memory and I/O devices using its I/O ports.

Module-1	**08 hrs**
8051 Microcontroller: Microprocessor Vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing. **Text2 :** Chapter 1 section 1.1 to 1.3, chapter 3 sections 3.1 to 3.3	
Teaching Learning Method: Chalk and talk method, Power Point Presentation, **RBT Level:** L1, L2, L3	

Module-2	**08 hrs**
8051 Instruction Set: Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Bit manipulation instructions. Simple Assembly language program examples (without loops) to use these instructions. **Text2 :** Chapter 5 , chapter 6, chapter 7, chapter 8	
Teaching Learning Method: Chalk and talk method, Power Point Presentation **RBT Level:** L1, L2, L3	

Module-3	**08 hrs**
8051 Jump and Call instructions & Embedded C Jump and Call Instructions, Calls & Subroutine instructions. Assembly language program examples of subroutines and involving loops. 8051 Programming in C: Data Types and Time delay in 8051 C, I/O programming in 8051 C, Logical Operations in C. **Text2 :** chapter 8 section 8.1 to 8.4.**Text1** : chapter 7 section 7.1 to 7.3	
Teaching Learning Method: Chalk and talk method, Power Point Presentation **RBT Level:** L1, L2, L3	

Module-4	**08 hrs**
8051 Timers and Serial Port 8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode- 2 on a port pin. 8051 Serial Communication- Basics of Serial Data Communication, RS- 232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially.	

Text1: Chapter 9 section 9.1 Chapter 10 section 10.1 to 10.5	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power Point Presentation, L1, L2, L3

Module-5	**08 hrs**

8051 Interrupts and Interfacing Applications.8051 Interrupts. 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a timer interrupt. Interfacing 8051 to ADC-0804, DAC, LCD and Stepper motor and their 8051 Assembly and C language interfacing programming.

Text 1: Chapter 11 section 11.1 and 11.2 Chapter 13 section 13.1 to 13.2, chapter 12 section 12.1, chapter 17 section 17.2

Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power Point Presentation L1, L2, L3

Course outcomes:

At the end of the course, the student will be able to:

CO1. Explain the difference between Microprocessors & Microcontrollers, Architecture of 8051 Microcontroller, Interfacing of 8051 to external memory and instruction set of 8051.

CO2. Develop 8051 Assembly level programs using the 8051-instruction set.

CO3. Develop 8051 Assembly / C language program to generate timings and waveform using 8051 timers, to send & receive serial data using 8051 serial ports.

CO4. Develop 8051 Assembly / C language programs to generate square wave on 8051 I/O port pin using interrupt and C Programme to send & receive serial data using 8051 serial port.

CO5. Interface various peripheral devices to 8051 using I/O ports.

Suggested Learning Resources:

Text Books:

1: Kenneth J. Ayala, "The 8051 Microcontroller", Kenneth J Ayala, 3rd Edition, Thomson/Cengage Learning.

2: Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay, "The 8051 Microcontroller and Embedded Systems – using assembly and C", PHI, 2006 / Pearson, 2006.

Reference Books:

1. "The 8051 Micro controller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.

2. "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

Web Links: https://swayam.gov.in/nd1_noc20_cs25

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity 1:

Activity 2:

Activity 3:

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	3					3	1	2		1	1	2	3
CO2	2	3	3		3			3	1	2		1	1	2	3
CO3	2	3	3		3			3	1	2		1	1	2	3
CO4	2	3	3		3			3	1	2		1	1	2	3
CO5	2	3	3	2	3			3	1	2		1	1	2	3

High-3, Medium-2, Low-1

VI Semester

BASIC VLSI DESIGN			
Course Code:	21ECT6053	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	(L:T:P :: 3:0:0)	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03 hrs

Course objectives:

1. Impart knowledge of MOS transistor theory and CMOS technologies
2. Impart knowledge on architectural choices and performance trade-offs involved in designing and realizing the circuits in CMOS technology
3. Cultivate the concepts of subsystem design processes
4. Demonstrate the concepts of CMOS testing

Module-1	**08 Hrs**
Introduction: A Brief History, MOS Transistors, MOS Transistor Theory, Ideal I-V Characteristics, Nonideal I-V Effects, DC Transfer Characteristics (1.1, 1.3, 2.1, 2.2, 2.4, 2.5 of TEXT2). **Fabrication:** nMOS Fabrication, CMOS Fabrication [P-well process, N-well process, Twin tub process], BiCMOS Technology (1.7, 1.8, 1.10 of TEXT1).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2
Module-2	**08 Hrs**
MOS and BiCMOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout. Basic Circuit Concepts: Sheet Resistance, Area Capacitances of Layers, Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit, Inverter Delays, Driving Large Capacitive Loads (3.1 to 3.3, 4.1, 4.3 to 4.8 of TEXT1).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method/Power point presentation RBT Level: L1, L2, L3
Module-3	**08 Hrs**
Scaling of MOS Circuits: Scaling Models & Scaling Factors for Device Parameters Subsystem Design Processes: Some General considerations, An illustration of Design Processes, Illustration of the Design Processes: Regularity, Design of an ALU Subsystem, The Manchester Carry chain and Adder Enhancement Techniques (5.1, 5.2, 7.1, 7.2, 8.2, 8.3, 8.4.1, 8.4.2 of TEXT1).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3
Module-4	**08 Hrs**
Subsystem Design: Some Architectural Issues, Switch Logic, Gate (restoring) Logic, Parity Generators, Multiplexers, The Programmable Logic Array (PLA) (6.1 to 6.3, 6.4.1, 6.4.3, 6.4.6 of TEXT1). **FPGA Based Systems:** Introduction, Basic concepts, Digital design and FPGAs, FPGA based System design, FPGA architecture, Physical design for FPGAs (1.1 to 1.4, 3.2, 4.8 of TEXT3).	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3
Module-5	**07 Hrs**

Memory, Registers and Aspects of system Timing: System Timing Considerations, Some commonly used Storage/Memory elements (9.1, 9.2 of TEXT1).

Testing and Verification: Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability (12.1, 12.1.1, 12.3, 12.5, 12.6 of TEXT 2).

Teaching Learning Method:	Chalk and talk method/Power point presentation
RBT Level:	RBT Level: L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.

CO2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.

CO3. Interpret Memory elements along with timing considerations.

CO4. Demonstrate knowledge of FPGA based system design.

CO5. Interpret testing and testability issues in VLSI Design and analyse CMOS subsystems.

Suggested Learning Resources:

Text Books:

1: "Basic VLSI Design"- Douglas A Pucknell & Kamran Eshraghian, PHI, 3rd Edition.

2: "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.

3: "FPGA Based System Design", Wayne Wolf, Pearson Education, 2004, Technology and Engineering.

Web Links:

https://nptel.ac.in/courses/117101058

https://nptel.ac.in/courses/117106093

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Wherever necessary Cadence/Synopsis/Menta Graphics tools must be used.

1.Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

i. An inverter

ii. A Buffer

iii. Transmission Gate

iv. Basic/universal gates

v. Flip flop -RS, D, JK, MS, T

vi. Serial & Parallel adder

vii. 4-bit counter [Synchronous and Asynchronous counter]

2. Design an op-amp with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:

a. Draw the schematic and verify the following

i) DC Analysis

ii) AC Analysis

iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS

d. Extract RC and back annotate the same and verify the Design

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	3		2								1	1	1
CO2	3	3	2										1	1	1
CO3	3	2	1										1	1	1
CO4	3	3	2										1	1	1
CO5	3	2	3										1	1	1

High-3, Medium-2, Low-1

VI Semester

ELECTRONICS CIRCUITS WITH VERILOG			
Course Code:	21ECT6054	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	(L:T:P :: 3:0:0)	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

1. To understand the basic Verilog HDL design flow.
2. To understand the basic Verilog programming concepts.
3. To describe the simple logic circuits using dataflow, gate-level, and behavioural level modelling.
4. To model digital systems using advanced concepts of Verilog HDL.

Module-1	**08 Hrs**
Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL flow, why Verilog HDL?, trends in HDLs. (Text 1) **Hierarchical Modelling Concepts:** Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. (Text 1)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
Module-2	**08 Hrs**
Basic Concepts: Lexical conventions, datatypes, system tasks, compiler directives. (Text 1) **Modules and Ports:** Module definition, port declaration, connecting ports, hierarchical name referencing. (Text 1)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
Module-3	**08 Hrs**
Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. (Text1) **Dataflow Modeling**: Continuous assignments, delay specification, expressions, operators, operands, operator types. (Text 1)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
Module-4	**08 Hrs**
Behavioral Description: Behavioral Description Highlights, Structure of the HDL Behavioral Description, Sequential Statements, IF Statement, The case Statement , Verilog casex and casez The wait-for Statement. The Loop Statement, For-Loop, While-Loop, Verilog repeat, Verilog forever (content with respect to Verilog only) (Text 2)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
Module-5	**07 Hrs**
Structural Description: Highlights of Structural Description, Organization of Structural Description Binding (4.1, 4.2, 4.3 till example 4.9) (Text 2) **Tasks and Functions:** Differences between tasks and functions, declaration, invocation, automatic tasks and functions. (Text 1)	
Teaching Learning Method: **RBT Level:**	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Understand the Verilog HDL design flow.

CO2. Describe the basic concepts of Verilog HDL programming

CO3. Design of digital electronics circuits using dataflow, behavioural, gate-level, and structural modelling.

CO4. Design complex digital circuits using advanced Verilog concepts.

Suggested Learning Resources:

Text Books:

1: "Verilog HDL: A Guide to Digital Design and Synthesis", Samir Palnitkar, Pearson education, Second edition.

2: "HDL programming (VHDL and Verilog)", Nazeih M Botros, John Wiley India Pvt. Ltd., 2008.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Wherever necessary Xilinx/Model sim, Questa tools must be used.

1.Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

i. An inverter

ii. A Buffer

iii. Transmission Gate

iv. Basic/universal gates

v. Flip flop -RS, D, JK, MS, T

vi. Serial & Parallel adder

vii. 4-bit counter [Synchronous and Asynchronous counter]

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	CO1	3	3	3		2								1	1
CO2	CO2	3	3	2										1	1
CO3	CO3	3	2	1										1	1
CO4	CO4	3	3	2										1	1

High-3, Medium-2, Low-1

VI Semester

SENSORS & ACTUATORS			
Course Code:	21ECE6055	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

- To provide the fundamental knowledge about sensors and measurement system.
- To impart the knowledge of static and dynamic characteristics of instruments and understand the factors in selection of instruments for measurement.
- To discuss the principle, design and working of transducers for the measurement of physical time varying quantities.
- Understand the working of various actuators suitable in industrial process control systems.
- Understand the principle and application of smart sensors.

Module-1

Sensors and measurement system: Sensors and transducers, Classifications of transducers-primary & secondary, active & passive, analog and digital transducers. Smart sensors.

Measurement: Definition, significance of measurement, instruments and measurement systems. mechanical, electrical and electronic instruments. Elements of generalized measurement system with example. Input-output configuration of measuring instruments and measurement systems, methods of correction for interfering and modifying inputs.

Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, More examples relating to applications
RBT Level:	L1, L2, L3

Module-2

Static and Dynamic Characteristics: Static calibration and error calibration curve, accuracy and precision, indications of precision, static error, scale range and scale span, reproducibility and drift, repeatability, signal to noise ratio, sensitivity, linearity, hysteresis, threshold, dead zone and dead time, resolution, signal to noise ratio, factors influencing the choice of transducers/instruments. Dynamic response – Dynamic characteristics, Transfer function of generalized first order system, time constant. Transfer function of generalized second order system, natural frequency and Damping ratio.

Teaching Learning Method:	Chalk and talk method, Power point presentation, VI Lab to demonstrate the characteristics of sensors, More examples relating to applications
RBT Level:	L1, L2, L3

Module-3

Measurement of Temperature: RTD, Thermistor, Thermocouple, laws of thermocouple, Thermopile, AD590.

Measurement of Displacement: Introduction, Principles of Transduction, Variable resistance devices, variable Inductance Transducer, Variable Capacitance Transducer, Hall Effect Devices, Proximity Devices, Digital Transducer.

Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, Virtual instrumentation Lab to demonstrate the characteristics of sensors
RBT Level:	L1, L2, L3

Module-4	
Measurement of Strain: Introduction, Types of Strain Gauges, Theory of operation of resistance strain gauges, Types of Electrical Strain Gauges –Wire gauges, unbounded strain gauges, foil gauges, semiconductor strain gauges (principle, types & list of characteristics only), Strain gauge Circuits – Wheatstone bride circuit, Applications. **Measurement of Force & Torque:** Introduction, Force measuring sensor –Load cells – column types devices, proving rings, cantilever beam, pressductor. Hydraulic load cell, electronic weighing system. Torque measurement: Absorption type, transmission type, stress type & deflection type.	
Teaching Learning Method:	Chalk and talk method, PowerPoint Presentation, More examples relating to applications
RBT Level:	L1, L2, L3
Module-5	
Actuators and process control system: Introduction. Block diagram and description of process control system with an example. Introduction, Block diagram of Final control operation, Signal conversions analog, digital, pneumatic signal. Actuators, Control elements. **Electrical actuating systems:** Solid-state switches, Solenoids, Electric Motors- Principle of operation and its application: D.C motors, AC motors, Synchronous Motor, Stepper motors. **Pneumatic Actuators**: Principle and working of pneumatic actuators. (Numerical problems on the topic). **Hydraulic Actuators:** Principle and working of Hydraulic actuators. (Numerical problems on the topic).	
Teaching Learning Method:	Chalk and talk method, Power point presentation, More examples relating to applications
RBT Level:	L1, L2, L3
Course outcomes: **At the end of the course the student will be able to:** **CO1:** Discuss the fundamental concepts related to sensors and measurement, functional elements of measurement system, I/O Characteristics of measurement system. **CO2:** Interpret and analyse the static and dynamic characteristics of instruments. **CO3:** Elucidate the working principle and usage of different transducers for temperature, displacement and level measurement. **CO4:** Discuss the principle and working of different types of actuators used in industrial application. **CO5:** Discuss the principle and working of strain, force and torque measurement	
Suggested Learning Resources: **Text Books:** 1.Electrical and Electronic Measurements and Instrumentation, A K Sawhney, 17th Edition, (Reprint 2004), Dhanpat Rai & Co. Pvt. Ltd., 2004. 2. Instrumentation: Devices and Systems, C S Rangan, G R Sarma, V S V Mani, 2nd Edition (32 Reprint), McGraw Hill Education (India), 2014. 3. Process Control Instrumentation Technology by C D Johnson, 7th Edition, Pearson Education Private Limited, New Delhi 2002.	
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning **Activity 1:** **Activity 2:** **Activity 3:**	

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1															
CO2															
CO3															
CO4															
CO5															

High-3, Medium-2, Low-1

VI Semester

VLSI LAB			
Course Code	21ECL606	**CIE Marks**	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	**SEE Marks**	50
Credits	01	**Exam Hours**	03

Course objectives:

This laboratory course enables students to

1. Design, model, simulate and verify CMOS digital circuits
2. Design layouts CMOS digital circuits
3. Perform physical verification of CMOS digital circuits
4. Perform RTL- flow and understand the stages in ASIC design.

Sl. No.	Experiments
1	DC, Transient analysis of CMOS logic-Universal gates schematic
2	DC, Transient analysis of CMOS full adder schematic
3	DC, Transient analysis of Pass transistor and transmission gates schematic
4	DC, Transient analysis of Sequential circuits schematic 1. Clocked D Latch 2. Master-Slave Edge Triggered Register
5	DRC and LVS analysis of CMOS Inverter layout
6	DRC and LVS analysis of Common Source Amplifier Layout
7	DRC and LVS analysis of Common Drain Amplifier Layout
8	DRC and LVS analysis of Differential Amplifier Layout
09	Synthesis and Simulation of Inverter using Verilog code
10	Synthesis and Simulation of Buffer Verilog code
11	Synthesis and Simulation of Basic/Universal Gate using Verilog code
12	Synthesis and Simulation of JK, MSJK flip-flops using Verilog code

Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

CO1. Design and simulate basic CMOS circuits like different logic structures.

CO2: Design and simulate basic CMOS circuits like inverter, common source amplifier and Differential Amplifier.

CO3: Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list.

CO4: Design and simulate combinational and sequential digital circuits using Verilog HDL.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1															
CO2															
CO3															
CO4															

` **High-3, Medium-2, Low-1**

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

VII Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	PCC	21ECT701	Advanced VLSI	ECE	3	0	0		3	3	50	50	100	3
2	PCC	21ECT702	Optical & Wireless Communication	ECE	2	0	0		3	3	50	50	100	2
3	PEC	21ECT703X	Professional elective Course-II	ECE	3	0	0		3	3	50	50	100	3
4	PEC	21ECT704X	Professional elective Course-III	ECE	3	0	0		3	3	50	50	100	3
5	OEC	21ECT705X	Open elective Course-II		3	0	0		3	3	50		100	3
6	Project	21ECP706	Project work	ECE						3	100	50	200	10
Total											350	450	700	24

Professional Elective Courses-II		Professional Elective Courses-III		Open Elective Courses-II	
Subject Code	Title	Subject Code	Title	Subject Code	Title
21ECT7031	Operating System	21ECT7041	IOT & wireless sensor networks	21ECT7051	Optical & Satellite Communication
21ECT7032	Digital Image Processing	21ECT7042	Network Security	21ECT7052	ARM Embedded Systems
21ECT7033	DSP Algorithms & Architecture	21ECT7043	Fabrication technology	21ECT7053	Basic Digital Image Processing
21ECT7034	Power Electronics	21ECT7044	Machine Learning with Python	21ECT7054	Cryptography
21ECT7035	Operational Research	21ECT7045	Multimedia Communication	21ECT7055	E-waste Management

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

VIII Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week				Examination				Credits
					L	T	P	S	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	Seminar	21ECS801	Technical Seminar		One contact hour /week for interaction between the faculty and students				--	100	---	100	01
2	Research Internship/ Industry Internship	21ECI802	Research/Industry Internship*		Two contact hours /week for interaction between the faculty and students.				3 (Batch wise)	100	100	200	15
3	NCMC	21EC803	National Service Scheme (NSS)	NSS	Completed during the intervening period of III semester to VIII semester.				--	50	50	100	--
		21EC803	Physical Education (PE) (Sports & Athletics)	PE									
		21EC803	Yoga	Yoga									
									Total	250	150	400	16

Note: (1) University /Institutions may swap 7th and 8th Semester Course work to accommodate industry/research internship at the end of sixth semester /at the end of seventh semester to balance the workload. (2) Credits earned for the course prescribed will be accounted in 8th semester

Dr. Ambedkar Institute of Technology, Bengaluru-560056

Outcome Based Education(OBE) and Choice Based Credit System (CBCS) (As per NEP2020)

B.E. Electronics & Communication Engineering

Tentative Scheme of Teaching and Examination effective from the Academic Year 2022-23

(Applicable to 2021 batch)

VII Semester

Sl. No.	Course Category	Course Code	Course Title	Teaching Department	Teaching Hrs/ Week					Examination				Credits
					L	T	P	S	Total	Duration (Hrs)	CIE Marks	SEE Marks	Total Marks	
1	PCC	21ECT701	Advanced VLSI	ECE	3	0	0		3	3	50	50	100	3
2	PCC	21ECT702	Optical & Wireless Communication	ECE	2	0	0		3	3	50	50	100	2
3	PEC	21ECT703X	Professional elective Course-II	ECE	3	0	0		3	3	50	50	100	3
4	PEC	21ECT704X	Professional elective Course-III	ECE	3	0	0		3	3	50	50	100	3
5	OEC	21ECT705X	Open elective Course-II		3	0	0		3	3	50		100	3
6	Project	21ECP706	Project work	ECE						3	100	50	200	10
Total											350	450	700	24

Professional Elective Courses-II		Professional Elective Courses-III		Open Elective Courses-II	
Subject Code	Title	Subject Code	Title	Subject Code	Title
21ECT7031	Operating System	21ECT7041	IOT & wireless sensor networks	21ECT7051	Optical & Satellite Communication
21ECT7032	Digital Image Processing	21ECT7042	Network Security	21ECT7052	ARM Embedded Systems
21ECT7033	DSP Algorithms & Architecture	21ECT7043	Fabrication technology	21ECT7053	Basic Digital Image Processing
21ECT7034	Power Electronics	21ECT7044	Machine Learning with Python	21ECT7054	Cryptography
21ECT7035	Operational Research	21ECT7045	Multimedia Communication	21ECT7055	E-waste Management

VII Semester

ADVANCED VLSI			
Course Code:	21EC71	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:1	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

1. Learn the overall VLSI design flow.
2. Emphasize on circuit modelling and optimization.
3. Familiarise with the basic VLSI design automation methods.

Module-1	**08 hrs**
DYNAMIC LOGIC CIRCUITS : Static Behavior: BiCMOS Logic , BiCMOS Applications, Dynamic CMOS Logic, DOMINO Logic Circuit. **SEQUENTIAL MOS LOGIC CIRCUITS**:, The SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, CMOS D-Latch **[TEXT 1]**	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-2	**08 hrs**
DATAPATH LOGIC CELLS **Data path Subsystem I:** Single bit addition, carry generation & propagation, PG Carry-Ripple Addition, carry skip adder, carry save carry select, conditional sum adders , Array Multiplication (Modified Baugh-Wooley two's complement Multiplier), Booth encoding (Radix 4). **[TEXT 1]** **Introduction to ASICS**: Types of ASICS, Design Flow **[TEXT 2]**	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-3	**08 hrs**
Circuits and Models: Graph Optimization problems and algorithms: Shortest and Longest path problems, vertex cover, graph coloring, clique covering and clique partitioning. **Boolean algebra and applications**: Boolean functions, representation of Boolean functions. **[TEXT 3]**	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3

Module-4	**08 hrs**
Hardware Modelling: Introduction, Hardware modelling languages, Abstract models -Structures, Logic networks, State diagrams, data-flow and sequencing graphs, Compilation and Behavioral optimization-Compilation techniques, optimization techniques. **[TEXT 3]**	
Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	L1, L2, L3

Module-5	**08 hrs**
Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. **Placement**: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, **Routing**: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks. **[TEXT 2]**	

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO 1- Understand the various VLSI logic circuits.
CO 2 – Describe the design concepts of data-path sub-systems and ASIC design methodology.
CO 3 - Apply the concepts of optimization of VLSI design at different abstract levels.
CO 4 –Understand the necessity of hardware modelling.
CO 5 – Create the automated floorplan, placement and routing algorithms.

Suggested Learning Resources:

Text Books:

1. Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits", WCB Mc Graw Hill,2003.
2. Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Pearson, 2016.
3. Giovanni De Micheli, "Synthesis and optimization of digital circuits", Tata Mc Graw Hill, 2005.

Reference Books:

1. Neil Weste, David Harris, "CMOS VLSI Design "Pearson, 2011.
2. N. A Sherwani, "Algorithms for VLSI Physical Design Automation", Springer-Verlag, 2013.
3. K V K K Prasad, "Embedded real time systems", Dreamtech publications, 2003.
4. Rajkamal, "Embedded Systems",2nd Edition, McGraw hill Publications, 2010.
5. P Augusta Sophy Beulet, Jie Li, A Ravi Sankar, "VLSI Design: Circuits, Systems and Applications", Lecture Notes in Electrical Engineering, ICNET2 proceedings, Springer, 2018.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	1	1	1						1			3	2	1
CO2	3	2	2	1	2	1	1	1		1	1	2	3	2	1
CO3	3	2	1	1				1	1	1			3	2	1
CO4	3	1	1		1		1	1	1	1		1	3	2	1
CO5	3	1	1		1				1	1			3	2	1

High-3, Medium-2, Low-1

VII Semester

OPTICAL AND WIRELESS COMMUNICATION			
Course Code:	21ECT702	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	2:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	26	**Total Marks:**	100
Credits:	02	**Exam Hours:**	03

Course objectives:

1. Learn the basic principle of optical fiber communication with different modes of light propagation.
2. Understand the transmission characteristics and losses in optical fiber and Study of optical components and its applications in optical communication networks.
3. Understand the concepts of propagation over wireless channels from a physics standpoint
4. Understand the multiple access techniques used in cellular communications standards.
5. Application of Communication theory both Physical and networking to understand GSM systems that handle mobile telephony.

Module-1	**05 hrs**

Optical Fiber Structures: Optical Fiber Modes and Configurations, Mode theory for circular waveguides, Single mode fibers, Fiber materials.

Attenuation and Dispersion: Attenuation, Absorption, Scattering Losses, Bending loss, Signal Dispersion: Modal delay, Group delay, Material dispersion.

[Text1 : 3.1, 3.2, 2.3[2.3.1 to 2.3.4], 2.4[2.4.1, 2.4.2],2.5, 2.7].

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-2	**05 hrs**

Optical Sources and detectors: Light Emitting Diode: LED Structures, Light source materials, Quantum efficiency and LED power, Laser Diodes: Modes and threshold conditions, Rate equations, External quantum efficiency, Resonant frequencies, Photodetectors: The pin Photodetector, Avalanche Photodiodes.

WDM Concepts: Overview of WDM, Isolators and Circulators, Fiber grating filters, Dielectric thin-film filters, Diffraction Gratings.

[Text1: 4.2 ,4.3, 6.1, 10.1, 10.3, 10.4, 10.5, 10.7]

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-3	**07 hrs**

Mobile Communication Engineering: Wireless Network generations, Basic propagation Mechanisms, Mobile radio Channel.

Principles of Cellular Communications: Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Frequency Reuse Distance, Cochannel Interference and signal quality.

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3

Module-4	**04 hrs**

Multiple Access Techniques: FDMA, TDMA, CDMA, SDMA, Hybrid Multiple Access Techniques, Multicarrier Multiple Access Schemes.

Teaching Learning Method: **RBT Level:**	Chalk and Talk, Power point presentations L1, L2, L3

Module-5	**05 hrs**

Global System for Mobile (GSM): GSM Network Architecture, GSM Channels, Frame structure for GSM, GSM Call procedures, GSM hand-off Procedures, GSM Services and features. [Text2: 11.1, 11.2,11.3,11.4, 11.5, 11.8, 11.9. 11.10]

Teaching Learning Method: **RBT Level:**	Chalk and Talk, Power point presentations **RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Explain classification and characterization of optical fibers with different modes of signal propagation.

CO2. Describe the constructional features and the characteristics of optical fiber and optical devices used for signal transmission and reception.

CO3. Understand the essential concepts and principles of mobile radio channel and cellular communication.

CO 4. Describe various multiple access techniques used in wireless communication systems.

CO 5. Describe the GSM architecture and procedures to establish call set up, call progress handling and call tear down in a GSM cellular network.

Suggested Learning Resources:

Text Books

1. Gerd Keiser, Optical Fiber Communication, 5th Edition, McGraw Hill Education (India) Private Limited, 2016. ISBN:1-25-900687-5.

2. T L Singal, Wireless Communications, McGraw Hill Education (India) Private Limited, 2016, ISBN:0 07-068178-3.

Reference Books

1. John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010, ISBN:978-81-317-3266-3

2. Theodore Rappaport, Wireless Communications: Principles and Practice, 2nd Edition, Prentice Hall Communications Engineering and Emerging Technologies Series, 2002, ISBN 0-13-042232-0.

3. Gary Mullet, Introduction to Wireless Telecommunications Systems and Networks, First Edition, Cengage Learning India Pvt Ltd., 2006, ISBN - 13: 978-81-315-0559-5.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	1	1			3	3					1	2	1	
CO2	3	1	1	2		2	1					1	1		
CO3	3					1	1					1	1		
CO4	3					1	1					1	1	2	
CO5	3		1			2	1					1	1	1	

High-3, Medium-2, Low-1

VII Semester

OPERATING SYSTEMS			
Course Code:	21ECT7031	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3: 0: 0: 0	**SEE Marks:**	50
Total Hours of Pedagogy:	39	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

This course will enable students to understand:

1. the history and types of operating systems.
2. the design issues associated with operating systems development.
3. the process management and scheduling of operating system.
4. the concepts of memory management of operating system.
5. the file and I/O operations of operating system.

Module 1	**07 hrs**

INTRODUCTION: Goals of an O.S, Operation of an O.S

OVERVIEW OF OPERATING SYSTEMS: OS and computer system, Efficiency, system performance and user convenience, Classes of operating systems, O.S and the computer system, Batch processing system, Multi programming systems, Time sharing systems, Real time operating systems. **TEXT 1**

Teaching Learning Method:	Chalk and Board, PowerPoint Presentation
RBT Level:	L1, L2

Module 2	**08 hrs**

STRUCTURE OF THE OPERATING SYSTEMS: Operation of an O.S, Structure of an operating system, Operating systems with monolithic structure, Layered design of an operating system, Virtual machine operating systems, Kernel based operating systems. **TEXT1**

Teaching Learning Method:	Chalk and Board, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module 3	**08 hrs**

PROCESS MANAGEMENT: Process and programs, Programmer view of processes, OS view of processes, Threads.

SHEDULING: Preliminaries, Non pre-emptive scheduling policies, pre-emptive scheduling policies, scheduling in practice. **TEXT 1**

Teaching Learning Method:	Chalk and Board, Power Point Presentation
RBT Level:	L1, L2, L3

Module 4	**08 hrs**

MEMORY MANAGEMENT: Managing the memory hierarchy, static and dynamic memory allocations, memory allocation to a process, reuse of memory, contiguous and non contiguous memory allocation, paging, segmentation, segmentation with paging.

VIRTUAL MEMORY: Virtual memory Basics, Demand paging, page replacement policies. **TEXT 1**

Teaching Learning Method: **RBT Level:**	Chalk and Board, PowerPoint Presentation L1, L2

Module 5	**08 hrs**

FILE SYSTEMS: File system and IOCS, Files and file organization, Fundamentals of file organizations, Directory structures, File protection, Interface between file system and IOCS, Allocation of disk space. implementation of file access. **TEXT 1**

Teaching Learning Method: **RBT Level:**	Chalk and Board, Power Point Presentation L1, L2

Course outcomes

CO1: Understand the evolution of operating systems and various types of operating systems in practice

CO2: Analyse the structure of operating system.

CO3: Analyse the concepts of process management and different scheduling management.

CO4: Understand the design issues in memory management and virtual memory.

CO5: Understand the file and I/O management techniques.

Suggested Learning Resources:

Text Book:

1. D. M. Dhamdhare, "Operating Systems", Second Edition, TMH, 2008

Reference Books:

1. Stalling William, "Operating Systems", Sixth edition, Pearson Education,
2. Avi Silberchatz, Peter Baer Galvin, Greg Gagne, "Operating system Concepts", Ninth edition, John wiley & Sons

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Seminar on different types of Operating System.
2. Problems on Scheduling Policies.
3. Posters about Fundamental Functions of Operating System.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	2		2								1			
CO2		2	2	2						2		2			
CO3	2	2	2			1	1					1			
CO4	2	2		2							1	1			
CO5	2	2									1	1			

High-3, Medium-2, Low-1

Semester VII

DIGITAL IMAGE PROCESSING			
Course Code:	21ECT7032	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

- Understand the fundamentals of digital image processing.
- Understand the image transform used in digital image processing.
- Understand the image enhancement techniques in spatial domain used in digital image processing.
- Understand the Color Image Processing and frequency domain enhancement techniques in digital
- Image processing.
- Understand the image restoration techniques and methods used in digital image processing.

Module-1	**08 hours**
Digital Image Fundamentals: What is Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels. [Text 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]	
Teaching Learning Method:	Chalk and Talk, power point presentation, animations, videos
RBT Level:	**L1,L2**
Module-2	**08 hours**
Image Transforms: Introduction, Two-Dimensional Orthogonal and Unitary Transforms, Properties of Unitary Transforms, Two-Dimensional DFT, cosine Transform, Haar Transform. Text 2: Chapter 5: Sections 5.1 to 5.3, 5.5, 5.6, 5.9]	
Teaching Learning Method:	Chalk and Talk, power point presentation, animations, videos
RBT Level:	**L1,L2.**
Module-3	**09 hours**
Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters [Text: Chapter 3: Sections 3.2 to 3.6].	
Teaching Learning Method:	Chalk and Talk, power point presentation, animations, videos
RBT Level:	**L1,L2,L3**
Module-4	**08 hours**
Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters. **Color Image Processing:** Color Fundamentals, Color Models, Pseudo-color Image Processing. [Text 1: Chapter 4: Sections 4.7 to 4.9 and Chapter 6: Sections 6.1 to 6.3]	
Teaching Learning Method:	Chalk and Talk, power point presentation, animations, videos
RBT Level:	**L1,L2, L3**
Module-5	**07hours**

Restoration: A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering.
[Text 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8]

Teaching Learning Method:	Chalk and Talk, power point presentation, animations, videos
RBT Level:	**L1,L2,L3**

Course outcomes:

At the end of the course the student will be able to:

CO1. Understand image formation and the role of human visual system plays in perception of gray and Color image data.

CO2.Compute various transforms on digital images.

CO3.Conduct independent study and analysis of Image Enhancement techniques.

CO4.Apply image processing techniques in frequency (Fourier) domain.

CO5.Design image restoration techniques.

Suggested Learning Resources:

Text Books:

1. Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3rd Edition 2010.
2. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014.

Reference Book:

Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014.

Web links and Video Lectures (e-Resources)

- Image databases, https://imageprocessingplace.com/root_files_V3/image_databases.htm
- Student support materials, https://imageprocessingplace.com/root_files_V3/students/students.htm
- NPTEL Course, Introduction to Digital Image Processing, https://nptel.ac.in/courses/117105079
- Computer Vision and Image Processing, https://nptel.ac.in/courses/108103174
- Image Processing and Computer Vision – Matlab and Simulink,
- https://in.mathworks.com/solutions/image-video-processing.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Verilog /VHDL coding for Image manipulation.
- Simulink models for Image processing.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	2		1								1	2	1
CO2	3	2	2		1								1	2	1
CO3	3	3	2		1								1	2	1
CO4	3	1	2		1								1	2	1
CO5	3	1	1		1								1	2	1

High-3, Medium-2, Low-1

VII Semester

DSP ALGORITHMS &ARCHITECTURE			
Course Code:	21ECT7033	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

1. To gain the knowledge of basics of DSP like FIR filters, IIR filters, FFT algorithms, architectures of DSP processors and interfacing to other devices
2. To interpret the basics of DSP like FIR filters, IIR filters, FFT algorithms, architectures of DSP processors and interfacing to other devices
3. To apply the concept of FIR filters, IIR filters, FFT algorithms, architectures of DSP processors and interfacing to other devices
4. To illustrate the basics of DSP like FIR filters, IIR filters, FFT algorithms, architectures of DSP processors and interfacing to other devices
5. To design and implement the FIR filters, IIR filters, FFT algorithms on DSP processor.

Module-1	**08 hrs**

Introduction to Digital Signal Processing: Introduction, a Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation.

Architectures for Programmable Digital Signal Processors:

Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing.

TEXT 1

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-2	**08 hrs**

Programmable Digital Signal Processors: Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54xx., Memory Space of TMS32OC54xx Processors, Program Control.

Detail Study of TMS320C54X & 54xx Instructions and Programming, On-Chip peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.

Text 1

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-3	**08 hrs**

Implementation of Basic DSP Algorithms: Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case).

Implementation of Basic DSP Algorithms: Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case).

Text 1

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos

RBT Level:	L1, L2, L3

Module-4	08 hrs

Implementation of FFT Algorithms: Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit-Reversed Index Generation & Implementation on the TMS32OC54xx.

Interfacing Memory and Parallel I/O Peripherals to DSP Devices: Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I / O Direct Memory Access (DMA).
TEXT 1

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	L1, L2, L3

Module-5	08 hrs

Interfacing and Applications of DSP Processor: Introduction, Synchronous Serial Interface, A CODEC Interface Circuit. DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.
TEXT 1

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1 Define the fundamentals of DSP and the general architecture of DSP

CO2 Understand the general architecture of DSP processor and in particular TMS320C54xx DSP to run algorithms.

CO3 Applying the concept of DSP algorithms when they are run on processors.

CO4 Analyze the implementation of FFT algorithms and interfacing memory to DSP processor.

CO5 Creating new designs based on existing algorithms targeted to DSP processor.

Suggested Learning Resources:

Text Books:

1. Avatar Singh and S. Srinivasan, "Digital Signal Processing", Third Edition, Thomsoc Learning, 2004.

Reference Books:

1."Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002.

2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010

3. "Architectures for Digital Signal Processing", Peter Pirsch John Weily, 200

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2												3	
CO2	3	2												3	
CO3	3	2												3	
CO4	3	2	2		2		1		1					3	
CO5	3	2	2		2		1		1					3	

High-3, Medium-2, Low-1

VII Semester

POWER ELECTRONICS			
Course Code:	**21ECT7034**	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	2:2:2:0	**SEE Marks:**	50
Total Hours of Pedagogy:	52 Hours	**Total Marks:**	100
Credits:	4 (2:1:1)	**Exam Hours:**	03 Hrs

Course objectives:

From this course the students can learn

1. Understanding of fundamentals of power electronics and various power devices/Thyristors.
2. Explaining the working principles of various types of AC-DC, DC-DC, DC-AC, and AC-DC converters.
3. Describing the requirements and working of gate drive circuits.

Module-1

Introduction

Power Electronics defined, Characteristics, Diode as a switch, properties of PN Junction, Common diode types, Diode ratings, and Snubber circuits for diode, series and parallel connection of power diodes, Applications of diodes.

Thyristors

Introduction, Basic Structure and Operation, Static Characteristics, Dynamic Switching Characteristics, Thyristor Parameters, Types of Thyristors, Gate Drive Requirements.

Text Book1:

Teaching Learning Method:	Chalk and Board, Problem Based Learning
RBT Level:	L1, L2

Module-2

Power Devices

Gate Turn-Off Thyristors-Basic Structure and Operation, GTO Thyristor Models, Static Characteristics, Switching Phases, **Power Bipolar Transistors**-Basic Structure and Operation, Static Characteristics, Dynamic Switching Characteristics, **The Power MOSFET**-MOSFET Structure, MOSFET Regions of Operation, **Insulated Gate Bipolar Transistor**- Basic Structure and Operation, Static Characteristics, Dynamic Switching Characteristics, IGBT Performance Parameters, Gate-Drive Requirements, **MOS Controlled Thyristors (MCTs)**- Equivalent Circuit and Switching Characteristics, Comparison of MCT and Other Power Devices, Gate Drive for MCTs, Protection of MCTs, Simulation Model of an MCT, Generation-1 and Generation-2 MCTs, Base Resistance-Controlled Thyristor, N-channel MCT, MOS Turn-Off Thyristor, Applications of PMCT, **Static Induction Devices**-Theory of Static Induction Devices, Characteristics of Static Induction, Transistor, Bipolar Mode Operation of SI devices (BSIT), Emitters for Static Induction Devices, Static Induction Diode (SID).

Teaching Learning Method:	Chalk and Board, Problem Based Learning
RBT Level:	L1, L2

Module-3

Diode Rectifiers

Single-Phase Diode Rectifiers, Three phase diode rectifiers, Filtering Systems in Rectifier, Single-Phase Controlled Rectifiers Circuits, Line Commutated Single-Phase Controlled Rectifiers, Line commutated Three phase controlled rectifiers.

Teaching Learning Method:	Chalk and Board, Problem Based Learning
RBT Level:	L1, L2, L3

Module-4

DC-DC Converters

Introduction, DC Choppers, Step-Down (Buck) Converter, Step-Up (Boost) Converter, Buck-Boost Converter, Cuck Converter. Effects of Parasitic, Synchronous and Bidirectional Converters, Control Principles, Applications of DC-DC Converters.

Inverters

Introduction, Single-Phase Voltage Source Inverters, Current Source Inverters.

Teaching Learning Method:	Chalk and Board, Problem Based Learning
RBT Level:	L1, L2, L3

Module-5

AC-AC Converters

Introduction, Single-Phase AC-AC Voltage Controller, Applications of AC/AC Converters

Gate Drive Circuits

Introduction, Thyristor Gate Requirements, Trigger Circuits for Thyristors, Simple Gate Trigger Circuits for Thyristors,

Text Book3: 8.1, 8.2, 8.4, 8.6

Teaching Learning Method:	Chalk and Board, Problem Based Learning
RBT Level:	L1, L2, L3

Course outcomes:

After successful completion of this course, the students will be able to

CO1. Explain the basics of power electronics and structure of thyristors with characteristics.

CO2. Describe the various power devices with their characteristics and applications.

CO3. Explain the working principle of rectifiers.

CO4. Illustrate DC-DC converters and Inverters working principle with control principles.

CO5. Illustrate AC-AC converters and gate drive circuits.

Assessment Details (both CIE and SEE):

Suggested Learning Resources:

Text Books:

Text book 1: Muhammed H Rashid, "Power Electronics Handbook", Academic Press, 3rd Edition.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity 1: Quizzes

Activity 2: Seminars

Activity 3: Simulation
Activity 4: Case studies

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	**2**	**1**										**2**	**3**		
CO2	**3**	**1**										**2**	**3**		
CO3	**3**	**1**	**1**									**2**	**3**		
CO4	**3**	**1**	**1**									**2**	**3**		
CO5	**3**	**1**	**1**									**2**	**3**		

High-3, Medium-2, Low-1

VII Semester

OPERATIONS RESEARCH			
Course Code:	21ECT703**5**	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

1. To be able to understand Scope of Operations Research and TP Formulation.
2. To be able to understand the Assignment Problem.
3. To be able to understand the Network Construction.
4. To be able to classify the type Game Theory.
5. To be able to understand the Queuing system and their characteristics.

Module-1	**08 hrs**
Introduction to Operations Research: Basics definition, scope, objectives, phases, models and limitations of Operations Research. **Transportation Problem:** Formulation, solution, unbalanced Transportation problem. Finding basic feasible solutions – Northwest corner rule, least cost method and Vogel's approximation method. **Text1**	
Teaching Learning Method: **RBT Level:**	Chalk and Talk, PowerPoint Presentation L1, L2, L3
Module-2	**08 hrs**
Assignment model: Formulation. Hungarian method for optimal solution. Solving unbalanced problem. Traveling salesman problem and assignment problem. **Text1**	
Teaching Learning Method: **RBT Level:**	Chalk and Talk, PowerPoint Presentation L1, L2, L3
Module-3	**08 hrs**
PERT-CPM Techniques: Network construction, determining critical path, floats, scheduling by network, project duration, variance under probabilistic models, prediction of date of completion, crashing of simple networks. **Text1**	
Teaching Learning Method: **RBT Level:**	Chalk and Talk, PowerPoint Presentation, YouTube videos L1, L2, L3
Module-4	**08 hrs**
Game Theory: Formulation of games, Two person-Zero sum game, games with and without saddle point, Graphical solution (2x n, m x 2 game). **Text1**	
Teaching Learning Method: **RBT Level:**	Chalk and Talk, Power point presentations L1, L2, L3
Module-5	**08 hrs**

Queuing Theory: Queuing system and their characteristics. The M/M/1 Queuing system, Steady state performance analyzing of M/M/ 1 and M/M/C queuing model.

Text1

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO 1 - Understand the OR Definitions and apply to TP and Assignment problems.
CO 2 - Analyze the Assignment problems and Game theory with and without Saddle point.
CO 3 - Apply the PERT-CPM techniques to find the critical path, floats and scheduling by network.
CO 4 - Analyze the Assignment problems and Game theory with and without Saddle point.
CO 5 - Evaluate the Queuing system and their characteristics.

Suggested Learning Resources:

Text Books:

1. S D Sharma, "Operations Research (Theory Methods & Applications)", Kedar Nath Ram Nath, 2020th edition

Reference Books:

1. J K Sharma, "Operations Research, Problems and Solutions", Third Edition, Macmillan India Ltd, 2010.
2. A.M. Natarajan, P. Balasubramani, A. Tamilarasi, "Operations Research", First Edition, Pearson Education, 2005

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3						2	2	2					
CO2	2	2						3	3	3					
CO3	1	1						3	2	2					
CO4	2	2	2					2	3	3					
CO5	3	3						2	2	2					

High-3, Medium-2, Low-1

VII Semester

IOT & WIRELESS SENSOR NETWORKS			
Course Code:	**21ECT7041**	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

- To provide an exposure to the broad perspective of Internet of Things with respect to the characteristics, design, technologies and applications.
- To provide a basic understanding of the important aspects of Wireless sensor networks covering applications, sensor and transmission technology & systems, middleware, performance and traffic management

Module-1	**08 hrs**
Internet of Things: Introduction, Physical design, Logical design, Enabling technologies, Levels & deployment templates. Text 1: Chapter 1	
Teaching Learning Method: Chalk and Talk, PowerPoint Presentation **RBT Level:** L1, L2	
Module-2	**08 hrs**
Domain Specific IoTs: Home automation, cities, environment, energy, retail, logistics, agriculture, industry, health & lifestyle. Text 1: Chapter 2	
Teaching Learning Method: Chalk and Talk, PowerPoint Presentation **RBT Level:** L1, L2, L3	
Module-3	**08 hrs**
Wireless Sensor Networks: Introduction, applications of sensor networks, basic overview of the technology, basic sensor network architectural elements, present day sensor network research, challenges and hurdles, examples of Category 2 WSN applications, examples of Category 1 WSN applications	
Teaching Learning Method: Chalk and Talk, PowerPoint Presentation, YouTube videos **RBT Level:** L1, L2, L3	
Module-4	**08 hrs**
Wireless sensor technology: Introduction, sensor node technology – overview, hardware and software, sensor taxonomy, WN operating environment, WN trends. **Wireless Transmission technology and systems:** Introduction, Campus applications, MAN/WAN applications. Text 2: Chapter 3: 3.1, 3.2 – 3.2.1, 3.2.2, 3.3, 3.4, 3.5 Chapter 4: 4.1, 4.3.1, 4.3.2	
Teaching Learning Method: Chalk and Talk, Power point presentations **RBT Level:** L1, L2, L3	
Module-5	**08 hrs**

Middleware for WSNs: Introduction, principles, architecture, data related functions
Performance and traffic management: background, WSN Design issues, performance modelling of WSNs.
Text 2: Chapter 8: 8.1, 8.2, 8.3, 8.3.1 Chapter 11: 11.2, 11.3, 11.4

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO 1 - Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.
CO 2 - Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
CO 3 - Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
CO 4 - Develop the hardware Software co-design and firmware design approaches.
CO 5 - Explain the need of real time operating system for embedded system applications.

Suggested Learning Resources:

Text Books:

1. 'Internet of Things', Arshdeep Bagha and Vijay Madisetti, Universities Press, 2015
2. 'Wireless Sensor Networks', Kazem Sohraby, Daniel Minoli and Taieb Znati, Wiley, 2015.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2												3	
CO2	3	2												3	
CO3	3	2												3	
CO4	3	2	2		2		1		1					3	
CO5	3	2	2		2		1		1					3	

High-3, Medium-2, Low-1

VII Semester

NETWORK SECURITY			
Course Code:	**21ECT7042**	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

- **Preparation**: To prepare students with fundamental knowledge/ overview in the field of Network Security with knowledge of security mechanisms and services.
- **Core Competence**: To equip students with a basic foundation of Network Security by delivering the basics of Transport Level Security, Secure Socket Layer, Internet Protocol security, Intruders, Intrusion detection and Malicious Software, Firewalls, Firewall characteristics, Biasing and Configuration.

Module-1	**08 hrs**
Attacks on Computers and Computer Security: Need for Security, Security Approaches, Principles of Security Types of Attacks. **(Text2: Chapter1)** Security Mechanisms, Services and Attacks, A model for Network security **(Text1: Chapter1: 3, 4, 5, 6)** Network Access Control, Extensible Authentication Protocol **(Text1: Chapter 16: Section 1,2)**	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2

Module-2	**08 hrs**
Transport Level Security: Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS, Secure Shell (SSH) **(Text1: Chapter15)**	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-3	**08 hrs**
IP Security: Overview of IP Security (IPSec), IP Security Architecture, Modes of Operation, Security Associations (SA), Authentication Header (AH), Encapsulating Security Payload (ESP), Internet Key Exchange. **(Text1: Chapter19)**	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3

Module-4	**08 hrs**
Intruders: Intruders, Intrusion Detection, Password Management. **(Chapter20-Text1)** **MALICIOUS SOFTWARE:** Viruses and Related Threats, Virus Countermeasures, **(Chapter21-Text1)**	
Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	L1, L2, L3

Module-5	**08 hrs**
Firewalls: The Need for firewalls, Firewall Characteristics, Types of Firewalls, Firewall Biasing, Firewall location and configuration **(Chapter 22-Text 1)**	
Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

1. Explain network security services and mechanisms and explain security concepts
2. Understand the concept of Transport Level Security and Secure Socket Layer.
3. Explain Security concerns in Internet Protocol security
4. Explain Intruders, Intrusion detection and Malicious Software
5. Describe Firewalls, Firewall Characteristics, Biasing and Configuration

Suggested Learning Resources:

Text Books:

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 5th Edition, 2014, ISBN: 978-81-317- 6166-3
2. Atul Kahate, "Cryptography and Network Security", TMH, 2003.

Reference Books:

1. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.
2. Introduction to Computer Security, Matt Bishop, Sathyanarayana S V, Pearson Education, 2006, ISBN 81-7758-425/1

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2												3	
CO2	3	2												3	
CO3	3	2												3	
CO4	3	2	2		2		1		1					3	
CO5	3	2	2		2		1		1					3	

High-3, Medium-2, Low-1

VII Semester

FABRICATION TECHNOLOGY			
Course Code:	21ECT7043	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

1. To be able to understand Scope of semiconductor Materials and Devices.
2. To be able to understand the Process of Crystal Growth.
3. To be able to understand the Photolithography and Etching.
4. To be able to classify the Diffusion and Ion Implantation.
5. To be able to understand the Film Deposition and Process Integration.

Module-1	**08 hrs**

Introduction to Semiconductor: Semiconductor Materials, Devices, Semiconductor process technology-key semiconductor technology, technology trends. Basic Fabrication Steps-oxidation, photolithography, etching, diffusion, Ion Implantation and metallization. **Text 1**

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-2	**08 hrs**

Crystal Growth: Silicon crystal growth from the melt-starting material, czochralski technique, distribution dopant, effective segregation coefficient. Silicon float zone process. GaAs crystal growth techniques- starting materials, crystal growth techniques. Material characterization- wafer shaping, crystal characterization. **Text 1**

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-3	**08 hrs**

Etching: Wet chemical etching-Si etching, Silicon dioxide etching, silicon Nitride and poly silicon etching, Aluminum etching and GaAs etching. Dry etching- Plasma Fundamentals, Etch mechanism. **Text 1**

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3

Module-4	**08 hrs**

Diffusion and Ion Implantation: Basic Diffusion Process, Diffusion profiles. Extrinsic Diffusion and Lateral diffusion.

Introduction Ion Implantation: Range of Implanted Ions- Ion Distribution, Ion Stopping, Ion Channeling. **Text 1**

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	L1, L2, L3

Module-5	**08 hrs**

Film Deposition and Process Integration: Epitaxial Growth Techniques- Chemical Vapor Deposition. Structures and Defects in Epitaxial Layers, Dielectric Deposition- Si Dioxide, Si Nitride. Poly silicon Deposition. Metallization- Aluminum Metallization and copper Metallization. **Text 1**

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO 1 - Identify the Semiconductor Materials.
CO 2 - Ability to interpret Fabrication Steps.
CO 3 - Creation of semiconductor devices
CO 4 - Understand the types of Diffusion and Ion Implantation.
CO 5 - Ability to Compare the types of Diffusion and Ion Implantation.

Suggested Learning Resources:

Text Books:

1. Gary S. May, Simon M. Sze, **"Fundamentals of Semiconductor Fabrication"** Wiley, 1st Edition, 2003.

Reference Books:

1. Anderson, Anderson" **Fundamentals of Semiconductor Devices**" McGraw-Hill Education, Indian Edition 2013.

2. Gary S. May, Costas J S, **"Fundamentals of Semiconductor Manufacturing and Process Control**" Wiley IEEE Press, 1st Edition, 2006

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	1			2		3	2							
CO2	3	1			2		3	2							
CO3	3	1			2		3	2							
CO4	3	1			2		3	2							
CO5	3	1			2		3	2							

High-3, Medium-2, Low-1

VII Semester

MACHINE LEARNING WITH PYTHON

Course Code:	21ECT7044	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

- To understand the basic theory underlying machine learning.
- To be able to formulate machine learning problems corresponding to different applications.
- To understand a range of machine learning algorithms along with their strengths and weaknesses.
- To be able to apply machine learning algorithms to solve problems of moderate complexity.
- To apply the algorithms to a real-world problem, optimize the models learned and report on the expected accuracy that can be achieved by applying the models.

Module-1	**08 hrs**

Introduction: Introduction to Machine Learning, Building intelligent machines to transform data into knowledge, The three different types of machine learning, An introduction to the basic terminology and notations, A roadmap for building machine learning systems, Using Python for machine learning. Training Machine Learning Algorithms for Classification Artificial neurons – a brief glimpse into the early history of machine learning, Implementing a perceptron learning algorithm in Python, Adaptive linear neurons and the convergence of learning. Textbook 1: Chapters 1, 2

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-2	**08 hrs**

A Tour of Machine Learning Classifiers Using Scikit-Learn Choosing a classification algorithm, First steps with scikit-learn, Modeling class probabilities via logistic regression, Maximum margin classification with support vector machines, Solving nonlinear problems using a kernel SVM, Decision tree learning, K-nearest neighbors – a lazy learning algorithm

Building Good Training Sets – Data Preprocessing Dealing with missing data, Handling categorical data, Partitioning a dataset in training and test sets, Bringing features onto the same scale, Selecting meaningful features, Assessing feature importance with random forests. Textbook 1: Chapters 3 ,4

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-3	**08 hrs**

Compressing Data via Dimensionality Reduction Unsupervised dimensionality reduction via principal component Analysis, Supervised data compression via linear discriminant analysis, Using kernel principal component analysis for nonlinear mappings Learning Best Practices for Model Evaluation and Hyperparameter Tuning Streamlining workflows with pipelines, Using k-fold cross-validation to assess model performance, Debugging algorithms with learning and validation curves, Fine-tuning machine learning models via grid search, Looking at different performance evaluation metrics Applying Machine Learning to Sentiment Analysis Obtaining the IMDb movie review dataset, Introducing the bag-of-words model, training a logistic regression model for document classification , Working with bigger data – online algorithms and out-of-core learning Textbook 1: Chapters 5,6,8

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation,

RBT Level:	L1, L2, L3

Module-4	**08 hrs**

Embedding a Machine Learning Model into a Web Application Serializing fitted scikit-learn estimators, Setting up a SQLite database for data storage, Developing a web application with Flask, Turning the movie classifier into a web application, Deploying the web application to a public server Predicting Continuous Target Variables with Regression Analysis Introducing a simple linear regression model, Exploring the Housing Dataset, Implementing an ordinary least squares linear regression model, Fitting a robust regression model using RANSAC, Evaluating the performance of linear regression models, Using regularized methods for regression- Turning a linear regression model into a curve – polynomial regression Textbook 1: Chapters 9,10

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	L1, L2, L3

Module-5	**08 hrs**

Working with Unlabeled Data – Clustering Analysis Grouping objects by similarity using k-means, Organizing clusters as a hierarchical tree, Training Artificial Neural Networks for Image Recognition Modeling complex functions with artificial neural networks, Classifying handwritten digits, Training an artificial neural network, Other neural network architectures Textbook 1: Chapters 11,12

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO1. Appreciate the importance of visualization in the data analytics solution

CO2. Apply structured thinking to unstructured problems

CO3. Understand a very broad collection of machine learning algorithms and problems

CO4. Learn algorithmic topics of machine learning and mathematically deep enough to introduce the required theory

CO5. Develop an appreciation for what is involved in learning from data.

Suggested Learning Resources:

Text Books:

1. Python Machine Learning by Sebastian Raschka, Published by Packt Publishing Ltd.
2. Machine Learning with Python for Everyone by Mark E Fenner
3. Machine Learning using Python by Manaranjan Pradhan & U Dinesh Kumar
4. Practical Machine Learning with Python by Dipanjan Sarkar, Raghav Bali &Tushar Sharma

Web links and Video Lectures (e-Resources)

•https://www.youtube.com/watch?v=RnFGwxJwx-0

https://www.youtube.com/watch?v=eq7KF7JTinU

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3									1	1	1	1	1
CO2		3	3	2	2	2	2	1	1				1	1	1
CO3	3	2	3	2	1	2							1	1	1
CO4	3	3	2	2	2	2	3	1	1				1	1	1
CO5	2	2	3	3	2	2	1	1	1				1	1	1

High-3, Medium-2, Low-1

VII Semester

MULTIMEDIA COMMUNICATION			
Course Code:	**21ECT7045**	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

- Understand the importance of multimedia in today's online and offline information sources and repositories.
- Understand the how Text, Audio, Image and Video information can be represented digitally in a computer so that it can be processed, transmitted and stored efficiently.
- Understand the Multimedia Transport in Wireless Networks
- Understand the Real-time multimedia network applications.
- Understand the Different network layer based application

Module-1	**08 hrs**
Multimedia Communications: Introduction, Multimedia information representation, Multimedia networks, multimedia applications, Application and networking terminology. (Chapter 1 of Text 1)	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2
Module-2	**08 hrs**
Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video. (Chapter 2 of Text 1)	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3
Module-3	**08 hrs**
Text and Image Compression: Introduction, Compression principles, text compression, image Compression. (Chapter 3 of Text 1)	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3
Module-4	**08 hrs**
Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression. (Chapter 4 of Text 1)	
Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	L1, L2, L3
Module-5	**08 hrs**
Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI Highspeed LANs, LAN protocol (Chap. 8 of Text 1).	
Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

the end of the course the student will be able to:
1. Understand basics of different multimedia networks and applications.
2. Understand different compression techniques to compress audio and video.
3. Describe multimedia Communication across Networks.
4. Analyse different media types to represent them in digital form.
5. Compress different types of text and images using different compression techniques.

Suggested Learning Resources:

Text Books:

Multimedia Communications- Fred Halsall, Pearson Education, 2001, ISBN -978813170994

Reference Books:

1. Multimedia: Computing, Communications and Applications- Raif Steinmetz, Klara Nahrstedt, Pearson Education, 2002, ISBN-978817758
2. Fundamentals of Multimedia – Ze-Nian Li, Mark S Drew, and Jiangchuan Liu.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2												3	
CO2	3	2												3	
CO3	3	2												3	
CO4	3	2	2		2		1		1					3	
CO5	3	2	2		2		1		1					3	

High-3, Medium-2, Low-1

VII Semester

OPTICAL & SATELLITE COMMUNICATION			
Course Code:	21ECT7051	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

Learn the basic principle of optical fiber communication with different modes of light propagation.

- Understand the transmission characteristics and losses in optical fiber.
- Study of optical components and its applications in optical communication networks.
- Understand the basic principle of satellite orbits and trajectories.
- Study of electronic systems associated with a satellite and the earth station.
- Study satellite applications focusing various domains services such as remote sensing, weather forecasting and navigation.

Module-1	**08 hrs**
Optical Fiber Structures: Optical Fiber Modes and Configurations, Mode theory for circular waveguides, Single mode fibers, Fiber materials, Photonic Crystal Fibers, Fiber Optic Cables. **Attenuation and Dispersion:** Attenuation: Absorption, Scattering Losses, Bending loss, Signal Dispersion: Modal delay, Group delay, Material dispersion. Text Book 1	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-2	**08 hrs**
Optical Sources and detectors: Light Emitting Diode: LED Structures, Light source materials, Quantum efficiency and LED power, Laser Diodes: Modes and threshold conditions, Rate equations, External quantum efficiency, Resonant frequencies, Photodetectors: The pin Photodetector, Avalanche Photodiodes. **WDM Concepts:** Overview of WDM, Isolators and Circulators, Fiber grating filters, Dielectric thin-film filters, Diffraction Gratings **Optical Amplifiers:** Basic Applications and types, Erbium doped fiber amplifiers. Text Book 1	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-3	**07 hrs**
Satellite Orbit and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits. [Text2: 2.1, 2.2, 2.3,2.4,2.5] **Satellite In-orbit Operations:** Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle. [Text2: 3.3, 3.4, 3.5, 3.6, 3.7]	
Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3

Module-4	**08 hrs**
Satellite Hardware: Satellite Subsystems, Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload. [Text2: 4.1, 4.5, 4.6, 4.7,4.8] **Earth Station:** Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking. [Text2: 8.1, 8.2, 8.3,8.4,8.5,8.6]	

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	L1, L2, L3

Module-5	**08 hrs**

Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Television, Satellite Data Communication Services.
Applications: Remote Sensing Satellites: Classification, Orbits, payloads. Weather Forecasting Satellites: Overview, Fundamentals, orbits and payload. Global Positioning Satellite System.

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

1. Classification and characterization of optical fibers and devices used for optical communication.
2. Understand the principle of operation of optical devices used for multiplexing and amplification of light.
3. Describe the satellite orbits and its trajectories with the definitions of parameters associated with it.
4. Describe the electronic hardware systems associated with the satellite subsystem and earth station.
5. Understand the functioning of satellites for communication, remote sensing, and weather and navigation applications.

Suggested Learning Resources:

Text Books:

1. Gerd Keiser, Optical Fiber Communication, 5th Edition, McGraw Hill Education (India) Private Limited, 2016. ISBN:1-25-900687-5.
2. Anil K Maini, Varsha Agrawal, Satellite Communication, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.

Reference Books:

1. John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010, ISBN:978-81-317-3266-3
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4
3. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition, 2006.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2												3	
CO2	3	2												3	
CO3	3	2												3	
CO4	3	2	2		2		1		1					3	
CO5	3	2	2		2		1		1					3	

High-3, Medium-2, Low-1

VII Semester

ARM EMBEDDED SYSTEMS			
Course Code:	21ECT7052	**CIE Marks:**	50
Teaching Hours/Week (L: T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

1. Understand the basic hardware components of embedded system.
2. Develop the hardware software co-design and embedded firmware design approaches.
3. Exposure to ARM processors and ARM based embedded systems.
4. Understand the architectural features and instructions of ARM Cortex M3 & M4 processors.
5. Explain the need of real time operating system for embedded system applications.

Module-1	**08 hrs**

Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of Embedded Systems. Elements of an Embedded System (Block diagram and explanation), Memory (ROM and RAM types), Sensors and Actuators – Light Emitting Diode (LED), 7-Segment LED Display, Keyboard, Communication Interfaces – Inter Integrated Circuit (I2C) Bus, Serial Peripheral Interface (SPI) Bus, Universal Serial Bus (USB), Infrared (IrDA), Bluetooth (BT), Wi-Fi.

Text 1

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-2	**08 hrs**

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Hardware Software Co-Design concept, Computational Models in Embedded Design, Embedded Firmware Design Approaches, Embedded Firmware Development Languages, Typical Embedded product design and development approach, Electronic Design Automation (EDA) Tools in embedded design.

Text 1

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-3	**08 hrs**

ARM Embedded System: RISC Design Philosophy, ARM design Philosophy, Embedded System hardware and Embedded System software.

ARM Processor Fundamentals: Registers, Current Program Status Registers, Pipeline, Exceptions, Interrupts and the Vector table, Core Extensions, Architecture Revisions, ARM processor families.

Text 2

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3

Module-4	**08 hrs**

ARM Cortex-M Processors: ARM processor evolution, Architecture versions, Cortex-M3 and Cortex-M4 processors, Cortex-M processor family, Differences between a processor and a microcontroller, ARM and the microcontroller vendors, Selecting Cortex-M3 and Cortex-M4 microcontrollers, Advantages of the Cortex-M processors, Applications of the ARM Cortex-M processors, Resources for using ARM

processors and ARM microcontrollers, Architecture of the Cortex-M3 and Cortex-M4 processor, Operation modes and states, Instruction set (Moving data within the processor, Arithmetic operations, Logic operations, Shift and rotate instructions), ARM programming examples.

Text 3

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	L1, L2, L3

Module-5	**08 hrs**

RTOS and IDE for Embedded System Design: The Operating System Architecture, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Multiprocessing and Multitasking, Preemptive Task scheduling techniques, How to choose an RTOS.

Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram, The Integrated Development Environment (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques.

Text 1

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

CO 1 - Describe the different elements of embedded system and their selection methods.
CO 2 - Develop the hardware Software co-design and firmware design approaches.
CO 3 - Describe the architectural features of ARM processors and ARM embedded systems.
CO 4 - Apply the knowledge gained for Programming ARM Cortex M3 & M4 for different applications.
CO 5 - Develop real time embedded system applications using suitable IDEs.

Suggested Learning Resources:

Text Books:

1. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2nd Edition.
2. Andrew N Sloss, "ARM System Developer's guide", Elsevier Publications, 2016.
3. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3 and Cortex-M4 Processors", Newnes, Elsevier.

Reference Books:

1. James K Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.
2. Yifeng Zhu, "Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", 2nd Ed., Man Press LLC ©, 2015.
3. K V K K Prasad, "Embedded real time systems", Dreamtech publications, 2003.
4. Rajkamal, "Embedded Systems",2nd Edition, McGraw hill Publications, 2010.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3				1										
CO2	3	2	2		2										
CO3	3				1										
CO4	3	2	2		2										
CO5	3	2	2	1	2										

High-3, Medium-2, Low-1

VII Semester

BASIC DIGITAL IMAGE PROCESSING			
Course Code:	21ECT7053	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

- Understand the fundamentals of digital image processing
- Understand the image enhancement techniques in spatial domain used in digital image processing
- Understand the frequency domain enhancement techniques in digital image processing
- Understand the Color Image Processing in digital image processing
- Understand the image restoration techniques and methods used in digital image processing

Module-1	**08 hrs**
Digital Image Fundamentals: What is Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels. [Text 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]	
Teaching Learning Method: **RBT Level:**	Chalk and Talk, PowerPoint Presentation L1, L2, L3
Module-2	**08 hrs**
Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters [Text 1: Chapter 3: Sections 3.2 to 3.6]	
Teaching Learning Method: **RBT Level:**	Chalk and Talk, PowerPoint Presentation L1, L2, L3
Module-3	**08 hrs**
Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters. [Text 1: Chapter 4: Sections 4.7 to 4.9]	
Teaching Learning Method: **RBT Level:**	Chalk and Talk, PowerPoint Presentation, YouTube videos L1, L2, L3
Module-4	**08 hrs**
Color Image Processing: Color Fundamentals, Color Models, Pseudo-color Image Processing. [Text 1: Chapter 6: Sections 6.1 to 6.3]	
Teaching Learning Method: **RBT Level:**	Chalk and Talk, Power point presentations L1, L2, L3
Module-5	**08 hrs**
Restoration: A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering. [Text 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8]	
Teaching Learning Method: **RBT Level:**	Chalk and Talk, Power point presentations **RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

1. Understand image formation and the role of human visual system plays in perception of gray and color image data.
2. Apply image processing techniques in spatial domains.
3. Apply image processing techniques in frequency (Fourier) domains.
4. Conduct independent study and analysis of Image Enhancement techniques.

Suggested Learning Resources:

Text Book:

1. Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3rd Edition, 2010.

Reference Books:

1. Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014.
2. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2												3	
CO2	3	2												3	
CO3	3	2												3	
CO4	3	2	2		2		1		1					3	
CO5	3	2	2		2		1		1					3	

High-3, Medium-2, Low-1

VII Semester

CRYPTOGRAPHY			
Course Code:	**21ECT7054**	**CIE Marks:**	40+5+5
Teaching Hours/Week (L:T:P:S):	3: 0: 0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	3	**Exam Hours:**	03

Course objectives:

This course will enable students to:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Information Security with knowledge of mathematical concepts required for cryptography.
- Core Competence: To equip students with a basic foundation of Cryptography by delivering the basics of symmetric key, public key cryptography and authentication techniques

Module	Syllabus Content	No of Hours
1	**Introduction:** Services, mechanisms and attacks, OSI security architecture, Model for network security. **Symmetric ciphers:** Symmetric Cipher Model, Substitution Techniques: Caesar Cipher, Mono Alphabetic Cipher, Playfair Cipher, Hill Cipher, polyalphabetic Cipher and One-Time Pad (OTP). Transposition Techniques, Rotor Machines, Steganography.	08
2	**Finite Fields:** Groups, Rings, Fields. Modular Arithmetic: Divisors, properties of modulo operator, modular arithmetic operations and properties. Euclid's Algorithm, Greatest Common Divisor (GCD), finding GCD. Finite Fields ofthe form GF (p): Finite fields of order p.	08
3	Private Key Encryption: Simplified DES, Block Cipher Principles, Data encryption standard (DES), Strength of DES, Block Cipher Design Principles and Block Cipher Modes of Operation, Evaluation Criteria for Advanced Encryption Standard, The AES Cipher.	08
4	Public Key Encryption: Principles of Public-Key Cryptosystems, The RSA algorithm. Key Management, Diffie - Hellman Key Exchange.	08
5	Authentication Functions and Hash Functions: Authentication functions, message authentication codes, hash functions, security of Hash functions and MACs	07

Course outcomes:

At the end of the course, the student will be able to:

At the end of the course the student will be able to:

1. Explain traditional cryptographic algorithms of encryption and decryption process.
2. To apply the concepts of number theory, abstract algebra that are required for Cryptographic algorithms
3. Use symmetric cryptography algorithms to encrypt and decrypt the data.
4. Use asymmetric cryptography algorithms to encrypt and decrypt the data.
5. Explain the methods used for authentication.

Suggested Learning Resources:

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3

Reference Books:

1. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.
3. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.

Weblink:

https://nptel.ac.in/courses/106105031

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Group Activity can be given to improve programming skills

VII Semester

E-WASTE MANAGEMENT			
Course Code:	21ECT7055	**CIE Marks:**	50
Teaching Hours/Week (L:T:P:S):	3:0:0:0	**SEE Marks:**	50
Total Hours of Pedagogy:	40	**Total Marks:**	100
Credits:	03	**Exam Hours:**	03

Course objectives:

- **Current Status:** According to a report on e-waste presented by the United Nations (UN) in World Economic Forum on January 24, 2019, the waste stream reached 48.5 MT in 2018. With such a large quantity of e-waste being generated each year, the future of e-waste recycling in India looks pretty bright. The E-waste (Management) Rules, 2016, enacted on October 1, 2017, added over 21 products (Schedule-I) under the purview of the rule.
- **Purview:** This course covers an extensive review of e-waste management in India. With a focus on the evolution of legal frameworks in India and the world, it presents impacts and outcomes; challenges and opportunities; and management strategies and practices to deal with e-waste. It also includes a survey of pan-India initiatives and trajectories of law-driven initiatives for effective ewaste management along with responses from industries and producers.
- **Scope:** There is a considerable scope for e-waste recycling in India. It is not only a solution to help mitigate e-waste management issues, but it also helps to generate employment. With the rise in ewaste recycling plants, the demand for employees with all levels of qualification and skills also increases.

Module-1	**08 hrs**

Sustainable development and e-waste management: Importance of electrical and electronic equipment in a nation's development, and e-waste as toxic companion of digital era, I: Let's understand e-waste, II: E-waste statistics: quantities, collection and recycling, E-waste categories and harmonising statistics, III: An overview on status of e-waste related legislation across the globe; IV: UN initiatives for e-waste management: creating partnerships and achieving Agenda 2030; V: Indian scenario: e-waste generation, collection and recycling.

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-2	**08 hrs**

Extended producer responsibility: a mainstay for e-waste management: Evolution of concept of 'extended producer responsibility', EPR applied for waste management and extended for e-waste management, EPR: goals, implementation, and challenges for e-waste management, EPR implemented for e-waste management under the existing regulatory frameworks in different countries, Role of a PRO prescribed in regulatory framework, Considerations for successful implementation of EPR, Challenges in implementation of EPR for e-waste management, Impact of EPR, EPR and e-waste management in India.

Toxicity and impacts on environment and human health: Toxicity, recycling, and regulations, I: Environmental concerns, II: Human health concerns.

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation
RBT Level:	L1, L2, L3

Module-3	**08 hrs**

Treating e-waste, resource efficiency, and circular economy: Safe environment, resource use, and circular economy, Circular economy: recycling, resource recovery, and resource efficiency, Potentials of urban mining in circular economy, Recycling and resource efficiency related challenges to the circular economy, Urban mining, recycling, resource use, resource efficiency, and circular economy in

India.

E-waste management through legislations in India: I: Historical backdrop of regulatory regime for e-waste in India, II: E-waste (management) Rules, 2016 and E-waste (management) Amendment Rules, 2018, III: Analysing performance of EPR and CPCB as regulatory mechanisms, IV: Legal cases and judicial directives.

Teaching Learning Method:	Chalk and Talk, PowerPoint Presentation, YouTube videos
RBT Level:	L1, L2, L3

Module-4	**08 hrs**

Strategies and initiatives for dealing with e-waste in India: I: Overview of pan-India initiatives for dealing with e-waste during 2000 and 2012, II: Law-driven e-waste management – initiatives by the government, non-government agencies, and judiciary.

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	L1, L2, L3

Module-5	**08 hrs**

Moving towards horizons: I: Legal and judicial domain, II: Economic concerns, III: Environment concerns, IV: Recycling culture/recycling society

Teaching Learning Method:	Chalk and Talk, Power point presentations
RBT Level:	**RBT Level:** L1, L2, L3

Course outcomes:

At the end of the course the student will be able to:

1. Understand the existing discourse on e-waste and its management, statistics across the world, opportunities, and challenges w.r.t. regulatory framework, SDGs, CE, and LCIA (Life Cycle Impact Assessment) and MFA (Material Flow Analysis), Indian scenario.
2. Describe EPR, a regulatory framework for achieving specified goals across different countries and impacts on environment and human health.
3. Explain themes in the context of resource use and sustainable development. Urban mining, informal sector operations and need for resource use policy, financial support for recycling infrastructure building, etc. in Indian context and also explain to what extent – different aspects of e-waste management have been incorporated in the existing regulatory framework in comparison with international legislatures.
4. Identify and infer pan-Indian initiatives dealing with e-waste management, ranging from building knowledge base through research and social action by different stakeholders to technological and legal advancements, and industrial initiatives. Analyse roadmap for the Agenda 2030.
5. Use opportunities and challenges around four domains: legal and judicial domain; economic concerns; recycling culture/society; and environment concerns.

Suggested Learning Resources:

Text Books:

1.Varsha Bhagat Gangulay, 'E-Waste Management', Taylor and Francis, 2022

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2												3	
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CO5	3	2	2		2		1		1					3	

High-3, Medium-2, Low-1