

Dr Hemalatha K N

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Expertise

Electrical and Electronic Engineering

Areas of interest include digital design, analog & mixed mode VLSI design , Verilog HDL, CMOS VLSI design, Analog Electronics, rreversible logic

Work experience

1. Dr Ambedkar Institute of Technology, Bengaluru 2007 — Present

Assistant Professor Bengaluru

Education

1. Ph.D - 2023

RNS Institute of Technology

Membership In Professional Bodies

- 1. **ISTE**, 2020 Life member
- 2. ISSS, 2010 Life Member, 2010 Life member
- 3. CRSI, 2010 Life member

Membership In Committees

Publication

1. State-Of-The-Art On Reversible Multiplier Architectures and Its Comparison for Future Quantum Computing

Hemalatha K N, Sangeetha B G Gazi University Journal of Science, Volume , Year 2023, Pages

2. Design and Implementation of 64-Bit Ripple Carry Adder and Ripple Borrow Subtractor Using Reversible Logic Gates

Hemalatha K N, Aishwarya Kamakodi, A Soppia, A Poornima, Sangeetha B G Int. J. Advanced Networking and Applications, Volume Volume: 13 Issue: 06, Year 2022, Pages 5215-5219

3. Efficient Design of Compact 8-bit Wallace Tree Multiplier Using Reversible Logic

Hemalatha K N, Sangeetha B G I. J. Engineering and Manufacturing, Volume , Year 2022, Pages 29-36

4. Optimized 64-bit Reversible BCD Adder for Low-power Applications and Its Comparative Study

Hemalatha K N, Girija S, Sangeetha B G Proceedings of the International Conference on Computational Intelligence and Sustainable Technologies ICoCIST 2021, Volume , Year 2021, Pages

5. Ultra-Optimized 8-bit Unsigned Array Multiplier design using Reversible Logic

Hemalatha K N, Sangeetha B G GIS SCIENCE JOURNAL, Volume VOLUME 8, ISSUE 1,, Year 2021, Pages 1105-1110

6. Performance Analysis of Array Multiplier Using Reversible Logic

Hemalatha K N, Sangeetha B G

Microelectronics, Communication Systems, Machine Learning and Internet of Things Select Proceedings of MCMI 2020, Volume , Year 2020, Pages

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